The documentation and process conversion measures necessary to comply with this revision shall be completed by May 01, 2023

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PERFORMANCE SPECIFICATION

INTEGRATED CIRCUITS (MICROCIRCUITS) MANUFACTURING, GENERAL SPECIFICATION FOR

AMSC N/A

FSC 5962

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This specification is approved for use by all Departments and Agencies of the Department of Defense.

This document is a performance specification. It is intended to provide the device manufacturers an acceptable established baseline in order to support Government microcircuit application and logistic programs. The basic section of this specification has been structured as a performance specification, which is supplemented with detailed appendices. These appendices provide guidance to manufacturers on demonstrated successful approaches to meeting military performance needs. These appendices are included as a benchmark and are intended to impose performance requirements. For QML microcircuits the manufacturer is required to develop a program plan that meets or exceeds the performance detailed in these appendices (see appendices A, G, H, and J). Appendix A is mandatory for manufacturers of device types supplied in compliance with MIL-STD-883 and forms the basis for QML classes Q, V and Y. Appendix B is intended for space application and is required for class V, class Y and class P (class level S) devices. Appendix C is mandatory for devices requiring radiation hardness assurance (RHA). Appendix D is mandatory for statistical sampling, life test, and qualification procedures used with microcircuits.

1. SCOPE

1.1 Scope. This specification establishes the general performance requirements for integrated circuits or microcircuits and the quality and reliability assurance requirements, which are to be met for their acquisition. The intent of this specification is to allow the device manufacturer the flexibility to implement best commercial practices to the maximum extent possible while still providing product that meets military performance needs. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended will be specified in the device specification. Quality assurance requirements outlined herein are for all microcircuits built on a manufacturing line which is controlled through a manufacturer's quality management (QM) program and has been certified and qualified by the Qualifying Activity (QA) in accordance with requirements herein. Several levels of product assurance including RHA are provided for in this specification. The certification and qualification sections found herein outline the requirements to be met by a manufacturer to be listed on a Qualified Manufacturer Listing (QML). After listing of a technology flow on a QML, the manufacturer is to continually meet or improve the established baseline of certified and qualified procedures, the QM program, the manufacturer's review system, the status reporting, and quality and reliability assurance requirements for all QML products. The manufacturer may present alternate methods of addressing the requirements contained in this specification. These alternate methods will be approved by the Qualifying Activity. This specification requires a manufacturer to establish a process flow baseline. If sufficient quality and reliability data is available, the manufacturer, through the QM program and the manufacturer's review system, may modify, substitute, or delete tests. Additional information on the QML process and its philosophy is available in 6.5 herein. Class T is not for use in National Aeronautics and Space Administration (NASA) manned, satellite, or launch vehicle programs without written permission from the applicable NASA project office (e.g., cognizant electrical, electronic, and electromechanical (EEE) parts authority).

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3 or 4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3 or 4 of this specification, whether or not they are listed.

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2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-M-38510	- Microcircuits, General Specification For
MIL-PRF-123	- Capacitors, Fixed, Ceramic Dielectric (Temperature stable and general purposes), High Reliability, General Specification For
MIL-PRF-55681	- Capacitors, Chip, Multiple Layers, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, General Specification For
MIL-PRF-32535	- Capacitors, BME Chip, Multiple Layers, Fixed, Ceramic Dielectric, Established Reliability and Non-Established Reliability, General Specification For

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883	- Test Method Standard Microcircuits
MIL-STD-1285	- Marking of Electrical and Electronic Parts

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103	- List of Standard Microcircuit Drawings
MIL-HDBK-780	- Standard Microcircuit Drawings
MIL-HDBK-1331	- Parameters to be Controlled for the Specification of Microcircuits, Handbook For

(Copies of these documents are available online at https://quicksearch.dla.mil/)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

QML-38535	Qualified Manufacturers List of Products Qualified Under Performance Specification MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification For

(Copies of these documents are available online at https://quicksearch.dla.mil/)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1269	- Test Methods for Destructive Shear Testing of Ball Bonds.

(Copies of this document are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

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JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP121	- Requirements for Microelectronic Screening and Test Optimization.
JEP163	- Selection of Burn-in/Life Test Conditions and Critical Parameters for QML Microcircuits.
JESD31	- General Requirements for Distributors of Commercial and Military Semiconductor Devices.
JESD471	- Symbol & Label for Electrostatic Sensitive Devices.
JESD625	- Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.
JESD22-B101	- External Visual.
JESD22-A102	- Accelerated Moisture Resistance - Unbiased Autoclave.
JESD22-A110	- Highly Accelerated Temperature and Humidity Stress Test (HAST) – biased.
JESD22-B117	- Solder Ball Shear.
JESD22-A118	- Highly Accelerated Temperature and Humidity Stress Test (HAST) – unbiased.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

ANSI/ESDA/JEDEC JOINT STANDARD

ANSI/ESDA/JEDEC JS-001 - For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level.

ANSI/ESDA/JEDEC JS-002 - For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) - Device Level.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.) or

(Copies of these documents are available online at https://www.esda.org/ or from Electrostatic Discharge Association(ESDA) 7900 Turin Road, Bldg. 3, Rome, NY 13440.)

ELECTROSTATIC DISCHARGE ASSOCIATION (ESDA)

ANSI/ESDA S20.20 – For the Development of an Electrostatic Discharge Control Program for- Protection of Electrical and Electronics parts, Assemblies and equipment.

(Copies of these documents are available online at https://www.esda.org/ or from Electrostatic Discharge Association(ESDA) 7900 Turin Road, Bldg. 3, Rome, NY 13440.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 General. The manufacturer of QML microcircuits in compliance with this specification shall have or have access to and use of production and test facilities, and a QM program to assure successful compliance with the provisions of this specification. All microcircuits manufactured on a QML line shall be processed on a QA certified fabrication line, and shall be assembled on a QA certified assembly line. All microcircuits shall be electrically capable of meeting parameters over the specified temperature range in accordance with the device specification in a QA certified test facility. The QML manufacturer shall be capable of demonstrating their ability to develop hardware and software test programs before delivery of the product. The QML certification mark (3.6.3) indicates compliance to all the performance provisions of this specification. The requirements described herein shall be addressed in one of two ways. These are as follows:

a. As specified herein.

b. Demonstration to the qualifying activity (QA) and validation team when applicable, of an alternate method, that assures at least the same level of quality and reliability as defined by the requirements herein, or demonstration to the QA that the requirement is not applicable to the manufacturer's technology.

NOTE: A QML manufacturer may modify screening and Technology Conformance Inspection (TCI) requirements of the device specification or Standard Microcircuit Drawing (SMD) under special criteria defined within this specification and as defined in the manufacturer's QM plan. (For guidance on screening and QCI optimization see JEP121 - Requirements for Microelectronic Screening and Test Optimization and J.3.12 herein.) These changes cannot affect any thermal, mechanical, electrical parameters, or radiation levels (when applicable) which affect form, fit, or function of the device, defined within the device specification or SMD.

3.1.1 Reference to applicable device specification. For purposes of this specification, when the term "as specified" is used without additional reference to a specific location or document, the intended reference shall be to the device specification.

3.2 Item requirements. The individual item requirements, including temperature range, for integrated circuits delivered under this specification shall be documented in the device specification prepared in accordance with 3.5 herein. Devices produced under this specification may have any operating temperature range (case, ambient, or junction) as long as it is specified in the device specification, and any references to minimum or maximum operating temperatures shall refer to the respective lower and upper limits of this range. However, the manufacturer shall demonstrate the operating temperature range (case, ambient, or junction) capability of the technology being offered. The standard evaluation circuit (SEC) is typically used for this demonstration.

3.2.1 Certification of conformance and acquisition traceability. Manufacturers or suppliers including distributors who offer QML microcircuits described by this specification shall provide written certification, signed by the corporate officer who has management responsibility for the production of the QML microcircuits, (1) that the QML microcircuits being supplied have been manufactured and meet the performance defined in the specification whether or not the actual testing has been performed, (2) that all QML microcircuits are as described on the certificate of conformance which accompanies the shipment, and (3) that dealers and distributors have handled the QML microcircuit in accordance with the requirements of JESD625 or ANSI/ESDA S20.20 and JESD31. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate of conformance (such as members of the manufacturer's review system), but, the responsibility for conformity with the facts shall rest with the responsible corporate officer. The certification shall be confirmed by documentation to the Government or to users with Government contractors or subcontractors, regardless of whether the QML microcircuits are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. The certificate shall include the following information:

a. Manufacturer documentation:

(1) Manufacturer's name and address.

(2) Customer's or distributor's name and address.

(3) Device type.

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(4) Date code and latest re-inspection date, if applicable.

(5) Quantity of devices in shipment from manufacturer.

(6) Statement certifying QML microcircuit conformance and traceability.

(7) Solderability re-inspection date, if applicable.

(8) Signature and date of transaction.

(9) If applicable, the certificate shall include a statement indicating that alternate die/fab requirements are being used ("QD" certification mark, see 3.6.3).

b. Distributor documentation for each distributor:

(1) Distributor's name and address.

(2) Name and address of customer.

(3) Quantity of devices in shipment.

(4) Latest re-inspection date, if applicable.

(5) Certification that this shipment is a part of the shipment covered by the manufacturer's documentation.

(6) Solderability re-inspection date, if applicable.

(7) Signature and date of transaction.

3.3 Quality management (QM) program. A QM program shall be implemented by the manufacturer (see G.3.1).

3.3.1 Manufacturer's review system. The Technology Review Board (TRB) (See G.3.2) shall implement a dedicated system of review. The TRB shall review, approve and document the implementation of the QM program, as reflected in the QM plan; maintenance of all certified and qualified processes; process change control; reliability data analysis, failure analysis (FA), and corrective actions; QML microcircuit recall procedures; and qualification status of the technology.

3.3.2 QM plan. A QM plan reflects the major elements of the manufacturer's QML process (see G.3.3). The QM plan shall be kept current and up-to-date and shall reflect all major changes. Whenever the TRB makes major changes to the QM plan, copies of the updated QM plan shall be submitted to the QA for review. The manufacturer's Technology Review Board (TRB) shall establish appropriate burn-in and life test methodology for new product families or technology by using JEDEC publication JEP163 in order to meet the quality and reliability performance requirements of MIL-PRF-38535. The burn-in and life test methodology shall be documented to the manufacturer's Quality Management (QM) plan and devices specification e.g. standard microcircuit drawing (SMD). However, JEP163 requirement shall not be applicable for legacy/heritage products and technologies.

3.3.3 Self-assessment program. The manufacturer's TRB shall ensure that a self-assessment program is implemented and perform evaluations on a periodic basis of all areas controlled by the QM Plan. Results of the self-assessment including corrective actions shall be documented by the TRB and shall be made available for review to the QA (see G.3.1).

3.3.4 Change control procedures. The manufacturer shall have a system that shall provide notification of change that affects form, fit, function and radiation (when applicable) to all known acquiring activities prior to the release of the affected product. The manufacturer may make notification of this change of product through the Government-Industry Data Exchange Program (GIDEP) using the Product Change Notice. In any case, the manufacturer shall assure that all known acquiring activities are notified. The following processes and procedures shall be addressed (see G.3.4):

a. Design methodology changes.

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b. Fabrication process changes.

c. Assembly process changes.

d. Package changes.

e. Test facility changes.

f. Location changes to fabrication, assembly, test, and qualification.

3.3.4.1 Discontinuation of products. The manufacturer shall have a system that provides notification of product discontinuation which comprises date of discontinuation and last times buy opportunity in advance (at least 6 month in advance) to the DLA Land and Maritime for purchasing devices.

3.4 Requirements for listing on a QML. To be listed on a QML, the manufacturer shall demonstrate compliance to the QML certification requirements (see 3.4.1), demonstrate compliance to the QML qualification requirements (see 3.4.2), and work with the DLA Land and Maritime to develop an SMD describing the candidate QML device(s) (see 3.5). An existing MIL-M-38510 device specification may be used. The QA shall verify compliance to the requirements and shall list the manufacturer's technology on the QML.

3.4.1 QML certification requirements. The manufacturers shall meet the minimum procedures and requirements in this section for QML certification of a manufacturing line. The QA shall determine adequacy and compliance to the requirements as specified herein and shall report their findings and recommendations in writing to the manufacturer's TRB. Each portion of a QML microcircuit manufacturer's line capability, including any offshore operations, may be demonstrated independently, but validation by the QA shall assess a complete technology flow. To maintain certification the manufacturer shall provide notification of change to the process baseline to the QA. For generic qualification procedures, certification shall consist of:

a. QM program documentation (see G.3.1).

b. Process capability demonstration for certification (see 3.4.1.1 and H.3.2).

c. QA management and technology validation (see 3.4.1.2).

d. All procedures used to manufacture masks for monolithic fabrication (see appendix H).

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3.4.1.1 Process capability demonstration. As part of certification, the manufacturer shall build devices, perform tests and run software benchmarks necessary to demonstrate that the manufacturer has a comprehension of the capability of the manufacturing process as related to quality, reliability and producibility. The summary of the results of all of these tests shall be available for review by the QA (prior to scheduling a validation review). These tests shall be designed to be used as a continual check of the process capability as well as an initial demonstration of such capability. The TRB shall determine when such tests are to be performed after initial certification.

Process capability demonstration shall consist of:

a. Design.

(1) Circuit.

(2) Package.

b. Wafer fabrication.

c. Statistical process control (SPC) and in-process monitoring programs including the technology characterization vehicle (TCV) program, the SEC, and parametric monitors (PMs) (see appendix H).

d. Wafer acceptance plan.

e. Assembly and packaging.

f. RHA (see appendix C).

g. Testing (Wafer and Packaged level, as applicable).

3.4.1.1.1 New technology insertion. The supplier shall establish a new technology insertion program for the identification, management, and tracking of new technology. The program shall include a plan that defines the new technology, and the criteria and methodology for characterization and qualification of new technology. It shall also include the specific details of determining the potential failure mechanisms and activation energies and their respective mitigation strategies. The new technology insertion program, plan and methods shall be reviewed by the qualifying activity.

3.4.1.2 Management and technology validation. The validation by the QA shall include, as a minimum, the following applicable areas of each of the manufacturer's facilities including second and third party facilities: Management quality assurance, design, mask, wafer fabrication, assembly and package, and electrical environmental and radiation test, when applicable. This validation procedure shall involve a QA review of the manufacturer's QM plan, self-validation and an on-site visit of the manufacturer's fabrication, assembly, test and other facilities as necessary.

3.4.1.3 On-site validation. Manufacturer shall make available to the QA all data needed to support QM policy and procedures. QA access to manufacturing (fab and assembly) , testing facilities and operators including offshore shall be required. For first time QML supplier certification, an on-site QA validation review of the manufacturer's design, wafer fabrication, assembly, and test facilities shall be required. After the initial qualification is accomplished and with the approval of the Qualifying Activity, an established manufacturer may add other design, wafer fabrication, assembly, and test facilities upon completion of the appropriate qualification testing, and a TRB self-assessment and approval. The QA reserves the right to perform on-site reviews of any facilities/technologies that the manufacturer plans to add to their QML listing. Validation of third party suppliers is the responsibility of the manufacturer.

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3.4.1.3.1 Second and third party validations. A QML certified manufacturer may use second party facilities with the approval of the QA. A second party facility shall be a QML certified manufacturer facility or a facility that has been granted approval by the QA for the manufacture or test of QML product. The QA is responsible for the initial and periodic validation of second party facilities. The process used by the manufacturer's TRB to initially validate, and to periodically revalidate, a third party facility shall be reviewed during the initial QML validation process. For third party facilities the QA shall make a determination whether an onsite certification is required for class level S product. The QA reserves the right to visit third party facilities to verify that the manufacturer's on-going validation process is effective.

3.4.1.3.2 Radiation source of supply (RSS) validations. An RSS shall receive a QML validation for all processes listed in this specification and the RSS's program plan. This includes a QML validation of the manufacturing process and laboratory suitability of the RHA test facilities.

3.4.1.4 Technology validation. The manufacturer's technology flow shall be reviewed and approved by the QA. Some critical areas which shall be assessed by the QA, as applicable during the validation, are:

a. Design center procedures.

b. Design review procedures.

c. Model verification.

d. Software configuration and configuration management.

e. Testability procedures and policies (e.g., Joint Test Action Group (JTAG)) as applicable.

f. Archival system (e.g., very high speed integrated circuit (VHSIC) hardware description language (VHDL)).

g. Mask validation/inspection procedures.

h. TCV, SEC, PM tests, and data.

i. Fabrication rework procedures.

j. SPC program (all areas).

k. Design rule documentation.

l. Clean room procedures.

m. Wafer traceability.

n. Gallium Arsenide (GaAs) wafer boule evaluation procedure.

o. Assembly rework procedure.

p. Die attach procedures.

q. Wire/ribbon bonding.

r. Device traceability and travelers.

s. Lot formation (wafer, device and inspection).

t. Assembly area environmental control.

u. Internal gas analysis control program.

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v. Electrostatic discharge (ESD) control and testing.

w. Visual inspection.

x. Human contamination prevention procedures.

y. Equipment calibration and maintenance.

z. Training policy and procedures.

aa. Electrical test procedures.

bb. Screening procedure.

cc. TCI procedures.

dd. Third party design center procedures.

ee. Change control procedure.

ff. Chip encapsulation/molding.

gg. Qualification test plan.

hh. Characterization procedures.

ii. Selection of suppliers.

jj. New technology/materials evaluation.

kk. Package integrity demonstration test plan (PIDTP).

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3.4.1.4.1 Package design selection reviews. The manufacturer shall establish and implement systematic package design or selection reviews to ascertain compatibility of chip(s) and packages with respect to thermal, electrical and mechanical performance and manufacturing, testing, and reliability requirements. Manufacturer's package element material and finish shall be in accordance with A.3.5.6 unless otherwise specified in the manufacturer's QM plan.

3.4.1.5 Manufacturer self-validation. The manufacturer shall perform a self-validation to determine compliance to the QM plan (see appendix G).

3.4.1.6 Change management system. The manufacturer shall have a system for change management. This system shall include a process to monitor internal changes and the assessment of those changes as to the impact to customers. The manufacturer shall analyze the impact of major changes and its effects on previously approved modifications of test (see J.3.12). An appropriate customer notification methodology shall be in place.

3.4.1.7 Deficiencies and concerns. Deficiencies and concerns shall be noted by the validation team during an exit critique and shall be followed up with a written report. The microcircuit manufacturer shall not receive a letter of certification until all certification requirements are met.

3.4.1.8 Letter of certification. After validation, the QA shall issue a letter of certification to the manufacturer, which shall include all certified site(s).

3.4.2 QML qualification requirements. Integrated circuits (ICs) furnished under this specification shall be products which are authorized by the QA for listing on the QML. Qualification testing shall be performed in accordance with the agreed upon qualification plan (see appendix H).

3.4.2.1 Qualification extension. When a basic plant desires to qualify a device or process flow that includes an offshore site, application for certification and qualification may be extended with QA approval under the following conditions:

a. Control and approval of the design, fab, assembly and test operations by the manufacturer's TRB is required along with periodic self-assessments of the offshore sites. The manufacturer's TRB shall review all screening and TCI tests to determine whether they should be performed exclusively in the offshore site or reserved for the basic plant in order to assure quality and reliability. The manufacturer's TRB assessment shall be made available to the QA for review or approval as appropriate.

b. QA certification of the offshore site is required. For classes Q, V, Y, N and T products all operations, sites, and plants shall be QA certified however, this certification may be issued through the manufacturer's TRB with QA approval. Validation of these offshore operations is also required. For assembly site(s) an initial site shall be certified and qualified by the QA. Additional assembly sites shall be assessed subsequent to the initial validation.

c. All operations, flows, quality control procedures and test standards at the offshore site shall be under the control of the manufacturer's TRB. Alternately, the manufacturer shall establish a procedure for maintaining oversight of the offshore facility. All such operations, flows, procedures and test standards shall be baselined by the manufacturer's TRB and the offshore site at all times.

d. The QA reserves the right to audit the offshore site(s) with a minimum notice. The basic plant site shall be responsible to facilitate all QA site assessments. Any refusal to allow such a site assessment may result in an immediate de-certification and QML removal.

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3.4.2.2 Qualification based on package construction. When manufacturer's desire to qualify microcircuits based on packages construction under this specification shall be as specified in the associated device specification and as specified herein. Adequacy of a device manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity. Only microcircuits offered in compliance with this specification shall be specified on a Standard Microcircuit Drawing (SMD) and shall meet the following:

a. Microcircuit die shall not utilize TSV (Through Silicon Via) or TGV (Through Glass Via interconnect technology.

b. Components are essentially co-planer with each other and the topography is considered "2 dimensional". Exceptions may be allowed on case by case basis (i.e. stacked die).

c. The passive elements shall serve simple functions, directly interfacing with microcircuit ports (filtering, voltage shift, input/output conditioning, etc.) such that in a block diagram of the MIL-PRF-38535 device, the passive elements do not form any "block" (i.e., on their own constitute a network such that significant circuit function is implied independent of the microcircuit die). Refer to section 3.15 for passives allowed in construction of the microcircuit.

d. For MCMs, an interposer is allowed to be used for connectivity of multiple flip chip die and wire bonding for standard die to die connectivity.

e. The use of discrete semiconductors (diode/transistor), other complex elements/networks, thick and thin film substrate, should not be considered under MIL-PRF-38535.

3.4.3 Qualification to RHA levels. Qualification to a RHA level shall consist of characterization to the highest offered RHA level of total ionizing dose (TID). The conditions for radiation testing shall consist of exposing the devices in a step-stress manner to the highest dose level offered and as a minimum the two next consecutive lower RHA levels. The levels are identified as follows: 3 krad(Si), 10 krad(Si), 30 krad(Si), 50 krad(Si), 100 krad(Si), 300 krad(Si), 500 krad(Si), 1 Mrad(Si). The radiation testing plan (QM Plan) and qualification to the appropriate quality and reliability assurance level for device classes B, Q, S, V, Y or T shall be submitted for QA approval. The designator RHA levels are defined below:

RHA levels:

RHA level designator (see 3.6.2.1)	Total ionizing dose (TID) level in Rad (Si)
/ or -	No RHA
M	3 krad(Si)
D	10 krad(Si)
P	30 krad(Si)
L	50 krad(Si)
R	100 krad(Si)
F	300 krad(Si)
G	500 krad(Si)
H	1 Mrad(Si)

3.4.4 QML listing. A certificate of qualification shall be issued upon successful completion of all qualification tests on the two demonstration vehicles and the acceptance of the qualification documentation by the QA. Issuance of the certificate of qualification shall coincide with listing of the manufacturing line and the SMD(s), or existing MIL-M-38510 device specification(s) on the QML. The manufacturer may be removed from the QML by the QA for cause.

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3.4.5 Maintenance and retention of QML. In order to sustain qualification status after initial qualification, the manufacturer shall fabricate and perform qualification testing on the selected SEC and TCV, or approved alternate assessment procedure as defined in the QM plan.

3.4.6 QML line shutdown. If an extended shutdown of a QML certified/qualified flow is necessary, the TRB shall assess and ensure that the process is still capable when production is restarted and notify the QA.

3.4.7 Revalidation reviews. The interval between on-site revalidation reviews shall normally not exceed two years, but the QA shall adjust this interval based on the manufacturer's TRB reports, customer feedback, and other indications of the manufacturer's maintenance of the QML system.

3.4.8 Performance requirements for class T devices. The manufacturer of a class T device shall be a certified and qualified QML manufacturer approved by the QA. The class T devices shall be manufactured on a certified and qualified QML line as defined in 3.4 herein. The class T flow shall be developed and approved through the manufacturer’s TRB; shall be qualified; shall be defined in the manufacturer’s QM plan; and be approved by the QA. Each technology flow (e.g., wafer fabrication, assembly, screening, qualification, TCI, etc.) shall be developed and documented taking into account the application requirements of the customers. The device manufacturer shall demonstrate that the failure mode and mechanisms of the technologies are considered when developing the technology flow. Copies of each technology flow, including supporting documentation, shall be reviewed and approved by the QA prior to listing as an approved source of supply. Any modification to the approved technology flow shall be reviewed and approved by the TRB and the QA. The technology flow and supporting documentation shall be made available to the systems manufacturers, the Government, and customers for review. The customer shall be notified of major changes which affect form, fit, or function of the device defined within the device specification and the manufacturer’s QM plan. Class T is not for use in NASA manned, satellite, or launch vehicle programs without written permission from the applicable NASA Project Office (e.g., cognizant EEE parts authority).

3.4.8.1 Class T radiation requirements. The device specification shall define all the radiation features offered by the QML manufacturer for the class T device. QML manufacturers supplying class T devices shall meet the requirements of TM 1019 of MIL-STD-883 and shall document in the QM plan the RHA level specified for the device offered. All devices supplied to this product class shall be marked with a RHA designator as specified in 3.4.3 herein. Traceability shall be established such that there is a technical basis for compliance to the specified RHA level designator as marked on the device.

3.5 Device specification. MIL-HDBK-780 details the SMD format to be used (SMD's are to be used except where the device specification is a MIL-M-38510 device specification or an altered item drawing is required by the device specification or SMD) and data requirements to be submitted with any device procured under this specification. The QML certification mark shall not be used until the device specification is approved (see 3.6.3).

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3.6 Marking of microcircuits. Marking of QML microcircuits shall be in accordance with the following and the identification and marking provisions of the device specification or drawing. The marking shall be legible and complete. If any special marking (e.g., altered item drawing number) is used by the device supplier or user/equipment contractor, it shall be in addition to the existing/original marking as required herein and shall be visibly separate from and in no way interfere with the marking required herein. The following shall be placed on each microcircuit:

a. Index point (see 3.6.1).

b. Part or identification number (PIN) (see 3.6.2).

c. Certification mark "Q", or "QML" or “QD”: All Microcircuits acquired to, and meeting the requirements of this specification and the applicable SMD, device specification, or military temperature range data book parts, which are approved for supply under QML shall bear the "QML" or "Q" certification mark (see 3.6.3). For diminishing manufacturing sources (DMS) product using the alternate die/fabrication requirements of A.3.2.2 or other alternatives, the manufacturer shall use the “QD” certification mark in lieu of the “Q” or “QML” mark (see 3.6.3.1). The certification marks “Q", or "QML" or “QD” shall be visibly separate and distinct from all other markings on the microcircuits package.

d. Manufacturer's identification (see 3.6.4).

e. Country of origin (see 3.6.5).

f. Date code (see 3.6.6).

g. Special marking (see 3.6.7).

h. Serialization; when specified by the procuring activity, each microcircuit shall be marked with a unique serial number assigned within that inspection lot prior to the first recorded electrical measurement in screening.

i. Electrostatic discharge sensitivity identifier, if applicable (see 3.6.7.2).

NOTE: For unpackaged die only items b. through i. shall apply and be marked on the wafer or die carrier and any other container external to the wafer or die carrier. For tape automated bonded (TAB) (see appendix F) device marking shall be as defined in the procurement document.

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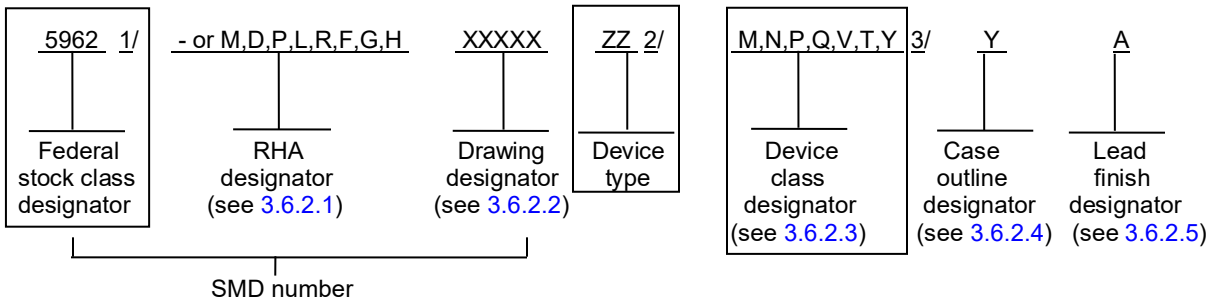
3.6.1 Index point. The index point, tab, or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified in the device specification and shall be designed so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline, or solid equilateral triangle(s), which are used as an electrostatic identifier (see 3.6.7.2), may also be used as the pin 1 identifier.

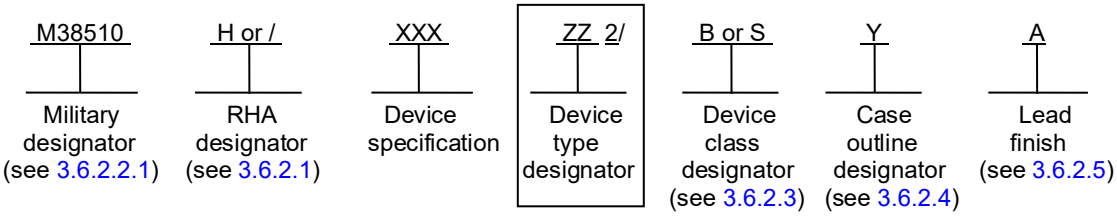
3.6.2 Part or identification number (PIN). Each QML microcircuit shall be marked with the complete PIN. The PIN may be marked on more than one line provided the PIN is continuous except where it "breaks" from one line to another. As of revision B of MIL-PRF-38535, several types of documents are acceptable for use when specifying QML microcircuits. They are MIL-M-38510 device specifications and SMD. The PIN marked on those parts under QML shall be the same as when supplied by the manufacturer prior to being listed on the QML-38535. The "Q" or "QML" designator combined with the listing of that PIN on a particular vendors QML listing shall indicate the fact that the manufacturer of the device is QML certified and qualified for the processes used to build that product. The PIN system shall be of one of the following forms, as applicable to the SMD or MIL-M-38510 device specification used for production:

a. SMD PINs shall be as follows:



For packages where marking of the entire SMD PIN and all other required topside markings are not possible due to space limitations, the manufacturer has the option of leaving the “5962-“ off the marking. The allowance for optional marking will be indicated in the individual SMD. For RHA product using this option, the RHA designator shall still be marked.

b. Device specification documents, originally published prior to 27 July 1990, shall be as follows:



All new PINs specified by new documents, originally published after 27 July 1990, shall be in accordance with the one part-one part number system.

All PINs specified by existing device specifications with the number assigned prior to 27 July 1990, may use either the original assigned PIN or the one part one-part number system with the first two digits in the drawing designator being "38" and the last three being the device specification number (e.g., M38510/00101BAC shall become 5962-3800101BAC).

1/ Drawings initiated prior to 1986 may not contain a federal stock class designator.
2/ Low dose rate sensitivity shall be indicated in the device specification for those devices that are susceptible to enhanced low dose rate sensitivity (ELDRS) effects. For device type series that are marked 61, 62, 63, and so forth, the designator shall indicate that the device has been characterized/tested for ELDRS and is ELDRS sensitive.
3/ Non one-part SMDs do not contain a device class designator. See MIL-HDBK-103 for qualification information. Prior MIL-M-38510 device specifications converted to SMDs shall contain a B or S class designator.

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3.6.2.1 RHA designator. A "- or /" indicates no radiation hardness assurance. Letters M, D, P, L, R, F, G, or H designations are defined RHA level in (rad(Si)) (see 3.4.3.).

3.6.2.2 Drawing designator. The first two characters of the designator shall consist of the last two digits of the year; the last three characters shall consist of unique characters assigned to the drawing by DLA Land and Maritime.

3.6.2.2.1 Military designator. The M38510 military designator for microcircuits means a "MIL" specification item produced in full compliance with this specification including qualification, and the device specification. Any device which does not meet all the requirements of this specification and the device specification shall not be marked M38510 and shall not make reference to MIL-PRF-38535.

NOTE: The military designator is optional for leadless chip carrier outlines that have a surface area smaller than the C-10 package.

3.6.2.3 Device class designator. The device class shall be designated by a single letter identifying the quality assurance level. For example:

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
MIL-PRF-38535 SMDs	5962-XXXXXZZ(M, N, P, Q, V, Y, T (B or S))YY (see 6.4.27 through 6.4.35)	QML-38535	MIL-HDBK-103
1.2.1 of MIL-STD-883 SMDs	5962-XXXXXZZ(M)YY (see 6.4.27 through 6.4.33)	MIL-HDBK-103	MIL-HDBK-103

3.6.2.4 Case outline. The case outline shall be designated by a single letter assigned to each outline within each device specification.

3.6.2.5 Lead finish. The lead finish (see A.3.5.6.3.2) shall be designated by a single letter as follows:

Finish letter	Process
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
D	Palladium
E	Gold flash palladium
F	Tin-lead alloy (BGA/CGA package) as defined in the applicable device document.
X	Either A, B, or C (mark on specification only)

NOTE: Lead finishes D and E are equivalent, and one may be substituted for the other, at the manufacturer's option.

3.6.3 Certification mark. All microcircuits acquired to and meeting the requirements of this specification and the applicable SMD, device specification, or military temperature range data book parts, which are approved for supply under QML, shall bear the "QML" or "Q" certification mark. The certification marks "Q", or "QML" shall be visibly separate and distinct from all other markings on microcircuits package.

3.6.3.1 "QD" certification mark. QML manufacturers shall request QA approval for diminishing manufacturing sources (DMS) product using the alternate die/fabrication requirements of A.3.2.2 or other alternatives. Upon approval the manufacturer shall use the "QD" certification mark in lieu of the "Q" or "QML" mark. The certification mark "QD" shall be visibly separate and distinct from all other markings on microcircuits package.

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3.6.3.2 "JAN" or "J" mark. The "J" marking is a legacy certification mark that was required by MIL-M-38510 device specifications and qualified on a QPL part by part basis. Since the "J" is often mistakenly considered part of the PIN, it may continue to be marked in front of the military designator portion of the device specification part number at the QML vendor's option. This "J" was not and shall not be considered an element of the official part number used to assign a national stock number.

3.6.4 Manufacturer's identification. Microcircuits shall, as a minimum, identify the manufacturer by the marking of name or trademark of the manufacturer or the manufacturer may also mark the manufacturer's Commercial and Government Entity (CAGE) code. The identification of the equipment manufacturer may appear on the microcircuit only if the equipment manufacturer is also the microcircuit manufacturer. If the microcircuit manufacturer's designating symbol or CAGE code number is marked, it shall be as assigned by the Defense Logistics Information Service (DLIS). The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small microcircuits, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

3.6.4.1 Code for assembly sites. If the manufacturer has more than one facility for assembly in a given country, a unique single letter code shall be assigned for the assembly sites used. This code shall be marked on the device immediately preceding or immediately after the date code. The assembly codes and the full address shall be included in the QML.

3.6.5 Country of origin. The name of the country of assembly or an appropriate abbreviation shall be marked in small characters below or adjacent to the other marking specified. Backside marking of the country of origin information is permitted.

3.6.6 Date code. Microcircuits shall be marked with a unique code to identify the first or the last week of the period (6 weeks maximum) during which devices in that inspection lot were sealed. The first two numbers in the code shall be the last two digits of the number of the year, and the third and fourth numbers shall be two digits indicating the calendar week of the year.

3.6.7 Marking location and sequence. The QML certification mark, the PIN, the date code, and ESD identifier, if applicable (see 3.6.7.2), shall be located on the top surface of leadless or leaded chip carriers, pin grid array packages, flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations). When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the backside of the package may be used for these markings except the ESD identifier, if applicable, which shall be marked on the top. Button cap flat packs with less than or equal to 16 leads may have the identifier marked on the ceramic. Backside marking with conductive or resistive ink shall be prohibited. For unpackaged die, marking is to be located on the container.

3.6.7.1 Beryllium oxide package identifier. If a microcircuit package contains beryllium oxide, the part shall be marked with the designation "BeO".

3.6.7.2 Electrostatic discharge (ESD) sensitivity identifier. Individual microcircuit ESD classification marking is optional. The manufacturer shall have an option of no ESD marking, marking a single ESD triangle symbol or marking in accordance with the ESD device classification defined in test method TM 3015 of MIL-STD-883 (ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) or ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) ESD marking is optional). Because it may no longer be possible to determine the ESD classification from the part marking, the device discharge sensitivity classification shall have to be obtained through MIL-HDBK-103 or QML-38535 or DLA Land and Maritime standard microcircuit cross reference website. If manufacturer is using the HBM or CDM or both method for ESD classification, it shall be reported in the device specification or standard microcircuit drawing (SMD) devices certificate of compliance (CofC).

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3.6.8 QML marked product. For QML certified and qualified manufacturers and manufacturers who have been granted transitional certification (see H.3.3), standard product (Joint Army Navy (JAN), class M SMDs, and military temperature range class B data book product), produced on a QML flow may be marked with the "Q" or "QML" certification mark. This allowance applies to contractor prepared drawings covering standard product only if the drawing was released prior to 31 December 1993 or the date the manufacturer becomes QML whichever is the later date, and the part is marked with the standard part number. A list of the manufacturer's military temperature range product to be included under QML shall be submitted to the QA for approval. Contractor prepared drawings written for nonstandard parts may not be marked with a "Q" or "QML". The only exception to this requirement is an altered item drawing required by a device specification or SMD.

Only parts covered by a MIL-M-38510 device specification, an SMD, or generic parts that have been grandfathered (a list of eligible devices shall be submitted to DLA Land and Maritime-VA or DLA Land and Maritime-VQ for review) shall be listed on QML-38535. After 31 December 93, new QML products, which are marked with a "Q" or "QML" certification mark, shall be documented on an SMD (see 3.5). Any device that is not processed in compliance with the provisions of MIL-PRF-38535 shall not be claimed to be compliant. Non-compliant products shall not contain “QML”, “QML V”, “QML Y” or any variant thereof within the vendor part number or within any marking located on the package.

3.6.9 Marking on container. All of the markings specified in 3.6, except the index point, shall appear on the die container/package (e.g., waffle pack, etc.), carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. For ESD sensitive devices, an industry standard symbol used to identify ESD sensitivity (e.g., JESD471 symbol) shall be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carriers, or both, then the ESD marking only (MIL-STD-1285) shall be required on the multiple carriers. These requirements apply to the original or repackaged QML microcircuits by the manufacturer or distributor.

3.7 Remarking. QML microcircuits may be remarked provided that all remarking procedures are approved by the TRB. Remarking shall be in accordance with 3.6 herein.

3.8 Screening and test. All microcircuits delivered in accordance with this specification shall meet the screening and testing requirements of 4.2 herein whether or not the actual testing has been performed.

3.9 Technology conformance inspection (TCI). All microcircuits delivered in accordance with this specification shall meet the TCI requirements of 4.3 herein whether or not the actual testing has been performed.

3.9.1 TCI assessment. In the event the TRB determines that the TCI requirements are not met, the TRB shall notify the Qualifying Activity (QA) immediately, a list of the product shall be generated by the TRB, and the qualifying activity shall be notified of the decision.

3.10 Solderability. All parts shall be capable of passing the solderability test in accordance with TM 2003 of MIL-STD-883, on delivery.

3.11 Traceability. Traceability to the wafer lot level (for GaAs to wafer level) shall be provided for all delivered microcircuits. Traceability includes, as a minimum, the completion of each step required in design (when applicable), fabrication, assembly, test and any applicable qualified rework procedure.

3.12 ESD control program. ESD protection, control, grounding procedures and training programs are very important key points to mitigate ESD damage at the microcircuits manufacturing and testing process. QML microcircuits manufacturers/suppliers shall establish an ESD mitigation program to safeguard against discharge damage at all wafer fabrication, wafer bumping, wafer scribing, coring services, automatic handling equipment’s, assembly facilities, testing station, packaging and handing of dice and devices in accordance with JESD625 or ANSI/ESDA S20.20. The established ESD control program documentation shall be under document control and TRB shall review and inspect periodically.

3.13 Recycled, recovered, environmentally preferable or biobased materials. Recycled, recovered, environmentally preferable or biobased materials should be used to the maximum extent possible provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.14 Alternate test requirements. The manufacturer shall follow the test method requirements per MIL-PRF-38535 or TM

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5004/5005 of MIL-STD-883. Upon approval from QA, as an option the manufacturer may follow TM 5004/5005 of MIL-STD-883 versus MIL-PRF-38535 test method. The manufacturer shall not be allowed to switch back and forth between TM 5004/5005 of MIL-STD-883 and MIL-PRF-38535 test method.

3.15 Passive elements. Passive elements are restricted to capacitors. Passive elements that are internally or externally utilized as an integral part of QML microcircuits shall meet the requirements of the following subparagraph. The microcircuits utilizing these passive elements shall be manufactured, processed, and verified to meet the requirements of this specification. The use of passive elements shall be documented on the applicable device specification SMD and shall include, but not be limited to, the type of element, the value and ratings of the element, the governing specification for the element, and other information necessary to positively identify the element.

3.15.1 Capacitors. Discrete capacitors, that are included as integral parts of the microcircuit design shall be used to improve the microcircuit performance in areas of decoupling, signal conditioning, or noise conditioning and radiation hardened assurance performance. Discrete capacitors that are internally or externally utilized as part of QML microcircuits shall meet one of the following requirements:

(i) For class Q microcircuits, the capacitors shall either meet the requirements of MIL-PRF-55681 (“S” failure rate level) or be approved for use by the Qualifying Activity (QA).

(ii) For Precious Metal Electrode(PME) capacitors use in microcircuits: For class V, class Y or class P (class level S) microcircuits, the capacitors shall meet or exceed the requirements of MIL-PRF-123 or be approved for use by the qualifying activity.

(iii) For thin layer Base Metal Electrode(BME) or PME capacitors use in microcircuits: For class Q devices, the capacitors shall meet or exceed the requirements of MIL-PRF-32535 class M level capacitors. For class V, class Y, or class P (class level S) devices, the capacitors shall meet or exceed the requirements of MIL-PRF-32535 class T level capacitors or its associated slash sheet capacitors (see 6.4.50) or be approved for use by the qualifying activity. The microcircuit manufacturer shall document the requirements used concerning the capacitors in their QM plan and standard microcircuit drawing(SMD).

This shall include, but not be limited to, inspection, assembly including attach procedures, testing including final electrical and groups A, D, and E.

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4. VERIFICATION

4.1 Verification. A verification system shall be in place to verify the requirements of section 3 in accordance with appendix J. Any screen or TCI test prescribed herein may be reduced, modified, moved, or eliminated by the QML manufacturer provided the product is still capable of meeting the screening and TCI testing groups A, B, C, D, and E for the applicable detail specification as approved by the QA.

4.2 Screening. All QML integrated circuits shall meet the requirements of the screens specified in tables IA and IB herein of the specification whether or not the actual testing has been performed. The procedures and accept and reject criteria for the screens shall have been certified by the QA. With QA approval the requirements of test method 5004 of MIL-STD-883 may be substituted for the screening requirements herein. When using TM 5004, class Q shall meet the requirements of the class level B screening flow whether or not the actual testing has been performed and class V, class Y, and class P shall meet the requirements of the class level S screening flow and appendix B herein whether or not the actual testing has been performed. The manufacturer, through its TRB, shall identify which tests are applicable to guarantee the quality and reliability of the associated technology or end product (e.g., wafer or die product, packaged product, plastic, etc.). The manufacturer may elect to eliminate or modify a screen based on supporting data that indicates that for the QML technology, the change is justified (see J.3.12 herein). If such a change is implemented, the manufacturer is still responsible for providing product that meets all of the performance, quality, and reliability requirements herein.

4.2.1 Screening testing failures. Devices that fail any screening test shall be identified, segregated, or removed.

4.2.2 Screening resubmission criteria. When it has been established that a failure during screening tests is due to operator error or equipment failure and it has been established that the remaining QML microcircuits have not been damaged or degraded, the surviving microcircuits, may be resubmitted to the corrected screening test(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the percent defective allowable (PDA) calculation (when applicable). ESD failures shall be counted as rejects and shall not be attributed to equipment failure or operator error.

4.2.3 Electrostatic discharge (ESD) sensitivity. ESD sensitivity testing shall be performed in accordance with TM 3015 of MIL-STD-883 and the device specification. The testing procedure defined within ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) may be used as an option in lieu of TM 3015 for applicable devices (e.g. high pin count devices wherein parasitic charge may effect ESD failures). However, manufacturers shall document such ESD testing procedure in the QM plan that require QA approval. The reported ESD sensitivity classification levels shall be documented in the device specification (see 3.6.7.2). In addition, unless otherwise specified, Human Body Model (HBM) and Charge Device Model (CDM) tests shall be performed for initial qualification and product redesign as applicable. If manufacturer is using the HBM or CDM or both method for ESD classification, it shall be reported in the device specification or standard microcircuit drawing (SMD) devices certificate of compliance (CofC).

4.3 Technology conformance inspection (TCI). All product shipped shall be capable of passing TCI in accordance with tables II, III, IV, and V; for plastic packages see table IB herein. With QA approval when TM 5005 of MIL-STD-883 is used as a TCI option, class Q shall be capable of passing the class level B flow. Both class V and class Y shall be capable of passing the flow of class level S and Appendix B herein. When selecting the TM 5005 TCI option for class V and class Y, the group B end-point electricals shall be the same as the group C end-point electricals, unless otherwise specified in the acquisition document. TCI testing shall be accomplished by the manufacturer on a periodic basis to assure that the manufacturer's quality, reliability, and performance capabilities meet the requirements of the QM plan (see G.3.3). Where appropriate, as an option, in place of the fixed sample size (Acceptance number) the manufacturer may use the sample size series (SSS) plan of APPENDIX D.

4.4 Qualification inspection. Qualification inspection shall be performed in accordance with H.3.4.

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits.

Screening Tests	MIL-STD-883, test method (TM) and conditions				
	Hermetic classes		Non-hermetic classes		
	Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
1. Wafer lot acceptance test	QM plan (see H.3.2.1.4) 1/	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots)	QM plan (see H.3.2.1.4) 1/	QM plan (see H.3.2.1.4) 1/ or TM 5007 of MIL-STD-883 (all lots
2. Nondestructive bond pull (NDBP) test 2/		TM 2023	TM 2023		
3. Internal visual inspection 3/	TM 2010, condition B	TM 2010, condition A	TM 2010, condition A	TM 2010, condition B	TM 2010, condition A
4. Temperature cycling 4/	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum	TM 1010, condition C, 10 cycles minimum or Condition B, 15 cycles minimum	TM 1010, condition B, -55 to 125 °C 15 cycles minimum	TM 1010, condition B, -55 to 125 °C 15 cycles minimum

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

Screening Tests	MIL-STD-883, test method (TM) and conditions				
	Hermetic classes		Non-hermetic classes		
	Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
5. Constant acceleration 5/	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only	TM 2001, condition E (minimum), Y1 orientation only		
6. Visual inspection 6/	100%	100%	100%	100%	100%
7. Particle Impact Noise Detection (PIND) test 7/ 8/		TM 2020, test condition A on each device	TM 2020, test condition A on each device		
8. Serialization 9/	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)	In accordance with device specification (100%)
9. Pre burn-in (Interim) electrical parameters test 10/	In accordance with device specification 11/	In accordance with device specification 12/ 25/	In accordance with device specification 12/ 25/	In accordance with device specification. 11/	In accordance with device specification 12/ 25/
10. Burn-in test: 10/ 13/ 14/	TM 1015 160 hours at +125°C minimum	TM 1015 240 hours at 125°C, condition D 15/	TM 1015 240 hours at 125°C , condition D 15/	TM 1015 160 hours at 125°C ,	TM 1015 240 hours at 125°C , condition D 15/
11. Post burn-in (Interim) electrical parameters test 10/		In accordance with device specification 12/ 25/	In accordance with device specification 12/ 25/		In accordance with device specification 12/ 25/

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

Screening Tests	MIL-STD-883, test method (TM) and conditions				
	Hermetic classes		Non-hermetic classes		
	Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
12. Reverse bias burn-in test (Static burn-in) 13/ 14/ 16/		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum	TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum		TM 1015, Condition A or C; 144 hours at +125°C or 72 hours at +150°C minimum
13. Post burn-in (Interim-reverse bias) electrical parameters test 10/		In accordance with device specification 12/ 25/	In accordance with device specification 12/ 25/		In accordance with device specification 12/ 25/
14. Percent defective allowable (PDA) calculation 17/	5 percent PDA (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)	5 percent PDA (all lots)	5 percent PDA, 3 percent PDA for functional parameters at 25°C (all lots)
15. Final electrical tests 18/ (see table III) 1. Static test : 1. at 25°C 2. Maximum and Minimum operating temperature 2. Dynamic or functional test : 19/ (1) at 25°C (2) Maximum and Minimum operating temperature 3. Switching test : (1) at 25°C (2) Maximum and Minimum operated temperature	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test) 25/ 26/	In accordance with applicable device specification (see group A test) 25/ 26	In accordance with applicable device specification (see group A test)	In accordance with applicable device specification (see group A test) 25/ 26/

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

Screening Tests	MIL-STD-883, test method (TM) and conditions				
	Hermetic classes		Non-hermetic classes		
	Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
16. Seal test 20/ a. Fine leak b. Gross leak	TM 1014	TM 1014	Not applicable		
17. Radiographic (X-ray) and/or Acoustic Microscopy test 21/		X-ray: TM 2012, Two views; Acoustic Microscopy TM 2030	X-ray: TM 2012, Two views; Acoustic Microscopy TM 2030		X-ray: TM 2012
18. External visual inspection 22/ 23/	TM 2009	TM 2009	TM 2009	TM 2009	TM 2009
19. Qualification or quality conformance inspection / TCI test sample selection	24/	24/	24/	24/	24/

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

1/ Testing per manufacturer's QM plan. See paragraph H.3.2.1.4 of MIL-PRF-38535 or TM 5007 of MIL-STD-883.

2/ For flip chip packages Nondestructive bond pull (NDBP) test is not required.

3/ Unless otherwise specified, at the manufacturer's option for test samples selection of group B, bond strength test (method 5005) may be randomly selected prior to or following internal visual (method 5004), prior to sealing provided all other specification requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond failures shall be counted even if the bond would have failed internal visual exam), and unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. Test method 2010 applies in full except when method 5004, alternate 1 or alternate 2 (appendix A) is in effect (see 3.3 method 5004 of MIL-STD-883). For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used. For flip chip devices, both internal visual and Acoustic Microscopy inspection (such as prior to bump attach to die and after bump attach to substrate and underfill cured etc.) shall be performed in accordance with TM 2010 and TM 2030.

4/ For devices with solder terminations, Temperature cycling test may be performed without balls and columns upon approval of PIDTP and QM plan. For class Y devices with organic substrates, Condition B, -55 to +125 may be used.

5/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

6/ At the manufacturer's option, external visual inspection for catastrophic failures may be conducted after each of the thermal/mechanical screens, after the sequence or after seal test. Catastrophic failures are defined as missing leads, broken packages, or lids off.

7/ See paragraph A.4.6.3 of appendix A and paragraph B.4.1 of appendix B of MIL-PRF-38535. The PIND test may be performed in any sequence after temperature cycling test and prior to post burn-in (interim) electrical parameters test.

8/ For device without a cavity or for flip chip devices with underfill, PIND test is not applicable.

9/ Class V, class Y, or class P (class level S) devices shall be serialized prior to the first recorded electrical measurement in screening. Class Q (class level B) microcircuits shall be serialized if delta calculations or matching characteristics are a requirement of the device specification. Each microcircuit shall be assigned a unique serial number in order to trace the data back to an individual device within the inspection lot which shall, in turn, be traceable to the wafer lot from which the device originated.

10/ Interim (pre and post burn-in) electrical testing shall be performed when specified, to remove defective devices prior to further testing or to provide a basis for application of percent defective allowable (PDA) criteria when PDA is specified (Ref. test step 14: PDA calculation, and footnote 17 herein). If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or standard microcircuit drawing (SMD). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to the time and temperature effects of burn-in and the most effective in removing electrically defective devices.

11/ When specified in the applicable device specification, 100 percent of the devices shall be tested and the results recorded for those parameters requiring delta calculations.

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

12/ For class V, class Y and class P (class level S) microcircuit devices, delta measurements shall be performed pre-burn-in and post-burn-in interim electrical measurements shall be recorded and delta calculations shall be performed on 100 percent of devices. In lieu of delta measurements and calculation, equivalent statistical techniques may be used if approved by the Qualifying Activity. The specific delta parameters shall be as defined in the applicable device specification.

13/ Burn-in shall be performed on all QML microcircuits, except as modified in accordance with SMD section 4.2, or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the wafer lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be documented in the QM plan and shall be available to the acquiring and qualifying activities upon request. For devices with solder terminations, burn-in test may be performed before solder balls/columns have been attached to the packages.

14/ When test condition F of method 1015 for temperature accelerated screening is used for either burn-in or reverse bias burn-in , it shall be used for both. Also, when devices have aluminum/gold metallurgical systems (at either the die pad or package post), the constant acceleration test shall be performed after burn-in and before completion of the final electrical tests (e.g, to allow completion of time limited tests but that sufficient 100 percent electrical testing to verify continuity of all bonds is accomplished subsequent to constant acceleration).

15/ Where applicable(for new product families or new technology devices use JEDEC publication JEP163) , dynamic burn-in test shall be performed, and test condition F of method 1015 and temperature accelerated test requirement shall not apply. For class V, class Y, or class P (class level S), burn-in test shall be performed in accordance with TM 1015 of MIL-STD-883, on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the qualifying activities for dealing with lot failures.

16/ The reverse bias burn-in is a requirement only when specified in the applicable device specification and is recommended only for a certain MOS, linear or other microcircuits where surface sensitivity may be a concern. When reverse bias burn-in is not required, interim post burn-in electrical parameter measurements shall be omitted. The order of performing the burn-in test and the reverse bias burn-in test may be inverted. Static burn-in may be substituted for high temperature reverse bias burn-in based on device technology and must be approved by the QA. Moreover, burn-in time-temperature regression table I of TM 1015 of MIL-STD-883 can be used for determination of reverse bias burn-in time and temperature.

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

17/ The percent defective allowable (PDA) shall be 5 percent or one device, whichever is greater. This PDA shall be based, as a minimum, on failures from group A, subgroup 1 plus deltas (in all cases where delta parameters are specified) with the parameters, deltas and any additional subgroups (or subgroups tested in lieu of A-1) subject to the PDA as specified in the applicable device specification or drawing. If no device specification or drawing exists, subgroups tested shall at least meet those of the most similar device specification or Standard Microcircuit Drawing. In addition, for class V, class Y, or class P (class level S) the PDA shall be 3 percent (or one device, whichever is greater) based on failures from functional parameters measured at room temperature. For class level S screening where an additional reverse bias burn-in is required, the PDA shall be based on the results of both burn-in tests combined. The verified failures after burn-in divided by the total number of devices submitted in the lot or sublot for burn-in shall be used to determine the percent defective for that lot, or sublot and the lot or sublot shall be accepted or rejected based on the PDA for the applicable device class. Lots and sublots may be resubmitted for burn-in one time only and may be resubmitted only when the percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater (see A.4.6.1.1 and A.4.6.1.2 of MIL-PRF-38535). This test need not include all specified device parameters, but shall include those measurements that are most sensitive to and effective in removing electrically defective devices.

18/ Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of table III, group A, subgroups 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, and 11, unless otherwise specified in the device specification. For solder termination devices, ball grid array (BGA) packages electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package, and for column grid array (CGA) packages, electrical test shall be performed across the full military temperature range before attachment of the solder columns on the package. After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process.

19/ Functional tests shall be conducted at input test conditions as follows: $V_{IH} = V_{IH}(min) +20$ percent, -0 percent; $V_{IL} = V_{IL}(max) +0$ percent, -50 percent; as specified in the most similar military detail specification. Devices may be tested using any input voltage within this input voltage range but shall be guaranteed to $V_{IH}(min)$ and $V_{IL}(max)$.

CAUTION: To avoid test correlation problems, the test system noise (e.g., testers, handlers, etc.) should be verified to assure that $V_{IH}(min)$ and $V_{IL}(max)$ requirements are not violated at the device terminals.

20/ The fine and gross leak seal tests shall be performed separately or together, between constant acceleration and external visual inspection test. For class level S and class level B devices, all device lots (sublots) having any physical processing steps (e.g., lead shearing, lead forming, solder dipping to the glass seal, change of, or rework to, the lead finish, etc.) performed following seal or external visual inspection shall be retested for hermeticity and visual defects. This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method TM 1014) using an acceptance criteria of a quantity (accept number) of 116(0), and an external visual inspection (method TM 2009) on the entire inspection lot (sublot). For devices with leads that are not glass-sealed and that have a lead pitch less than or equal to 1.27 mm (0.050 inch), the sample seal test shall be performed using an acceptance criteria of a quantity (accept number) of 15(0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance. For class level S devices, with the approval of the qualifying activity, an additional room temperature electrical test may be performed subsequent to seal, but before external visual, if the devices are installed in individual carriers during electrical test.

21/ The radiographic and/or Acoustic Microscopy screening test may be performed in any sequence after serialization. Only one view is required for flat packages and leadless chip carriers having lead (terminal) metal on four sides. For flip chip technology, only Acoustic Microscopy inspection is required. Acoustic Microscopy inspection may be performed in any sequence after underfill cure for flip chip technology. For additional requirements for this test, see appendix B paragraph B.4.1 of MIL-PRF-38535.

22/ External visual inspection shall be performed on the lot any time after radiographic test and prior to shipment, and all shippable samples shall have external visual inspection at least subsequent to qualification or quality conformance inspection testing.

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TABLE IA. Screening procedure for hermetic classes Q, V and non-hermetic classes N, P, Y microcircuits. - Continued.

23/ The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the double sample also has one or more failures, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

24/ Samples shall be randomly selected from the assembled inspection lot for testing in accordance with the specific device class and lot requirements of Group A, B, C, D, E and applicable appendices of MIL-PRF-38535 or TM 5005 of MIL-STD-883; after the specified screen requirements herein table IA or TM 5004 have been satisfactorily completed.

25/ For class V, class Y and class P (class level S) microcircuit devices, all specified pre-burn-in and post burn-in interim tested electrical parameters shall be read and recorded on 100 percent of devices. Specified electrical parameters that cannot be read and recorded shall be identified in the SMD if approved by the Qualifying Activity. In lieu of 100% Read and Record data collection, testing may be performed that includes automatic removal of units that are outside the normal electrical distribution of the product (outlier devices) as determined by statistical techniques if approved by the Qualifying Activity.

26/ For class V, class Y and class P (class level S) microcircuit devices, the supplier shall perform some variant of part-average-testing (PAT) and/or statistical-bin-analysis (SBA) that meets the intent of the guideline. The supplier determines the sample sizes and acceptance criteria per the test methods (see JEDEC standard JESD50). If these tests are not possible for a given part, then the supplier shall provide justification to the Qualifying Activity. The PAT and/or SBA requirements may be performed in any sequence (e.g. at wafer sort and/or final test) in the screening flow.

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TABLE IB. Tests/monitors for plastic packages (certified prior to 01 May 2023). 1/ 3/

Test/monitor	MIL-STD-883 test method (TM) or industry standard
1. Wafer acceptance	TRB / QM plan (see H.3.2.1.4)
2. Internal visual	TM 2010 or in accordance with manufacturers internal procedures
3. Temperature cycling/thermal shock	TM 1010/TM 1011
4. Resistance to solvents	TM 2015
5. Bond strength	TM 2011
6. Ball shear	ASTM F1269
7. Solderability	TM 2003
8. Die shear or stud pull	TM 2019 or TM 2027
9. Steady-state life test End-point electricals	TM 1005 In accordance with device specification
10. Physical dimensions	TM 2016
11. Lead integrity	TM 2004
12. Inspection for delamination	e.g., TM 1034 (dye penetrant test), cross-sectioning, C-mode scanning acoustical microscopy (AM) TM 2030, etc.
13. Highly accelerated stress testing (HAST)	JESD22-A118, 100 hours, +130°C, 85% relative humidity (RH) 2/
14. Autoclave	JESD 22-A102 (no bias) 2 atm., +121°C
15. Salt atmosphere	TM 1009
16. Adhesion to lead finish	TM 2025
17. Interim pre burn-in electricals	In accordance with device specification
18. Burn-in test	TM 1015, 160 hours at +125°C or manufacturers QM plan
19. Interim post burn-in electricals	In accordance with device specification
20. PDA or alternate procedure for lot acceptance	1% PDA or manufacturer's QM plan
21. Final electrical tests (see table III, herein, for definition of subgroups) a. static test b. dynamic test c. functional test d. switching test	In accordance with device specification
22. External visual inspection test	TM 2009 or JESD22-B101 or manufacturers internal procedures

1/ Test methods (TMs) are listed herein to give the manufacturer an available method to use. Alternate procedures and test methods may be used. Monitor frequency and sample plan shall be in accordance with manufacturer's QM plan.
2/ An alternate process monitor may be used; e.g., +85°C/85% relative humidity (RH).

3/ The requirements of Table IB only apply to existing / legacy class N microcircuits with QML certification successfully completed prior to 01 May 2023, (implementation date of Rev M MIL-PRF-38535).

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TABLE II. Group B tests (Mechanical and environmental test)

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)					Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Hermetic classes		Non-hermetic classes				
	Class Q	Class V	Class Y (Ceramic or Organic)	Class N (PEM) (class level B)	Class P (PEM) (class level S)	Class level B	Class level S
Subgroup 1	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)	Resistance to solvents 2/ TM 2015 3(0)		a. Physical dimensions 3/ TM 2016 2(0) b. Internal gas analysis (IGA) test TM 1018 3(0) 3/ 4/ 5/ (5,000 ppm maximum water content at 100°C)

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TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)					Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Hermetic classes		Non-hermetic classes				
	Class Q	Class V	Class Y (Ceramic or Organic)	Class N (PEM) (class level B)	Class P (PEM) (class level S)	Class level B	Class level S
Subgroup 2 6/	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)	a. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)	a. Resistance to solvents 2/ TM 2015 3(0)	a. Resistance to solvents 2/ TM 2015 3(0) b. Internal visual and mechanical TM 2013, TM 2014 2(0) c. Bond strength 7/ TM 2011 22(0) (1) Thermo compression - Test condition C or D (2) Ultrasonic - Test condition C or D (3) Beam lead - Test condition H d. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)

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TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)					Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Hermetic classes		Non-hermetic classes				
	Class Q	Class V	Class Y (Ceramic or Organic)	Class N (PEM) (class level B)	Class P (PEM) (class level S)	Class level B	Class level S
Subgroup 3 sample size 22(0) (22 leads from 3 devices) 8/	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 Solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C	Solderability TM 2003 solder temperature +245°C ±5°C
Subgroup 4 sample size 45(0) 3/		For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)	For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package - TM 2038 (45 columns from 2 devices minimum)		For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package - TM 2038 (45 columns from 2 devices minimum)		a. Lead integrity TM 2004 9/ (Test condition B2, lead fatigue) b. Seal test TM 1014 as applicable (1) Fine leak (2) Gross leak c. Lid torque TM 2024 10/ as applicable d. For BGA/CGA packages: (i) Ball shear test for BGA package - JESD22-B117 (45 balls from 2 devices minimum) (ii) Solder column pull test for CGA package – TM 2038 (45 columns from 2 devices minimum)

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TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

Subgroups 1/	Group B tests for QML microcircuits (MIL-PRF-38535)					Group B tests for class level B and S microcircuits (TM 5005 of MIL-STD-883)	
	Hermetic classes		Non-hermetic classes				
	Class Q	Class V	Class Y (Ceramic or Organic)	Class N (PEM) (class level B)	Class P (PEM) (class level S)	Class level B	Class level S
Subgroup 5 6/						a. Bond strength TM 2011 15(0) 11/ (1) Thermo compression - Test condition C or D (2) Ultrasonic - condition C or D (4) Beam lead - condition H b. Die shear test or substrate attach strength or stud pull test including passive elements TM 2019 or TM 2027 3(0)	sample size 45(0) a. End-point electrical parameters 12/ - As specified in the applicable device specification b. Steady state life test 13/ TM 1005 Test condition C, D or E c. End-point electrical parameters 12/ - As specified in the applicable device specification
Subgroup 6 Sample size 15(0) 14/							a. Temperature cycling TM 1010, condition C, 100 cycles minimum b. Constant acceleration TM 2001, condition E, Y_1 orientation only c. Seal test TM 1014 (1) Fine leak (2) Gross leak d. End-point electrical parameters - As specified in the applicable device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

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TABLE II. Group B tests (Mechanical and environmental test) . – Continued.

1/ Electrical reject devices from the same inspection lot may be used for all subgroups when end-point measurements are not required provided that the rejects are processed identically to the inspection lot through pre burn-in electrical and provided the rejects are exposed to the full temperature/ time exposure of burn-in. Group B test shall be performed on each inspection lot as a condition for lot acceptance for delivery. Group B test shall be performed on each qualified package type and lead finish.

2/ Resistance to solvents testing required only on devices using inks or paints as a marking medium.

3/ Not required for qualification or quality conformance inspections where group D inspection is being performed on samples from the same inspection lot. For devices with solder terminations, Physical dimension test shall be performed with balls/columns.

4/ This test is required only, if it is a glass-frit-sealed package. Unless handling precautions for beryllium packages are available and followed TM 1018, procedure 3 shall be used (see group D, subgroup 6 of table V). For class Y non-hermetic microcircuits devices Internal gas analysis (IGA) test is not applicable.

5/ Test three devices; if one fail, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails, a second complete sample may be tested at an alternate laboratory that has been granted current suitability status by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity.

6/ For all devices, except flip chip, the die shear test or substrate attach strength or stud pull test including passive elements shall be performed per TM 2019 or TM 2027, as applicable. For flip chip devices, TM 2019 die shear strength, TM 2027 substrate attach strength, or TM 2031 flip chip pull-off tests are not recommended. Failure mode for flip chip is complete destruction of the die or exceeding tool maximum limits, thus the test does not add value. Electrical test and radiography (X-ray) or Acoustic Microscopy will validate adhesion of flip chip die. If the flip chip device uses passive elements the substrate attach strength or stud pull test shall also be performed on the passive elements per TM 2019 or TM 2027. For solder termination devices, subgroup 2 test may be performed without balls and columns attached.

7/ Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition H is the number of dice (not bonds) (see TM 2011).

8/ All devices submitted for solderability test shall be in the lead finish that will be on the shipped product and which has been through the temperature/time exposure of burn-in except for devices which have been hot solder dipped or undergone tin-lead fusing after burn-in. The sample size number applies to the number of leads inspected except in no case shall less than 3 (three) devices be used to provide the number of leads required. For BGA/CGA packages, solderability test shall be verified after solder ball or solder column attachment processes per TM 2003. For CGA packages, solder temperature shall be maintained in accordance with table 1 of TM 2003.

9/ The sample size number of 45 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test and lid torque test, if applicable, (see 10/) in order to meet the requirements of subgroup 4. For pin grid array leads and rigid leads, use TM 2028. For leaded chip carrier packages, use condition B1. For leadless chip carrier packages only, use test condition D and a sample size number of 15 based on the number of pads tested taken from 3 devices minimum. Seal test (subgroup 4b) need to be performed only on packages having leads exiting through a glass seal. For LGA/BGA/CGA packages, TM 2004 does not apply.

10/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

11/ Test samples for bond strength may, at the manufacturer's option, unless otherwise specified, be randomly selected prior to or following internal visual (PRESEAL) inspection specified in table IA herein or TM 5004, prior to sealing provided all other specifications requirements are satisfied (e.g., bond strength requirements shall apply to each inspection lot, bond strength samples shall be counted even if the bond would have failed internal visual exam). Unless otherwise specified, the sample size number for condition C or D is the number of bond pulls selected from a minimum number of 4 devices, and for condition F or H is the number of dice (not bonds) (see TM 2011).

12/ Read and record group A subgroups 1, 2 and 3.

13/ The alternate removal-of-bias provisions of 3.3.1 of TM 1005 shall not apply for test temperature above 125°C.

14/ For devices with solder terminations, Temperature cycling and Constant acceleration test may be performed without balls/columns attachment.

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TABLE III. Group A (electrical tests) . 1/

Subgroups	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.) 2/ 3/ 4/ 5/				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V 6/ (class level S)	Class Y 6/ (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P 6/ (PEM) (class level S)
1 2 3	Static tests at +25°C Static tests at maximum rated operating temperature Static tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
4 5 6	Dynamic tests at +25°C Dynamic tests at maximum rated operating temperature Dynamic tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
7 8A 8B	Functional tests at +25°C Functional tests at maximum rated operating temperature Functional tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample
9 10 11	Switching tests at +25°C Switching tests at maximum rated operating temperature Switching tests at minimum rated operating temperature	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample	116(0) or 100 percent/ 0 sample

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TABLE III. Group A (electrical tests) . 1/

1/ The specific parameters to be included for tests in each subgroup shall be as specified in the applicable acquisition document. Where no parameters have been identified in a particular subgroup or test within a subgroup, no group A testing is required for that subgroup or test to satisfy group A requirements.

2/ At the manufacturer's option, the applicable tests required for group A testing (see 1/ herein) may be conducted individually or combined into sets of tests, subgroups (as defined in table III), or sets of subgroups. However, the manufacturer shall pre-designate these groupings prior to group A testing. Unless otherwise specified, the individual tests, subgroups, or sets of tests/subgroups may be performed in any sequence.

3/ The sample plan (quantity and accept number) for each test, subgroup, or set of tests/subgroups as pre-designated in 2/ herein, shall be 116/0.

4/ A greater sample size may be used at the manufacturer's option; however, the accept number shall remain at zero. When the (sub)lot size is less than the required sample size, each and every device in the (sub)lot shall be inspected and all failed devices removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For those lots having a quantity of less than 116 devices, the test shall be imposed on a 100 percent basis with zero failure.

5/ If any device in the sample fails any parameter in the test, subgroup, or set of tests/subgroups being sampled, each and every additional device in the (sub)lot represented by the sample shall be tested on the same test set-up for all parameters in that test, subgroup, or set of tests/subgroups for which the sample was selected, and all failed devices shall be removed from the (sub)lot for final acceptance of that test, subgroup, or set of tests/subgroups, as applicable. For device class V, class Y, or class P (class level S), if the testing results in a percent defective allowable (PDA) greater than 5 percent, the (sub)lot shall be rejected, except that for (sub)lots previously unscreened to the tests that caused failure of this percent defective, the (sub)lot may be accepted by resubmission and passing the failed individual tests, subgroups, or set of tests/subgroups, as applicable, using a 116/0 sample.

6/ For class V, class P and class Y, group A electrical tests additional requirements see paragraph B.4.3 appendix B of MIL-PRF-38535.

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TABLE IV. Group C life tests .

Subgroup	Tests	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B) 1/	Class V (class level S) 1/ 2/	Class Y (ceramic or organic (class level S) 1/ 2/	Class N (PEM) (class level B) 1/	Class P (PEM) (class level S) 1/ 2/
Subgroup 1	a. Steady-state life test	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C	a. TM 1005 45(0) 1000 hours at 125°C
	b. End-point electrical parameters	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification	b. As specified in the applicable device procurement specification

1/ Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3-months period.

2/ Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV herein. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

(a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

(b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

(c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

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TABLE V. Group D tests (Package related test) .

Subgroups	Test 1/	MIL-STD-883 test method and conditions				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 1 sample size 15(0) 2/	Physical dimensions	TM 2016	TM 2016	TM 2016	TM 2016	TM 2016
Subgroup 2 sample size 45(0) 2/ 3/	a. Lead/terminal integrity test	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style	Where applicable a. TM 2004 condition B2 (lead fatigue) or applicable for the package technology style
	b. Seal test 4/ (1) Fine leak (2) Gross leak	b. TM 1014 Test condition as applicable	b. TM 1014 Test condition as applicable	b. 5/	b. 5/	b. 5/
	c. For BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages	c. BGA/CGA packages
	(i) Ball shear test for BGA package	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)	(i) For BGA package - JESD22-B117 (45 balls from 2 devices minimum)
	(ii) Solder column pull test for CGA package	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)	(ii) For CGA package - TM 2038 (45 columns from 2 devices minimum)

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TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 3 sample size 15(0) 6/ 7/ 17/	a. Thermal shock	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum	a. TM 1011 Test condition B, 15 cycles minimum (Ceramic class Y only)	a. 5/	a. 5/
	b. Temperature cycling	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum	b. TM 1010 Test condition C, 100 cycles minimum or condition B 150 cycles	b. i) Acoustic Microscopy 18/ ii) TM1010 Condition B (150 cycles min) iii) Acoustic Microscopy	b. i) Acoustic Microscopy 18/ ii) TM1010 Condition B (150 cycles min) iii) Acoustic Microscopy
	c. Moisture resistance	c. TM 1004 8/	c. TM 1004 8/	c. JESD22-A118 Unbiased HAST condition B	c. JESD22-A118 Unbiased HAST Condition B and/or (JESD22-A110) Biased HAST Condition B 18/	c. JESD22-A118 Unbiased HAST Condition B and/or (JESD22-A110) Biased HAST Condition B 18/
	d. Visual examination	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010	d. In accordance with visual criteria of TM 1004 or TM 1010
	e. Seal test 9/ (1) Fine leak (2) Gross leak	e. TM 1014 test condition as applicable	e. TM 1014 test condition as applicable	e. 5/	e. 5/	e. 5/
	f. End-point electrical parameters 10/	f. As specified in the applicable device	f. As specified in the applicable device	f. As specified in the applicable device	f. As specified in applicable device.	f. As specified in applicable device.

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TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 4 sample size 15(0) 6/ 7/	a. Mechanical shock b. Vibration, variable frequency c. Constant acceleration 11/ d. Seal test (1) Fine leak (2) Gross leak e. Visual examination f. End-point electrical parameters	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. TM 1014 condition as applicable e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	a. TM 2002 condition B minimum b. TM 2007 condition A minimum c. TM 2001 Test condition E, Y1 orientation only d. TM 1014 condition as applicable e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	a.TM 2002 condition B minimum b.TM 2007 condition A minimum c.TM 2001 Test condition E, Y1 orientation only d. 5/ e. In accordance with visual criteria of TM 2007 f. As specified in the applicable device specification	5/	5/

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TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 5 sample size 15(0) 2/	a. Salt atmosphere b. Visual examination c. Seal 9/ (1) Fine leak (2) Gross leak	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. TM 1014 condition as applicable	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. TM 1014 condition as applicable	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. 5/	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. 5/	a. TM 1009 Test condition A minimum b. In accordance with visual criteria of TM 1009 c. 5/
Subgroup 6 2/ 12/	Internal gas analysis (IGA) test (cavity packages)	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	TM 1018 3(0) 5,000 ppm maximum water content at 100°C	5/	5/	5/
Subgroup 7 sample size 15(0) 2/ 13/ 14/	Adhesion of lead finish	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025	Where applicable TM 2025
Subgroup 8 sample size 5(0) 2/	Lid torque 15/	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024	Where applicable TM 2024

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TABLE V. Group D tests (Package related test) . - Continued.

Subgroups	Test 1/	MIL-STD-883 test method and conditions				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 9 sample size 3(0) (3 leads minimum) 16/	a. Soldering heat b. Seal (1) Fine leak (2) Gross leak c. External Visual examination d. End-point electrical	Where applicable a. TM 2036 b. TM 1014 condition as applicable c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. TM 1014 condition as applicable c. TM 2009 d. As specified in the applicable device specification	Where applicable a. TM 2036 b. 5/ c. TM 2009 d. As specified in the applicable device specification	5/	5/

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

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TABLE V. Group D tests (Package related test) . - Continued.

1/ In-line monitor data may be substituted for subgroups D1, D2, D6, D7, and D8 upon approval by the qualifying activity. The monitors shall be performed by package type and to the specified subgroup test method(s). The monitor sample shall be taken at a point where no further parameter change occurs, using a sample size and frequency of equal or greater severity than specified in the particular subgroup. The in-line monitor data shall be traceable to the specific inspection lot(s) represented (accepted or rejected) by the data.

2/ Electrical reject devices from that same inspection lot may be used for samples. For devices with solder terminations, subgroups 1, 2, 5 and 8 tests shall be performed with balls and columns. For Subgroup 1 and 5, BGA/CGA packages may test 12 samples without balls/columns at land grid array (LGA) level and 3 samples with balls/columns.

3/ The sample size number of 45, C = 0 for lead integrity shall be based on the number of leads or terminals tested and shall be taken from a minimum of 3 devices. All devices required for the lead integrity test shall pass the seal test if applicable (see 4/) in order to meet the requirements of subgroup 2. For leaded chip carrier packages, use condition B1. For pin grid array leads and rigid leads, use TM 2028. For leadless chip carrier packages only, use test condition D and a sample size number of 15 (C = 0) based on the number of pads tested taken from 3 devices minimum. For LGA/BGA/CGA packages, TM 2004 does not apply.

4/ Seal test (subgroup 2b) need be performed only on packages having leads exiting through a glass seal.

5/ This test is not applicable for class N, P, and Y non-hermetic microcircuits devices.

6/ Devices used in subgroup 3, "Thermal and Moisture Resistance" may be used in subgroup 4, "Mechanical".

7/ For devices with solder terminations, subgroups 3 and 4 tests may be performed without balls and columns. For class Y devices with organic substrates, Condition B, -55 to +125 may be used.

8/ Lead bend stress initial conditioning is not required for leadless chip carrier packages or BGA/CGA packages. For fine pitch packages (≤ 25 mil pitch) using a nonconductive tie bar, preconditioning shall be required on 3 devices only prior to the moisture resistance test with no subsequent electrical test required on these 3 devices. The remaining 12 devices from the sample of 15 devices do not require preconditioning but shall be subjected to the required endpoint electrical tests.

9/ After completion of the required visual examinations and prior to submittal to TM 1014 seal tests, the devices may have the corrosion by-products removed by using a bristle brush.

10/ At the manufacturer's option, end-point electrical parameters may be performed after moisture resistance and prior to seal test.

11/ All microcircuits shall be subjected to constant acceleration. For microcircuits which are contained in packages that have an inner seal or cavity perimeter of 2 inches or more in total length or have a package mass of 5 grams or more may be tested by replacing test condition E with condition D or with test conditions as specified in the applicable device specification. Unless otherwise specified in the acquisition document, the stress level for large, monolithic microcircuit packages shall not be reduced below test condition D. If the stress level specified is below condition D, the manufacturer must have data to justify this reduction and this deviation shall be specified in the QM plan, and data available for review by the preparing or acquiring activity. The minimum stress level allowed in this case is condition A. For flip chip devices, Constant acceleration test is not required.

12/ Test three devices; if one fails, test two additional devices with no failures. At the manufacturer's option, if the initial test sample fails a second complete sample may be tested at an alternate laboratory that has been issued suitability by the qualifying activity. If this sample passes, the lot shall be accepted provided the test data from both submissions is submitted to the qualifying activity.

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TABLE V. Group D tests (Package related test) . - Continued.

13/ The adhesion of lead finish test shall not apply for leadless chip carrier, land grid array (LGA), ball grid array (BGA), and column grid array (CGA) packages.

14/ Sample size number 15 leads from 3 devices minimum are based on number of leads with zero failure.

15/ Lid torque test shall apply only to packages which use a glass-frit-seal to lead frame, lead or package body (e.g., wherever frit seal establishes hermeticity or package integrity). Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures for lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

16/ This test is performed at qualification/re-qualification of design changes which may affect this test. The manufacturer shall determine, for each package, the applicable conditions from TM 2036 that are appropriate for the mounting conditions, and assure by testing, or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

17/ Preconditioning shall be performed on surface mount devices in accordance with JESD22-A113, prior to subgroup 3 test for non hermetic device classes N, P, and Y with organic substrates. Manufacturer may perform these test sequentially or in parallel (separate samples for 3b and 3c) in accordance to the manufacturers QM plan. Thermal shock is not applicable to class N, P, and organic class Y.

18/ Applicability of this test to be determined by the manufacturers TRB and documented to the QM plan.

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5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of material is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service of Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit application and logistic purposes. For maximum cost effectiveness while maintaining essential quality and reliability requirements, it is recommended that, for initial acquisitions for original equipment complements, the device class appropriate to the need of the application be acquired.

6.1.1 Class T. As the requirements for class level T are specified in the manufacturer's Quality Management (QM) plan for each technology, the user is cautioned to review the manufacturer's QM plan to assure that the part being acquired meets the requirements/reliability of the system application. Class T is not for use in NASA manned, satellite, or launch vehicle programs without written permission from the applicable NASA Project Office (e.g., cognizant EEE parts authority).

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identification (if applicable).

c. Packaging requirements (see 5.1).

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturer's List, QML-38535, whether or not such manufacturers have actually been listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: DLA Land and Maritime-VQ, P.O. Box 3990, Columbus, Ohio 43218-3990.

6.4 Terms and definitions. For the purpose of this specification, the terms, and definitions of MIL-STD-883 and MIL-HDBK-1331, and those contained herein apply and should be used in the applicable device specifications wherever they are pertinent.

6.4.1 Microelectronics. The area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

6.4.2 Element (of a microcircuit or integrated circuit). A constituent of the microcircuit, or integrated circuit, that contributes directly to its operation. (e.g., A discrete part incorporated into a microcircuit becomes an element of the microcircuit.)

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6.4.3 Substrate (of a microcircuit or integrated circuit). The supporting material upon, or within which, the elements of a microcircuit or integrated circuit are fabricated or attached.

6.4.4 Integrated circuit (microcircuit). Integrated circuit (microcircuit). A die with a high equivalent circuit element density, composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (e.g., this excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.)

6.4.4.1 Multichip microcircuit or multichip module (MCM). An integrated circuit or microcircuit consisting of two or more die which are attached to a substrate or package and meets all applicable requirements of section 3.4.

6.4.4.2 Monolithic microcircuit. An integrated circuit or microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

6.4.5 Production lot. A production lot of devices manufactured on the same production line(s) (QM technology flow) by means of the same production technique, materials, controls, and design.

6.4.6 Inspection lot. A quantity of integrated circuits submitted at one time for inspection to determine compliance with the requirements and acceptance criteria of the applicable device specification. Each inspection lot is to be manufactured on the same production line through final seal by the same production techniques.

6.4.7 Wafer lot. A wafer lot consists of integrated circuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group, and assigned a unique identifier or code to provide traceability.

6.4.8 Percent defective allowable (PDA). PDA is the maximum observed percent defective which permits the lot to be accepted after the specified 100 percent test.

6.4.9 Delta limit. The maximum change in a specified parameter reading that will permit a device to be accepted on the specified test, based on a comparison of the present measurement with a specified previous measurement.

NOTE: When expressed as a percentage value, it should be calculated as a proportion of the previous measured value.

6.4.10 Rework. Any processing or reprocessing operation documented in accordance with the manufacturer's QM plan, other than testing, applied to an individual device, or part thereof, and performed subsequent to the prescribed non-repairing manufacturing operations which are applicable to all devices of that type at that stage.

6.4.11 Final seal. The manufacturing operation that completes the enclosure of a device so that further internal processing cannot be performed without disassembling the device.

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6.4.12 Acquiring activity. The organizational element which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity does not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has been given by the organization (e.g., preparing activity, qualifying activity).

6.4.13 Qualifying activity (QA). The organizational element of the Government that grants certification and qualification for the specific technology flow in accordance with this specification.

6.4.14 Parts per million (PPM). Parts per million is as defined in EIA-557.

6.4.15 Device type. The term device type refers to a single specific microcircuit configuration.

6.4.16 Die type. A microcircuit manufactured using the same physical size, materials, topology, mask set, process flow, on a single fabrication line.

6.4.17 Radiation hardness assurance (RHA). The portion of product assurance that assures that parts continue to perform as specified or degrade in a specified manner when subjected to the specified radiation environmental stress. The radiation hardness assurance capability level (RHACL) is the radiation level that the manufacturer chooses for each radiation environment appropriate to his technology as a consistently achievable exposure level that does not cause degradation in the microcircuit beyond the specified level of performance.

6.4.18 Electrostatic discharge (ESD) sensitivity . ESD sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESD classification testing and is used as the basis for assigning an ESD class.

6.4.19 Package family. A group of package types with identical configuration and process techniques (e.g., cerdip, side braze, cerpack).

6.4.20 Technology flow. A technology flow is that specific manufacturing line from design, fabrication, assembly, packaging, and test in a given technology from which a manufacturer designs, builds, and tests integrated circuits. Once a manufacturer's technology flow has been certified and qualified by the QA, it is listed on the QML.

6.4.21 Qualified Manufacturer's Listing (QML). The QML is a listing of the manufacturers and their parts which utilize a certified and qualified technology flow.

6.4.22 Third party design center. A subcontract design center, or an original equipment manufacturer (OEM) design center, that uses a microcircuit manufacturer's design tools (including approved industry/third party tools), interface procedures, design rules, and design controls.

6.4.23 Radiation source of supply (RSS). A company (e.g., original equipment manufacturer (OEM)) who establishes a relationship with a device manufacturer for the sole purpose of developing qualified RHA product and has the responsibility to incur the radiation response of said product to the requirements of MIL-PRF-38535, the applicable detail specification, and the RSS program plan. The RSS will be listed in the QML for those devices covered by the RSS's QML. All requests for this product will be submitted through the RSS.

6.4.24 Form. The shape, size, dimension, mass, weight, and other visual parameters which uniquely characterize an item. For software, form denotes the language and media.

6.4.25 Fit. The ability of an item to physically interface, or interconnect with, or become an integral part of another item.

6.4.26 Function. The action or actions that an item is designed to perform.

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6.4.27 Class M. Items which have been subjected to and passed all applicable requirements of appendix A herein and are documented on an SMD. This product is intended for military applications.

6.4.28 Class N. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections, and are encapsulated in plastic. This product must be assessed by the user to determine if it is appropriate for use in users' application.

6.4.29 Class Q. Items which have been subjected to and passed all applicable requirements of this specification and applicable appendices including qualification testing, screening testing, and TCI/QCI inspections.

6.4.30 Class V. Items that meet all the class Q requirements, and have been subjected to, and passed all applicable requirements of appendix B herein.

6.4.31 Class Y. A microcircuit employing a non-hermetic package, which meets all applicable requirements of this specification including qualification, screening and TCI/QCI requirements, and all applicable requirements of Appendix B herein.

6.4.32 Class B. Items which have been subjected to and passed all applicable requirements of this specification including qualification testing, screening testing, and TCI/QCI inspections and are documented on a MIL-M-38510 specification sheet.

6.4.33 Class S. Items that meet all the class B requirements, and have been subjected to, and passed, all applicable requirements of appendix B herein and are documented on a MIL-M-38510 specification sheet.

6.4.34 Class T. Class T is a quality level whose requirements are defined by 3.4.8 herein and as documented on an SMD. Class T is not for use in NASA manned, satellite, or launch vehicle programs without written permission from the applicable NASA Project Office (e.g., cognizant EEE parts authority).

6.4.35 Class P. A non-hermetic Plastic Encapsulated Microcircuit (PEM), which meets all applicable requirements of this specification including qualification, screening and TCI/QCI inspections, and all applicable requirements of Appendix B herein. This product must be assessed by the user to determine if it is appropriate for use in users' system application.

6.4.36 Qualified manufacturer's line. The specified line, which is the certified and qualified technology flow, of a manufacturer from which QML integrated circuits may be purchased.

6.4.37 Test optimization. The process used by the manufacturer to optimize testing utilizing the best commercial practices available while still assuring all applicable performance, quality, and reliability requirements are met. Any screen or TCI test prescribed herein may be reduced, modified, moved, or eliminated by the QML manufacturer provided the product is still capable of meeting the screening and TCI testing groups A, B, C, D, and E for the applicable detail specification as approved by the QA.

6.4.38 Audit team. The audit team will be led by DLA Land and Maritime personnel and comprised of government representatives (e.g., NASA, NRO, ARMY, NAVY, USAF and DTRA) as designated by the qualifying activity.

6.4.39 Class level B. Class level B requirements contained in this document define the requirements for class Q and class B, including SMDs and M38510 JAN slash sheet product. Class level B is the standard military quality level, it is intended for high reliability military applications.

6.4.40 Class level S. Class level S requirements contained in this document define the requirements for class V, class Y, and class P (class level S) (Space level product), including SMDs and M38510 JAN slash sheet product. Class level S is the highest reliability level provided for in this specification, it is intended for space applications.

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6.4.41 Class level vs Class. This specification defines the requirements for two class levels of product, class level S and class level B. Each class level is made up of multiple classes of product, class level S contains the requirements for classes V, Y and P product, and class level B contains the requirements for class Q and class B product.

6.4.42 Second party facility. A second party facility is a QA approved facility that acts as a subcontractor to a QML device manufacturer (e.g. QML Company X using QML Company Y for wafer fabrication, or as a test lab performing TCI testing).

6.4.43 Third party facility. A third party facility is a manufacturer whose facility does not have QML certification. The process or line used by the QML manufacturer has been certified through the manufacturer for those products supplied as QML by the manufacturer (e.g., QML Company X using non-QML Company Z to Fab die, only the line or process of the non-QML company is evaluated for use by the QML manufacturer not the entire facility).

6.4.44 New technology. New technology is defined as a product family, material, or process that has never been previously characterized and qualified by the manufacturer for a military or space level application.

6.4.45 Mature technology. A mature technology is defined as one which the manufacturer has previously released to production and has a continuous reliability monitor plan in place to identify major reliability life-limiting mechanisms, detect long-term product shifts, and generate process data or established proof of stable process and/or equipment with negligible wear out.

6.4.46 Lot date code. Lot date code will be assigned to identify the devices with the assembly processing and assembly location. Devices will be traceable through the lot date code to the assembly year, sealing week and assembly location.

6.4.47 Storage temperature. The optimal storage temperature range is defined as -65°C to +150°C.

6.4.48 Multi-product wafer (MPW) . A wafer composed of more than one integrated circuit (microcircuit) design fabricated on the same wafer. The Multi-product wafer (MPW) may contain a Standard Evaluation Circuit (SEC) design along with product designs or contain just product designs. MPW wafers will be fabricated as a wafer lot as defined in section 6.4.7.

6.4.49 Package integrity demonstration test plan (PIDTP) . The package integrity demonstration test plan defines to address the manufacturability, test, quality and reliability issues associated with unique to specific assembly/package techniques as defined in Appendices B and H.

6.4.50 Thin layer capacitor. A thin layer capacitor is a capacitor rated voltage at 50 volts or less with dielectric thickness less than 0.8 mil or a capacitor rated voltage greater than 50 volts with a dielectric thickness less than 1.0 mil. Dielectric thickness is the actual measured thickness of the fired ceramic dielectric layer (see MIL-PRF-123 and MIL-PRF-32535).

6.4.51 Glass transition temperature. The glass transition temperature is the temperature which an amorphous solid becomes soft upon heating or brittle upon cooling.

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6.5 Discussion. The foundation of generic qualification is the requirement for a Quality Management (QM) program within the manufacturing environment. QM requires that all levels of management and non-management be actively involved in the commitment to quality. Also, a TRB is to be established to control, stabilize, monitor and improve the qualified technology. The TRB will develop a QM plan that outlines how the manufacturing operation for a given technology is controlled, monitored and improved throughout its entire "life cycle". Key aspects of this plan are the establishment of statistical process control (SPC), field failure return programs, corrective action procedures, quality improvement, and any other approaches required to control and improve product quality and reliability. These requirements are detailed in this specification. Further, this specification describes procedures and requirements for manufacturer's listing on the QML for integrated circuits. Manufacturers listed on the QML will be able to produce microcircuits without the need for extensive end-of-manufacturing qualification testing and QCIs on each device design. The reduction of the end-of-manufacturing testing will be replaced with in-line monitoring and testing and SPC. Also, surrogate devices, such as the SEC will be used to assess the technology's reliability. Introduction of this methodology shifts the emphasis from the need of individual microcircuit qualification to process (technology) certification and qualification. This will accelerate the microcircuit insertion cycle of high quality and reliable microcircuits.

The generic qualification philosophy, leading to QML, is a process by which a manufacturer acquires a manufacturing line or technology flow certification and qualification. Ongoing monitoring techniques will be used to maintain QML status. The manufacturing line consists of facilities and procedures appropriate to accomplish the design, mask making, wafer fabrication, assembly, package and testing of microcircuits (see figure 1). figure 2 illustrates six possible combinations of a manufacturing line utilizing three design centers, two mask fabrication facilities, three wafer fabrication facilities, two package and assembly sites and two test facilities. The procedure of generic qualification is accomplished in two stages; certification and qualification. The process of certification is the recognition of evidence by the QA that the manufacturing line is capable of producing microcircuits of high quality and compliant with the requirements of this specification. Qualification is the actual demonstration of the certified manufacturing line capabilities by producing "first pass" microcircuits compliant with the requirements of this specification and the device specification. On figure 2, each block can be individually reviewed, but is to be certified as a flow. The only process flow which would be qualified (QML listed) would be the group of blocks which are linked together and tested during qualification. The letters "A" and "B" indicate a QML flow where qualification testing has qualified a complete path. The other paths are not QML until certification and qualifications testing of those processes are done.

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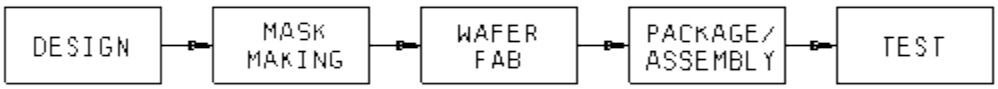

FIGURE 1. The QML manufacturing line.

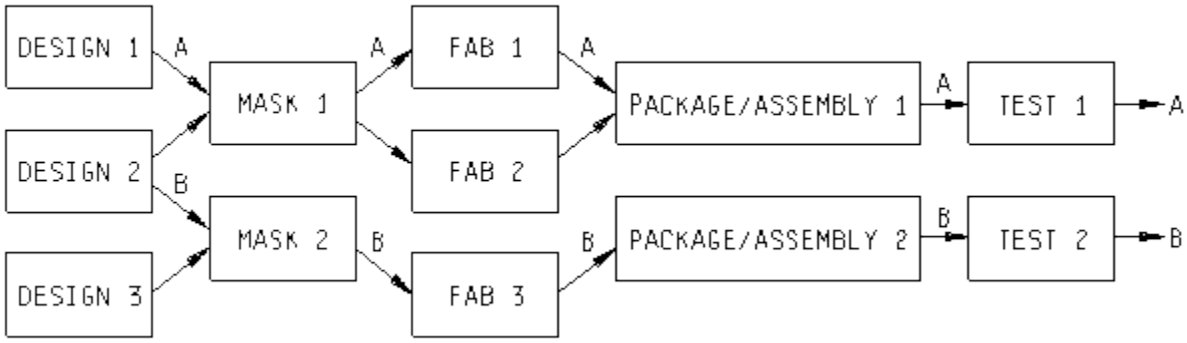

FIGURE 2. Combinations of a manufacturing line.

QM does not stop with a manufacturer listed on the QML. This specification identifies the necessary screens which QML devices are to be capable of meeting. These screens can be reduced or changed by the manufacturers' TRB when gathered reliability data on the technology indicates that such changes are substantiated. The philosophy of generic qualification incorporates the idea that high quality and reliable microcircuits can be obtained without excessive testing if the processes are properly monitored and controlled at each step of the manufacturing line. The following describes the monitors and controls that may be used.

a. The design procedure and tools are controlled in such a manner that the ensuing microcircuit design performs only with limits that have been shown to be reliable for the technology being used, within the constraints of established design rules (electrical, geometric and reliability).

b. The mask fabrication facility is controlled such that an error free mask is produced from the microcircuit design database. Monitoring, controlling and reducing defect density is helpful in obtaining error free masks.

c. The wafer fabrication process is controlled with the following: Use of in-line statistical control; a parametric monitor structure for measuring electrical parameters; a TCV structure to study intrinsic reliability mechanisms; and a SEC to monitor the fabrication process and to serve as a surrogate microcircuit for reliability testing.

d. The package and assembly facility is controlled with emphasis on in-line statistical process control of all assembly steps.

e. The test area controls consist of test equipment accuracy and calibration as well as a controlled interface to the microcircuit design center.

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f. The overall control of the process are under the auspices of a TRB which is established by the manufacturer. The TRB is solely responsible for the QML flow that has been certified and qualified.

g. For RHA devices, procedures and requirements are integrated into this specification for establishing and demonstrating a RHACL for the technology. Many device-oriented tests can be reduced or eliminated when correlation data for models and test structures have been established by the TRB. The main concern in the RHA community is whether the device specification accurately describes the device performance in the radiation environment specified. Until such models and test structures are developed, some actual device radiation testing will be required.

h. Appendix B to this specification defines an implementation transition approach which may be used for space or other critical environment applications.

6.6 Additional reference documents. The following documents are not directly referenced herein but should be used as guidelines.

MIL-HDBK-339 - Custom Large Scale Integrated Circuit Development and Acquisition for Space Vehicles.
MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices.
MIL-HDBK-815 - Dose-Rate Hardness Assurance Guidelines.
MIL-HDBK-816 - Guidelines for Developing Radiation Hardness Assurance Device Specifications.
MIL-HDBK-817 - System Development Radiation Hardness Assurance.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

ASTM INTERNATIONAL (ASTM)

ASTM B487 - Standard Test Method for Measurement of Metal and Oxide Coating Thickness by Microscopical Examination of a Cross Section.

ASTM B567 - Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD541 - Packaging Material Standards for ESD Sensitive Items.
JEP95 - JEDEC Registered and Standard Outlines for Solid State and Related Products.
JESD16 - Assessment of Average Outgoing Quality Levels in Parts Per Million (PPM).

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

ANSI/ESDA/JEDEC JOINT STANDARD

ANSI/ESDA/JEDEC JESD541 - Packaging Material Standards for ESD Sensitive Items.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.) or

(Copies of these documents are available online at https://www.esda.org/ or from Electrostatic Discharge Association(ESDA) 7900 Turin Road, Bldg. 3, Rome, NY 13440.)

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6.7 Subject term (key word) listing.

Application specific integrated circuit (ASIC)
Computer-aided design (CAD)
Design-for-test (DFT)
Design rule check (DRC)
Electrical rule check (ERC)
Enhanced low dose rate sensitivity (ELDRS)
Electrostatic discharge (ESD)
Failure analysis (FA)
Joint Test Action Group (JTAG)
Linear energy transfer threshold (LET_{TH})
Mean time to failure (MTTF)
Parametric monitor (PM)
Post irradiated end-point parameter limits (PIPL)
Quality management (QM)
Radiation hardness assurance (RHA)
Radiation hardness assurance capability level (RHACL)
Single event effects (SEE)
Standard evaluation circuit (SEC)
Statistical process control (SPC)
Technology characterization vehicle (TCV)
Technology conformance inspection (TCI)
Technology Review Board (TRB)
Time dependent dielectric breakdown (TDDB)
Very high speed integrated circuit (VHSIC)
VHSIC hardware description language (VHDL)
Package integrity demonstration test plan (PIDTP)
Multi-product wafer (MPW)

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6.8 List of acronyms.

AQL	- Acceptable quality level
ANSI	- American National Standards Institute
ASIC	- Application specific integrated circuit
ASTM	- American Society for Testing and Materials
BV	- Breakdown voltage
CAD	- Computer aided design
CAGE	- Commercial and Government Entity
CDM	- Charged device model
CMOS	- Complementary metal oxide semiconductor
SAM	- Scanning acoustical microscopy
CSI	- Contractor source inspection
DFT	- Design-for-test
DMS	- Diminishing manufacturing sources
DRC	- Design rules check
DSCC	- Defense Supply Center, Columbus
DTL	- Diode transistor logic
ECL	- Emitter coupled logic
EEE	- Electrical, electronic, and electromechanical
EIA	- Electronic Industries Alliance
ELDRS	- Enhanced low dose rate sensitivity
EPI	- Epitaxial
ERC	- Electrical rules check
ESD	- Electrostatic discharge
ESDA	- Electrostatic discharge association
FA	- Failure analysis
FET	- Field effect transistor
FIFO	- First in, first out
FSC	- Federal stock class
GaAs	- Gallium arsenide
GCR	- Galactic cosmic rays
GIDEP	- Government - Industry Data Exchange Program
g_m	- linear transconductance
GSI	- Government Source Inspection
HAST	- Highly accelerated temperature and humidity stress test
HAST	- Human body model
HCMOS	- High-speed CMOS
HDBK	- Handbook
IC	- Integrated circuit

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ILB	- Inner lead bond
IGA	- Internal gas analysis
JAN	- Joint Army Navy
JEDEC	- (Formerly known as Joint Electronic Device Engineering Council)
JEP	- JEDEC publication
JESD	- JEDEC standard
JTAG	- Joint Test Action Group
LET	- Linear energy transfer
LET_{TH}	- Linear energy transfer threshold
MIL	- Military
MOS	- Metal oxide semiconductor
MTTF	- Mean time to failure
NASA	- National Aeronautics and Space Administration
NDBP	- Nondestructive bond pull
OEM	- Original equipment manufacturer
PDA	- Percent defective allowable
PIN	- Part or identifying number
PIDTP	- Package integrity demonstration test plan
PIND	- Particle impact noise detection
PIPL	- Post - irradiation parameter limits
PLA	- Programmable logic array
PM	- Parametric monitor
PPM	- Parts per million
PROM	- Programmable read only memory
QA	- Qualifying activity
QAR	- Quality assurance representative
QCI	- Quality conformance inspection
QM	- Quality management
QML	- Qualified manufacturer listing
QPL	- Qualified products list
RAM	- Random access memory
RH	- Relative humidity
RHA	- Radiation hardness assurance
RHACL	- Radiation hardness assurance capability level
RMS	- Root mean square
ROM	- Read only memory
RSS	- Radiation source of supply
SAE	- Society of Automotive Engineers
SEC	- Standard evaluation circuit
SEE	- Single event effects

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SEM	- Scanning electron microscope
SEP	- Single event phenomenon
SEU	- Single event upset
SMD	- Standard Microcircuit Drawing
SOI	- Silicon on insulator
SOS	- Silicon on sapphire
SPC	- Statistical process control
SSS	- Sample size series
STD	- Standard
TAB	- Tape automated bonded
TCI	- Technology conformance inspection
TCV	- Technology characterization vehicle
TDDB	- Time dependent dielectric breakdown
TLD	- Thermo luminescence dosimetry
TM	- Test method (e.g., MIL-STD-883)
TRB	- Technology review board
TTL	- Transistor transistor logic
UL	- Underwriters Laboratory
VHDL	- VHSIC hardware description language
VHSIC	- Very high speed integrated circuit
VT	- Threshold voltage

6.9 Changes from previous issue. Marginal notations are not used in this revision to identify changes with respect to the previous issue due to the extent of the changes.

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APPENDIX A

MICROCIRCUIT SPECIFICATION REQUIREMENTS

A.1 SCOPE

A.1.1 Scope. This appendix establishes the minimum requirements for MIL-STD-883 compliant class level B and S, monolithic and multichip microcircuits and the quality and reliability assurance requirements that are to be met in the acquisition of these microcircuits. This appendix will also be required as a performance baseline for qualified manufacturer listing (QML) class level B and S microcircuits. Detail requirements, specific characteristics of microcircuits, and other provisions which are sensitive to the particular use intended are to be specified in the applicable device specification. Two levels, class B and S, of product assurance requirements and control for monolithic and multichip microcircuits are provided for in this appendix. It is the intent of the Government that a compliant manufacturer can use this appendix as the first step to becoming a qualified manufacturer under the QML program. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. However, for QML microcircuits the manufacturers may offer approved alternatives that demonstrate a process control system that achieves at least the same level of quality and reliability as could be achieved by this appendix.

A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in sections A.3, A.4, or A.5 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections A.3, A.4, and A.5 of this appendix, whether or not they are listed.

A.2.2 Government documents.

A.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-I-46058 - Insulating Compound, Electrical (For Coating Printed Circuit Assemblies).
MIL-M-38510 - Microcircuits, General Specification For.
MIL-DTL-45204 - Gold Plating, Electrodeposited

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1285 - Marking of Electrical and Electronic Parts.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-505 - Definitions of Item Levels, Item Exchangeability, Models, and Related Terms.
MIL-HDBK-780 - Standard Microcircuit Drawings.
MIL-HDBK-1331 - Parameters to be Controlled for the Specification of Microcircuits, Handbook For.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

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A.2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

QML-38535 - Qualified Manufacturers List of Products Qualified Under Performance Specification MIL-PRF-38535 Integrated Circuits (Microcircuits) Manufacturing, General Specification For.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

A.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F15 - Standard Specification for Iron-Nickel-Cobalt Sealing Alloy.
ASTM F30 - Standard Specification for Iron-Nickel Sealing Alloy.
ASTM B170 - Standard Specification for Oxygen-Free Electrolytic Copper-Refinery Shapes.
ASTM B487 - Standard Test Method for Measurement of Metal and Oxide Coating Thickness by Microscopical Examination of a Cross Section.
ASTM B567 - Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
ASTM B568 - Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

International Organization for Standardization (ISO)

ISO/IEC 17025 - General requirements for the competence of testing and calibration laboratories

(Copies of these documents are available online at https://www.iso.org or from ISO Central Secretariat, Chemin de Blandonnet 8, CP 401, 1214 Vernier, Geneva, Switzerland.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD31 - General Requirements for Distributors of Commercial and Military Semiconductors.
JESD471 - Symbol & Label for Electrostatic Sensitive Devices.
JESD625 - Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.
JEP114.01 - Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training and Certification.
JEP121 - Requirements for Microelectronic Screening and Test Optimization.
JEP163 - Selection of Burn-in/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

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APPENDIX A

ANSI/ESDA/JEDEC JOINT STANDARD

ANSI/ESDA/JEDEC JS-001 - For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) - Component Level.

ANSI/ESDA/JEDEC JS-002 - For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.

ANSI/ESDA/JEDEC JESD541 - Packaging Material Standards for ESD Sensitive Items.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.) or

(Copies of these documents are available online at https://www.esda.org or from Electrostatic Discharge Association(ESDA) 7900 Turin Road, Bldg. 3, Rome, NY 13440.)

ELECTROSTATIC DISCHARGE ASSOCIATION (ESDA)

ANSI/ESDA S20.20 – For the Development of an Electrostatic Discharge Control Program for- Protection of Electrical and Electronics parts, Assemblies and equipment.

(Copies of these documents are available online at https://www.esda.org/ or from Electrostatic Discharge Association(ESDA) 7900 Turin Road, Bldg. 3, Rome, NY 13440.)

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO) STANDARDS

ISO 14644-1 - Clean rooms and Associated Controlled Environments – Part 1: Classification of Air Cleanliness.

ISO 14644-2 - Clean rooms and Associated Controlled Environments – Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1.

(Copies of these documents are available online at https://www.iest.org/ or from Institute of Environmental Sciences and Technology (IEST), 940 East Northwest Highway, Mount Prospect, IL 60056-3444.)

SAE International

SAE-AMS-I-23011 - Iron-Nickel Alloys for Sealing to Glasses and Ceramics.

(Copies of this document are available online at https://www.sae.org/ or from Society of Automotive Engineers, 400 Commonwealth Dr., Warrendale, PA 15096-0001.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

A.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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A.3 REQUIREMENTS

A.3.1 General. The manufacturer of microcircuits in compliance with this appendix shall have and use production and test facilities and a quality and reliability assurance program adequate to assure successful compliance with the provisions of this appendix, the manufacturer's baseline (DSCC-VQC-42 or equivalent) and the device specification or drawing. The individual item requirements shall be as specified herein, and in accordance with the device specification or drawing.

The requirements of this appendix, or 1.2.1 of MIL-STD-883 are met or exceeded by product built to a QML certified flow by a QA certified and qualified manufacturer or by a manufacturer who has been granted transitional certification to MIL-PRF-38535. The QML flow as documented in the QM plan allows modification to processes and tests used in producing QML devices (See J.3.12 herein). These changes shall not affect the form, fit, function or radiation hardness assurance level (when applicable) of any QML devices. These devices are marked with the "Q" or "QML" certification mark to reflect the QML flow used.

A.3.1.1 Reference to device specification or drawing. For purposes of this appendix, when the term "as specified" is used without additional reference to a specific location or document, the intended reference shall be to the device specification or drawing which constitutes the applicable individual device specification.

A.3.1.2 Conflicting requirements. In the event of conflict between the requirements of this appendix, this specification and other requirements of the applicable device specification, the precedence in which requirements shall govern, in descending order, is as follows:

a. Applicable device specification or drawing.

b. This appendix.

c. Specifications, standards, and other documents referenced in A.2.2 and A.2.3.

A.3.1.3 Terms, definitions, symbols and requirements. For the purpose of this appendix, the terms, definitions, and symbols of MIL-STD-883 and MIL-HDBK-1331, and those contained herein shall apply and shall be used in the applicable device specifications or drawings wherever they are pertinent. The definitions of part, subassembly, assembly, unit, group, set, and system, as well as the ancillary terms accessory and attachment are contained in MIL-HDBK-505. To further define a particular type of microcircuit, additional modifiers may be prefixed.

A.3.1.3.1 Microelectronics. The area of electronic technology associated with or applied to the realization of electronic systems from extremely small electronic parts or elements.

A.3.1.3.2 Element (of a microcircuit or integrated circuit). A constituent of the microcircuit, or integrated circuit, that contributes directly to its operation. (e.g., A discrete part incorporated into a microcircuit becomes an element of the microcircuit.)

A.3.1.3.3 Substrate (of a microcircuit or integrated circuit). The supporting material upon or within which the elements of a microcircuit or integrated circuit are fabricated or attached.

A.3.1.3.4 Integrated circuit (microcircuit) . Integrated circuit (microcircuit). A die with a high equivalent circuit element density, composed of interconnected elements on or within a single substrate to perform an electronic circuit function. (e.g., This excludes printed wiring boards, circuit card assemblies, and modules composed exclusively of discrete electronic parts.)

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A.3.1.3.4.1 Multichip microcircuit or multichip module (MCM). An integrated circuit or microcircuit consisting of two or more die which are attached to a substrate or package and meets all applicable requirements of section 3.4.

A.3.1.3.4.2 Hybrid microcircuit. A microcircuit consisting of elements that are a combination of the film microcircuit type (see A.3.1.3.4.4) and the semiconductor types (see A.3.1.3.4.1 and A.3.1.3.4.3) or a combination of one or both of the types with discrete parts.

A.3.1.3.4.3 Monolithic microcircuit (or integrated circuit). A microcircuit consisting exclusively of elements formed in situ on or within a single semiconductor substrate with at least one of the elements formed within the substrate.

A.3.1.3.4.4 Film microcircuit (or film integrated circuit). A microcircuit consisting exclusively of elements which are films formed in situ upon an insulating substrate.

A.3.1.3.5 Production lot. A production lot shall consist of devices manufactured on the same production line(s) by means of the same production technique, materials, controls, and design. Where a production lot identification is terminated upon completion of wafer or substrate processing, or at any later point prior to device sealing, it shall be permissible to process more than a single device type in a single production lot provided traceability is maintained by assembling devices into inspection lots, as defined herein, at the point where production lot identification is terminated.

A.3.1.3.6 Inspection lot - class level S. An inspection lot for class level S microcircuits shall consist of a single device type from a single wafer lot in a single package type and lead finish unless otherwise specified in the QM plan. With qualifying activity approval, a maximum of 4 wafer lots may be used to form a class level S inspection lot. All devices shall be sealed within a single week. All assembly operations from die mounting through package sealing shall be completed within the same 6-week period. Each inspection sublot shall be uniquely identified to maintain traceability of that sublot from the wafer lot to the inspection lot (see A.3.4.6 and A.4.3.3).

A.3.1.3.7 Inspection lot - class level B. A quantity of microcircuits submitted at one time for inspection to determine compliance with the requirements and acceptance criteria of the applicable device specification. Each inspection lot shall consist of microcircuits of a single device type, in a single package type and lead finish. Each inspection lot shall be manufactured on the same production lines through final seal by the same production techniques and sealed within the same period not exceeding 6 weeks. Inspection lot identification shall be maintained from the time the inspection lot is formed through the time the lot is accepted, and shall be traceable to the production lot(s) from which the inspection lot was formed (see A.3.4.6 and A.4.3.3).

A.3.1.3.8 Inspection sublot - class level S. An inspection sublot for class level S microcircuits shall be a division (one wafer lot maximum) of parts in an inspection lot into smaller quantities of parts (see A.4.5.2 herein).

A.3.1.3.9 Inspection lot split - class level B. A class level B inspection lot split shall be a further division of the number of parts in an inspection lot into smaller quantities of parts (see A.4.5.2 herein).

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A.3.1.3.10 Wafer lot. A wafer lot consists of microcircuit wafers formed into a lot at the start of wafer fabrication for homogeneous processing as a group, and assigned a unique identifier or code to provide traceability, and maintain lot integrity throughout the fabrication process (see A.4.3.3 herein).

A.3.1.3.11 Package type. A package with a unique case outline (see MIL-STD-1835), configuration, materials (including bonding wire and die attach), piece parts (excluding pre-forms which differ only in size), and assembly processes.

A.3.1.3.12 Microcircuit group. Microcircuits which are designed to perform the same type of basic circuit function (e.g., for linear: Amplifier, comparator, sense amplifier, regulator, etc.; for digital: Logic gate buffer, flip-flop, combinational gate, sequential register/counter) within a given circuit technology (e.g., diode transistor logic (DTL), non-Schottky transistor transistor logic (TTL), emitter coupled logic (ECL), Schottky TTL, linear, hybrid, metal oxide semiconductor(MOS)) which are designed for the same supply, bias and signal voltages and for input-output compatibility and which are fabricated by use of the same basic die construction and metallization; the same die attach method; and by use of bonding interconnects of the same size, material and attachment method.

A.3.1.3.13 Percent defective allowable (PDA). Percent defective allowable is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

A.3.1.3.14 Delta limit (Δ). The maximum change in a specified parameter reading which will permit a device to be accepted on the specified test, based on a comparison of the present measurement with a specified previous measurement. NOTE: When expressed as a percentage value, it shall be calculated as a proportion of the previous measured value.

A.3.1.3.15 Rework. Any processing or reprocessing operation documented in accordance with A.4.8.1.1.6h herein, other than testing, applied to an individual device, or part thereof, and performed subsequent to the prescribed non repairing manufacturing operations which are applicable to all devices of that type at that stage.

A.3.1.3.16 Final seal. That manufacturing operation which completes the enclosure of a device so that further internal processing cannot be performed without disassembling the device.

A.3.1.3.17 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services; or it may be a contractor or subcontractor when the organizational element of the Government has given specific written authorization to such contractor or subcontractor to serve as agent of the acquiring activity. A contractor or subcontractor serving as agent of the acquiring activity shall not have the authority to grant waivers, deviations, or exceptions to this appendix unless specific written authorization to do so has also been given by the Government organization (e.g., preparing activity).

A.3.1.3.18 Qualifying activity. The organizational element of the Government that grants certification and qualification for the specific associated end-product in accordance with this appendix and the applicable device specification or drawing. For non-JAN product built in accordance with this appendix, the qualifying activity shall be either the acquiring activity or quality organization within the manufacturer's company that is independent of the group(s) responsible for device production screening and marketing or by an independent organization outside the manufacturer's company.

A.3.1.3.19 Device type. The term device type refers to a single specific microcircuit configuration. Samples of the same device type will be electrically and functionally interchangeable with each other at the die or substrate level even though made by different manufacturers using different mechanical layouts and possibly different materials. The electrical and environmental limits will be the same (but not necessarily the inherent reliability) for a given device type even though the device class, the case outline, the lead finish, the lot identification code, and the manufacturer may be different.

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A.3.1.3.20 Die type. A microcircuit manufactured using the same physical size, materials, topology, mask set, and process flow, on a single fabrication line.

A.3.1.3.21 Antistatic. An antistatic material resists triboelectric charging upon contact and separation with another material. Plastic materials impregnated with antistatic agents (antistats) are antistatic if their surface resistivity is between 10^9 and 10^{14} ohms/square.

A.3.1.3.22 Conductive. A conductive material is one capable of electrostatic field shielding and having a volume resistivity of 10^3 ohm-cm maximum or a surface resistivity less than 10^5 ohms/square.

A.3.1.3.23 Insulating. An insulating material is defined as having a volume resistivity of 10^{12} ohm-cm minimum, or a surface resistivity of 10^{14} ohms/square minimum.

A.3.1.3.24 Dissipative. A dissipative material is defined as having a surface resistivity between 10^5 and 10^9 ohms/square.

A.3.1.3.25 Radiation hardness assurance (RHA). The portion of product assurance which insures that parts continue to perform as specified or degrade in a specified manner when subjected to the specified radiation environmental stress.

A.3.1.3.26 Electrostatic discharge (ESD) sensitivity. Electrostatic discharge sensitivity is defined as the level of susceptibility of a device to damage by static electricity. The level of susceptibility of a device is found by ESD classification testing and is used as the basis for assigning an ESD class (see A.3.4.1.4).

A.3.1.3.27 Custom microcircuit. A nonstandard microcircuit, the design, and right(s) to the design (for example, ownership, control, or proprietary rights) of which are under the control of the purchaser-user of the microcircuit.

A.3.1.3.28 Die family. All devices manufactured by the same basic process (e.g., low power Schottky, high speed CMOS (HCMOS), Bipolar linear, CMOS linear, MOS memory, etc.) as specified in tables A-VI, A-VII, A-VIII, and A-IX.

A.3.1.3.29 Package family. A set of package types with the same package configuration (e.g., side brazed, bottom brazed) material type (e.g., alumina, beryllium oxide (BeO)) package construction techniques (e.g., single layer, multilayer) terminal pitch, except for can packages in which pin circle diameter can be used in place of terminal pitch, lead shape (e.g., gullwing, J-hook), and row-spacing (e.g., dual-in-line packages only) and with identical package assembly techniques (e.g., material and type of seal, wire bond method and wire size, die attach method and material).

A.3.1.3.30 Military operating temperature range. The military temperature range or military operating temperature range is defined as -55°C to +125°C.

A.3.1.3.31 Process monitor. The regularly scheduled periodic sample measuring of a parameter during normal performance of production operations in accordance with the manufacturer's approved program plan. The parameter to be measured, the frequency of measurement, the number of sample measurements, the conditions of measurement, the analysis of measurement data shall vary as a function of the requirements, capability and criticality of the operation being measured.

A.3.1.3.32 Device specification. The terms device specification or Standard Microcircuit Drawing (SMD) shall be used exclusively to reference or describe Government published documents with the combined purposes of standardization and procurement which detail the specific requirements of performance based microcircuits.

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A.3.1.3.33 Class level B. Class level B requirements contained in this document are intended for use for class Q and class M products, as well as class B M38510 JAN slash sheet product. Class level B requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for high reliability military applications.

A.3.1.3.34 Class level S. Class level S requirements contained in this document are intended for use for class V, class Y, or class P and slash sheet M38510 JAN product. Class level S requirements are also intended for use for product claimed as 883 compliant or 1.2.1 compliant for space level applications.

A.3.2 Item requirements. The individual item requirements for microcircuits delivered under this appendix shall be documented in the device specification or SMD or other drawing (SMD format, in accordance with MIL-HDBK-780, shall be used for drawings). Unless otherwise specified in the device specification or drawing, all devices procured under this appendix shall have an operating ambient temperature range from -55°C to +125°C and any references to minimum or maximum operating temperatures shall refer to the respective lower and upper limits of this range. Contractor-prepared specifications or drawings shall be approved by the acquiring activity as acceptable for the requirements of a specific contract or order, at the time of acquisition.

A.3.2.1 Electrical test requirements. The electrical test requirements (parameters, test conditions, test limits, and applicable test temperatures) which apply to electrical screening (e.g., final electrical parameters), group A Quality Conformance Inspection (QCI), and end-point electrical testing for other QCI subgroups shall be clearly documented by the manufacturer as to the actual parameters, conditions, methods, limits, burn-in/life test circuits, and test temperatures used in device testing. All those parameters important to the design application of the device shall be specified over the full military operating temperature range and supply voltage range and be included in the testing requirements of the applicable specification(s). For devices whose initial release date is after 29 May 1987, the subgroups to be tested, and the parameters that constitute a subgroup shall, as a minimum, be equivalent to those of the most similar device specification or drawing. The manufacturer's electrical test specification shall be documented in a SMD device specification table I format, or equivalent, that is clear to the user and shall be available to the user upon request.

A.3.2.2 Alternate die/fabrication requirements. When deemed necessary by the preparing or acquiring activity, (e.g., a class M SMD device, a DLA Land and Maritime drawing device, a MIL-STD-883 compliant device, or a Qualified Products List/Qualified Manufacturers List (QPL/QML) device or a unique package/die combination is not available from a DLA Land and Maritime drawing, SMD, QML, or QPL source that meets the full wafer fabrication requirements of this appendix), the DLA Land and Maritime drawing, SMD, JAN specification sheet or other procurement document (e.g., contractor-prepared drawing for “D” certification only) may be modified to provide a source for logistics support. This modification shall allow either a detailed certificate of compliance (itemized listing of die fabrication requirements from this appendix - see example in A.3.2.2.1 herein) or a die evaluation as defined by A.3.2.2.2 herein to be used in lieu of meeting the full die/fabrication requirements of this appendix. Alternate die fabrication requirements of A.3.2.2.1 and A.3.2.2.2 are permitted only for product that does not have the required traceability of A.3.4.6. These alternate requirements are acceptable only when the manufacturer planning to use this allowance has information on the wafer lot number, date of fabrication of the die, the fabrication line where the die was processed, and that the die was previously qualified by a QML/QPL manufacturer (for QML product) or by a MIL-STD-883 compliant manufacturer (for MIL-STD-883 compliant product). The manufacturer that meets the die/fabrication requirements of A.3.2.2.1 or A.3.2.2.2 is required to perform QCI testing of groups C and D (and E if applicable) on the first inspection lot of each wafer lot and shall replace the “C” certification mark with a “D” certification mark. An additional complete group D test is not required if the manufacturer already has group D coverage on the package family; however, subgroups D3 and D4 shall be required on the first inspection lot of the wafer lot. For excess die from the evaluated wafer lot, an additional group C and group D (subgroups D3 and D4 only) tests are not required for subsequent inspection lots built solely from die from that wafer lot. If the product is built in full compliance to the requirements of this appendix (the alternate die/fabrication allowance of A.3.2.2 is not being used), the “C” certification mark shall be used on the device.

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A.3.2.2.1 Example C of C. This C of C from the wafer manufacturer certifies that the product identified by fabrication code XXXXXX meets the fabrication requirements of appendix A of MIL-PRF-38535 (1.2.1 of MIL-STD-883) including the following itemized requirements:

a. Change to product requirement of A.3.4.2.

b. Internal conductor (current density) requirements of A.3.5.5.

c. Traceability requirements of A.3.4.6.

d. Glassivation thickness requirements of A.3.5.8.

e. Die thickness requirement of A.3.5.9.

f. Quality assurance program requirements of A.4.8.

g. Control and traceability of design documentation requirements of A.3.5.4.

h. Workmanship and rework provisions of A.3.7.

i. Design and construction baseline requirements of A.4.8.1.3.8.

A.3.2.2.2 Die evaluation requirements. The following requirements shall be met for each wafer lot. The results of this evaluation shall demonstrate compliance to this appendix for wafer manufacturing requirements.

a. Functional diagram and high power photomicrographs.

b. Analysis of internal conductor materials.

c. Composition of glassivation material and thickness measurement.

d. Total die thickness measurement.

e. SEM analysis of metallization.

f. Adhesion of gold backing.

g. Calculated current density in accordance with this appendix.

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A.3.3 Classification of requirements. The requirements of the microcircuits are classified herein as follows:

Requirement	Paragraph
Quality assurance requirements	A.3.4
Qualification	A.3.4.1
Compliance validation	A.3.4.1.1
Process Monitor Programs	A.3.4.1.2
Qualification to RHA levels	A.3.4.1.3
Qualification to ESD classes	A.3.4.1.4
Change to product or QA program	A.3.4.2
Screening	A.3.4.3
Quality conformance inspection	A.3.4.4
Wafer lot acceptance	A.3.4.5
Traceability	A.3.4.6
Design and construction	A.3.5
Marking of microcircuits	A.3.6
Workmanship	A.3.7

A.3.3.1 Certification of conformance and acquisition traceability. Manufacturers or suppliers including dealers and distributors who offer the product described by this appendix shall provide written certification, signed by the corporate officer who has management responsibility for the production and assurance of the quality and reliability of the product, (1) that the product being supplied has been manufactured and tested in accordance with this appendix and conforms to all of its requirements, and can be reasonably expected to remain in conformance indefinitely unless destructively mishandled, (2) that all products are as described on the certificate which accompanies the shipment, and (3) that dealers and distributors have handled the product in accordance with the requirements of JESD625 and JESD31. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate, but, the responsibility for conformity with the facts shall rest with the responsible corporate officer. The certification shall be confirmed by documentation to the Government or to users with Government contractors or subcontractors, regardless of whether the products are acquired directly from the manufacturer or from another source such as a distributor. When other sources are involved, their acquisition certification shall be in addition to the certificates of conformance and acquisition traceability provided by the manufacturer and previous distributors. The certificate shall include the following information:

a. Manufacturer documentation:

(1) Manufacturer's name and address.

(2) Customer's or distributor's name and address.

(3) Device type and product assurance level.

(4) Lot date code and latest re-inspection date, if applicable.

(5) Quantity of devices in shipment from manufacturer.

(6) Statement certifying product conformance and traceability.

(7) Solderability re-inspection date, if applicable.

(8) Signature and date of transaction.

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(9) If applicable, the certificate shall include a statement indicating that alternate die/fab requirements are being used, see A.3.2.2 (”D” cert mark).

b. Distributor documentation for each distributor:

(1) Distributor's name and address.

(2) Name and address of customer.

(3) Quantity of devices in shipment.

(4) Latest re-inspection date, if applicable.

(5) Certification that this shipment is a part of the shipment covered by the manufacturer's documentation.

(6) Solderability re-inspection date, if applicable.

(7) Signature and date of transaction.

A.3.4 Quality assurance requirements. The quality assurance provisions provided in this appendix are intended to provide a compliant MIL-STD-883 class level B or level S device (see A.3.1.3.33 and A.3.1.3.34). Devices or lots which have failed to pass any tests applied or acceptance criterion (PDA) shall not be downgraded to any lower quality assurance level even though that test or criterion may not be a requirement of the lower level (a failed device or lot shall not be accepted). Where shown, method references are in accordance with MIL-STD-883.

A.3.4.1 Qualification. The manufacturer supplying devices in compliance to this appendix shall perform sufficient product qualification testing to assure the devices supplied meet the minimum class level B or S performance requirements as described herein. The manufacturer shall maintain documentation of qualification testing for review of the preparing or acquiring activity upon request.

A.3.4.1.1 Compliance validation. Although on-site audits are not a condition to begin supplying under the requirements of this appendix, all manufacturers supplying in compliance to this appendix are subject to periodic Government compliance validation audits on a drop-in basis with a minimum of notice.

A.3.4.1.2 Process monitor programs. Process monitor programs performed by the manufacturer shall be established as a minimum for the following processes: Scanning Electron Microscope (SEM), wire bonding, die attachment, lid seal, particle detection, lead trimming, and final lead finish thickness. The implementing procedures shall provide for frequency, sample size, reject criteria, allowable rework, and disposition of failed product/lot(s). With the exception of the particle detection monitor, a procedure is required for the traceability, recovery, and disposition of all units monitored since the last successful test. As with all monitors, the particle detection procedure shall provide for continual process improvement. Records of these monitors and procedures shall be maintained and available for review.

A.3.4.1.2.1 Inspection by scanning electron microscope (SEM). A continuing SEM program shall be established to ensure adequate process control and coverage of metallization at oxide steps, contact openings, and general metallization. A monthly (minimum frequency) SEM evaluation shall be performed on product that is in the manufacturing process. The SEM program shall establish routine control over metallization processes by process families or inspection of products.

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A.3.4.1.2.2 Wire bonding. The manufacturer shall monitor the wire bond strength in accordance with the manufacturer's documented procedure. The frequency of this procedure shall be performed at machine setup and at the end of the production run as a minimum. At the manufacturer's option, this procedure shall consider shift start and stop, change of operators, spools, packages, wire size, lot size, and other related factors.

A.3.4.1.2.3 Die attachment. The manufacturer shall monitor the die attachment integrity in accordance with the manufacturer's documented procedure. This procedure shall be performed at each equipment setup and at the end of the production run as a minimum. At the manufacture's option, this procedure shall consider other related factors.

A.3.4.1.2.4 Lid seal. The manufacturer shall monitor, as a minimum, glass frit packages for seal integrity in accordance with the manufacturer's documented procedure. A sample and test plan shall be available for review by the qualifying or preparing activity.

A.3.4.1.2.5 Particle detection. The manufacturer shall establish a particle detection monitoring program which assesses the particle contamination of sealed devices on an individual manufacturing line basis. The monitor shall have provisions for testing in accordance with TM 2020, condition A of MIL-STD-883. JEP114, "Guidelines for Particle Impact Noise Detection (PIND) Testing, Operator Training and Certification" may be used as a guideline. Suitable data for each manufacturing line shall be used to establish an appropriate need, sample size, and sampling frequency for each package family. Unless otherwise approved by the qualifying activity (QA), the minimum sampling frequency of those devices in production shall be once each month per package family. Investigative and corrective actions shall be established which address noted deficiencies. Records of this monitor shall be made available for review and shall represent at least the six-month period preceding the audit.

A.3.4.1.2.6 Lead trimming and final lead finish thickness. The manufacturer shall monitor the package lead lengths to assure meeting the applicable device specification or drawing for proper lead length and the final lead finish thickness in accordance with this appendix. The frequency of the lead length monitor shall be performed at each equipment setup as a minimum. A sample and test plan shall be available for review by the qualifying or preparing activity.

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A.3.4.1.3 Qualification to RHA levels. Qualification to a RHA level shall consist of characterization to the highest offered RHA level of total ionizing dose (TID). The conditions for radiation testing shall consist of exposing the devices in a step-stress manner to the highest dose level offered and as a minimum the two next consecutive lower RHA levels. The levels are identified as follows: 3 krad(Si), 10 krad(Si), 30 krad(Si), 50 krad(Si), 100 krad(Si), 300 krad(Si), 500 krad(Si), 1 Mrad(Si). The radiation testing plan (QM Plan) and qualification to the appropriate quality and reliability assurance level for device classes B, Q, S, V, Y or T shall be submitted for QA approval. The designator RHA levels are defined below:

RHA levels:

RHA level designator (see 3.6.2.1)	Total ionizing dose (TID) level in Rad (Si)
/ or -	No RHA
M	3 krad (Si)
D	10 krad (Si)
P	30 krad (Si)
L	50 krad (Si)
R	100 krad (Si)
F	300 krad (Si)
G	500 krad (Si)
H	1 Mrad (Si)

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A.3.4.1.4 Qualification to ESD classes. Initial qualification to an ESD class, or requalification after redesign, shall consist of qualification to the appropriate quality and reliability level (class level S or B) plus ESD classification in accordance with test method 3015 of MIL-STD-883. The ESD testing procedure defined within ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) may be used as an option in lieu of TM 3015 for applicable devices (e.g. high pin count devices wherein parasitic charge may effect ESD failures). However, manufacturers shall document such ESD testing procedure in the QM plan that require QA approval, and ESD classification levels as defined below shall be reported.

ESD class designator	Prior destination category	Optional individual part marking	Optional package marking	Electrostatic voltage
0	---	Δ0	Δ0	< 250 V
1A	---	ΔA	ΔA	250 V – 499 V
1B	---	ΔB	ΔB	500 V – 999 V
1C	---	ΔC	ΔC	1,000 V – 1,999 V
1 (see note)	A	Δ (see note)	Δ (see note)	0 V – 1,999 V
2	B	ΔΔ	ΔΔ	2,000 V – 3,999 V
3 (see note)	---	ΔΔΔ (see note)	ΔΔΔ (see note)	≥ 4,000 V
3A	---	ΔΔΔA	ΔΔΔA	4,000 V – 7,999 V
3B	---	ΔΔΔB	ΔΔΔB	≥ 8,000 V

NOTE: ESD class designator 1 has been replaced with designators 0, 1A, 1B, and 1C as of 15 March 2006. The manufacturer shall test and may mark the tested level obtained under “Optional individual part marking” and the optional individual part marking may be used as the pin one identifier. Also, ESD class designator 3 has been replaced by 3A and 3B ESD class designators. ESD class designation 3 may continue to be used for devices tested before 15 March 2006. After 15 March 2006, for newly developed products, the 3A and 3B designators shall be used. Prior designation category devices previously classed by test as category A may be marked as class 1 (Δ) and devices previously classified as category B may be marked as class 2 (ΔΔ).

a. Devices existing prior to 30 September 1989 that were not ESD classification tested shall be marked as class 1 until classified. Devices previously classified by test as category A shall be marked class 1. Devices previously classified by test as category B shall be marked as class 2. If it can be shown that test results obtained using TM 3015.3 of MIL-STD-883 correlate with results using TM 3015.6 of MIL-STD-883 (or later versions) or ANSI/ESDA/JEDEC JS-001 (see A.4.4.2.8) and give correct ESD classification, retesting of previously tested devices is not required except where redesign has occurred.

b. Beginning no later than 31 December 1988 but prior to 15 March 2006, all newly designed or redesigned device types shall have been classified as ESD class 1, 2, or 3 in accordance with TM 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 (see A.4.4.2.8). After 15 March, 2006 the device types shall be classified as above.

c. After 30 September 1989, in order to be compliant with this appendix or 1.2.1 of MIL-STD-883, all other device types for use in new system or equipment designs or system or equipment redesigns shall have completed classification in accordance with test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-0014(see A.4.4.2.8). All devices of existing design (e.g., not subject to A.3.4.1.4b above) shall be marked class 1 except when known by test to be, in fact, class 2 or better, in which case they shall be correctly identified for ESD.

d. Although little variation due to case outline is expected, if a device type is available in more than one package type or case outline, ESD testing and classification shall be applied to at least that one package type shown by experience to be worst case for ESD.

e. ESD testing classification results (or class one marking assigned without test) shall be submitted to DLA Land and Maritime-VA for all SMD devices built in compliance to this appendix. ESD testing classification results for non-SMD devices built in compliance to this appendix shall be retained by the manufacturer and made available to the acquiring or preparing activity upon request.

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A.3.4.2 Changes and notification of change to product or quality assurance program. The manufacturer shall be responsible for the implementation of any major changes(s) of the product or quality assurance program which may affect performance, quality, reliability, radiation hardness assurance (when specified), ESD class or interchangeability (see table A-I). Manufacturers shall notify the qualifying activity (QA) of any major changes as listed table A-I herein. The information needed to support these changes shall include acceptable engineering data, quality conformance inspection data, or a test plan sufficient to demonstrate that the changes(s) shall not adversely affect performance, quality, reliability, interchangeability, radiation hardness, or electrostatic discharge sensitivity and that the product will continue to meet the specification requirements. Notification to the qualifying activity (QA) and acquiring activity of major changes that may affect the performance, quality, reliability, or interchangeability to the product for devices acquired to any detail specification/drawing/data sheet is required. Major changes as defined in table A-I shall, as a minimum, be reviewed to determine whether notification to the users is required. The manufacturer shall make this notification to the acquiring activity at the time of acceptance of a new order or delivery of an existing order. The manufacturer may make notification of this change of product through the GIDEP using the Product Change Notice; in any case the manufacturer shall assure that all known acquiring activities for this product are notified.

A.3.4.2.1 Discontinuation of products. The manufacturer shall have a system that provides notification of product discontinuation which comprises date of discontinuation and last time buy opportunity in advance (at least 6 months in advance) to the DLA Land and Maritime for purchasing devices.

A.3.4.3 Screening. All microcircuits to be delivered or submitted for quality conformance in accordance with this appendix shall have been subjected to, and passed, all the screening tests detailed in TM 5004 of MIL-STD-883 for the type of microcircuit and quality assurance level (device class) specified.

A.3.4.4 Quality conformance inspection (QCI). Microcircuits shall not be accepted or approved for delivery until the inspection lot has passed QCI (see A.4.5).

A.3.4.5 Wafer lot acceptance. Class level S microcircuits furnished under this appendix shall be products from wafer lots that are subjected to and successfully meet the wafer lot acceptance inspections and tests specified in test method 5007 of MIL-STD-883 or equivalent procedures approved by the acquiring activity.

A.3.4.6 Traceability. Traceability shall be provided for all microcircuit quality assurance levels. Each delivered microcircuit shall be traceable to the inspection and wafer lot(s) (see A.4.8.1.2).

A.3.4.6.1 Lot travelers. The manufacturer shall maintain lot travelers to document the completion of each required processing step from wafer diffusion for class level S (and class level B radiation hardened devices) and beginning with assembly for class level B with wafer lot identification through microcircuit assembly and screening test. Travelers shall provide space for those items specified in A.4.8.1.3.7. The lot travelers shall provide traceability to all prior processing steps and shall be identifiable through assembly and acceptance testing and shall be monitored by the manufacturer's quality control organization.

A.3.4.7 Government source inspection. Government source inspection is required as detailed in the contract or order.

A.3.5 Design and construction. Microcircuit design and construction shall be in accordance with all the requirements specified herein and in the device specification or drawing.

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A.3.5.1 Package. All devices supplied under this appendix except for class Y, class N, and class P shall be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. No organic or polymeric materials (lacquers, varnishes, coatings, adhesives, greases, etc.) shall be used inside the microcircuit package unless specifically detailed in the device specification or drawing (e.g., polyimide interlayer dielectric). Alpha Particle protection is permitted if permitted by the device specification or drawing. Desiccants may be used in the microcircuit package (except for class level S devices where they are prohibited) only if each lot is subjected to and passes an internal gas analysis test, TM 1018 of MIL-STD-883, with a limit of 1,000 ppm at +100°C for a sample of 3(0). The internal moisture content for class level S devices, after completion of all screening, shall not exceed 5,000 ppm at +100°C. Polymer impregnations (backfill, docking, coating, or other uses of organic or polymeric materials to effect, improve, or repair the seal) of the microcircuit packages shall not be permitted. Polymer coating used to effect or improve marking adhesion shall not be applied over lid seal area.

NOTE: Packages containing beryllia shall not be ground, sand blasted, machined, or have other operations performed on them which shall produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that shall produce fumes containing beryllium.

A.3.5.1.1 Polymeric materials. All polymeric materials of microcircuits shall meet the requirements of TM 5011 of MIL-STD-883. Polymeric materials shall be approved by the acquiring or preparing activity.

A.3.5.1.2 Package configurations. Package configurations (e.g., 14-lead flat package, 16-lead DIP, 20-terminal SQ.CCP, etc.) defined in MIL-STD-1835 shall be in accordance with the case outline of MIL-STD-1835. Package configurations not defined in MIL-STD-1835 shall be specified in the applicable acquisition document, and require approval of the acquiring activity.

A.3.5.2 Metals. External metal surfaces shall be corrosion-resistant or shall be plated or treated to resist corrosion. External leads shall meet the requirements specified in A.3.5.6.

A.3.5.3 Other materials. External parts, elements or coatings including markings shall be inherently non-nutrient to fungus and shall not blister, crack, outgas, soften, flow or exhibit defects that adversely affect storage, operation, board assembly (e.g., permanently attached organic bumpers), or environmental capabilities of microcircuits delivered to this appendix under the specified test conditions.

A.3.5.4 Design documentation. Design, topography, and schematic circuit information for all microcircuits supplied under this appendix shall be available for review by the acquiring activity and the preparing activity upon request. Control and traceability of design documentation for all new designs and redesigns shall follow the guidelines of A.3.5.4.1 through A.3.5.4.4. This design documentation shall be sufficient to depict the physical and electrical construction of the microcircuits supplied under this appendix, and shall be traceable to the specific part, drawing, or type numbers to which it applies, and to the production lot(s) and inspection lot codes under which microcircuits are manufactured and tested so that revisions can be identified.

A.3.5.4.1 Die topography. For semiconductor die (monolithic die or dice for inclusion in multichip microcircuits), there shall be a photograph, drawing(s), mask list with revisions, or other representation defining the topography of the elements of the die without the intraconnection pattern.

A.3.5.4.2 Die intraconnection pattern. There shall be an enlarged photograph(s) or transparency of diazotypes of the mask set to the same scale as the die topography (see A.3.5.4.1) showing the specific intraconnection pattern used to connect the elements on the die so that elements used and those not used can be easily determined. For multichip microcircuits, this requirement shall apply to the substrate and all conductor pattern and active or passive circuit elements deposited thereon, as well as to semiconductor die, as applicable.

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A.3.5.4.3 Die to terminal interconnection. There shall be an enlarged photograph(s), transparency, or drawing(s) to scale and of sufficient magnification to clearly depict the interconnection pattern for all connections made by wire or ribbon bonding, beam leads or other methods between the semiconductor die, other elements of the microcircuit, substrate(s) and package terminals or lands as applicable to the specific type of microcircuit supplied. If these interconnections show clearly on the die intraconnection pattern photograph, an additional photograph or drawing is not required.

A.3.5.4.4 Schematic diagrams. For microcircuits supplied under this appendix, the actual schematic diagram(s), logic diagram(s), or combination thereof shall be maintained, sufficient to represent all electrical elements functionally designed into the microcircuit together with their values (when applicable). For simple devices, this shall be a complete detailed schematic circuit showing all functional elements and values. For complex devices, or those with redundant detail, the overall microcircuit may be represented by a logic diagram in combination with schematic details. Minimum details that shall be included are: A schematic presentation of input/output stages and protection network details identified by appropriate pin numbers. Sufficient details to depict addressing or other device elements where the test parameters, conditions, or limits are sensitive to the specific device schematics. Where parasitic elements are important to the proper functioning of any microcircuit, they shall be included in the schematic diagram.

A.3.5.5 Internal conductors. Internal thin film conductors on semiconductor die or substrate (metallization stripes, contact areas, bonding interfaces, etc.) shall be designed so that properly fabricated conductors shall not experience in normal operation, over the operating temperature range (see A.3.1.3.30) (at worst case specified operating conditions), a current density in excess of the maximum allowable value shown below for the applicable conductor material:

Conductor material	Maximum allowable current density
Aluminum (99.99 percent pure or doped) without glassivation or without glassivation layer integrity test	2×10^5 A/cm^2
Aluminum (99.99 percent pure or doped) glassivated (see A.3.5.5.4)	5×10^5 A/cm^2
Refractory metals (Mo, W, Ti-W, and Ti-N) glassivated (see A.3.5.5.4)	5×10^5 A/cm^2
Gold	6×10^5 A/cm^2
Copper	1×10^6 A/cm^2
All other	2×10^5 A/cm^2

The current density shall be calculated at the point(s) of maximum current density (e.g., greatest current (see A.3.5.5a) in accordance with unit cross section) for the specific device type and schematic or configuration. Individual device calculations are not required when appropriate documented design rules or requirements have been used, which limit or control the current density in the resulting design.

a. Use a current value equal to the maximum continuous current (at full fan-out for digitals or at maximum load for linear) or equal to the simple time averaged current obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point(s) of maximum current density. This current value shall be determined at the maximum recommended supply voltage(s) and with the current assumed to be uniform over the entire conductor cross-sectional area.

b. Use the minimum allowed metal thickness in accordance with manufacturing specifications and controls including appropriate allowance for thinning experienced in the metallization step. The thinning factor over a metallization step is not required unless the point of maximum current density is located at the step.

c. Use the minimum actual design conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

d. Areas of barrier metals, not intended by design to contribute to current carrying capacity, and non-conducting material shall not be included in the calculation of conductor cross section.

Thick film conductor's multichip substrates (metallization strips, bonding interfaces, etc.) shall be designated so that no properly fabricated conductor shall dissipate more than 4 watts/cm^2 when carrying maximum design current.

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TABLE A-I. Testing guidelines for changes identified as major.

Major changes		Testing per group A, B, C, D, E herein or TM 5005 of MIL-STD-883 (All electrical parameters in accordance with the device specification or drawing 1/)
a.	Doping material source concentration Process technique	Group A and C-1 deltas (variables only when deltas are required)
b.	Diffusion profile	Group A and C-1 deltas (variables only when deltas are required)
c.	Die structure	Group A and C-1 deltas (variables only when deltas are required)
d.	Mask changes affecting die size or active element	Variable group A, C-1 prior to shipment, and notify the qualifying activity if new area is smaller/larger in applicable package than previously qualified.
	Wafer diameter	Group A, C-1 prior to shipment
	Final die thickness	Group D-3
e.	Passivation/glassivation	Group A, C-1 and glass integrity test if current density is over 2 x 10^5
f.	Metallization changes	Group A, C-1, and B-5
g.	Die attach method	D-3 and D-4
h.	Die attach process	D-3 and D-4
i.	Bond process	B-5 and D-3
j.	Bond wire material/dimension	B-5 and D-3
k.	Package or lid structure	D-1 (variables), D-3, D-4, D-8 (lid torque) (variables)
	Package or lid material	D-3, D-4, D-5, D-6 (variables), and D-8 (lid torque) (variables)
	Package or lid dimension	D-1 (variables), D-2, and D-8 (lid torque) (variables)
	Lead frame material	See A.4.4.2.7
	Lead frame dimension	D-1 (variables) and D-2
	Cavity dimension	B-5, D-2, D-6 (variables), and D-8 (lid torque) (variables)
l.	Sealing profile	D-3, D-4, D-6 (variables), and D-8 (lid torque) (variables)
	Sealing material	D-3, D-4, D-6 (variables), and D-8 (lid torque) (variables)
	Frame attach	B-3, D-3, D-4, D-6 (variables), and D-7 (adhesion of lead finish) (variables)
	Frame cleaning	B-3, D-2, D-3, and D-7 (adhesion of lead finish)

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TABLE A-I. Testing guidelines for changes identified as major. - Continued.

Major changes		Testing per group A, B, C, D, E herein or TM 5005 of MIL-STD-883 (All electrical parameters in accordance with the device specification or drawing 1/)
m.	Implementation of test methods	Notify qualifying activity (may involve test demonstration)
n.	Critical documents (see A.4.8.1.3b)	Notify qualifying activity (may involve test demonstration)
o.	Fab move 2/	Group A and C
p.	Assembly move 2/	Group D in accordance with each package family (see A.3.1.3.29) prior to ship
q.	Test facility move 2/	Notify qualifying activity
r.	Scribe/die separation	5 SEM photographs of randomly selected die showing one full edge of die front and back
s.	Qualification/QCI procedures	Notify qualifying activity
t.	Passivation for RHA	Group A, E, C-1, and glass integrity test if current density is over 2 x 10^5
u.	Diffusion profile for RHA	Group A, E, and C-1 deltas (variables only when deltas are required).
v.	Sinter/anneal for RHA	Group A, E, C-1, and B-5
w.	Modification of programming algorithms	Notify qualifying activity
x.	Flip chip devices: Solder bump materials/dimension, Wafer bumping process, Underfill process and materials selection	Notify qualifying activity and document in QM plan/PIDTP (group A, B, C and D as applicable)

1/ Manufacturers shall notify the qualifying activity (QA) of any major changes as listed table A-I herein. Group/subgroup(s) test requirement shall be applicable in accordance with device classes M, N, Q, V, T and Y (class level B and S).

2/ Manufacturer shall notify the qualifying activity (QA) before moving any fabrication, assembly and test facility.

A.3.5.5.1 Metallization thickness. For class level S microcircuits the metallization thickness shall be adequate to satisfy the current density requirements of A.3.5.5.

A.3.5.5.2 Internal wire size and material. For class level S microcircuits, the internal wire diameter shall be 0.001 inch minimum (0.0254 mm) or of sufficient diameter to meet the minimum fusing requirements and bond pull strength requirements with the approval of qualifying activity. The internal lead wire shall be the same metal as the die metallization.

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A.3.5.5.3 Internal lead wires. Internal lead wires or other conductors which are not in thermal contact with a substrate along their entire length (such as wire or ribbon conductors) shall be designed to experience, at maximum rated current, a continuous current for direct current, or a root mean square (RMS) current (peak current divided by $\sqrt{2}$), for alternating or pulsed current, not to exceed the values established by the following relationship:

$$I = Kd^{3/2}$$

Where: I = Maximum allowed current in amperes.
d = Diameter in inches for round wire (or equivalent round wire diameter which would provide the same cross-sectional area for other than round wire internal conductor).
K = A constant taken from TABLE A-IA below for the applicable wire or conductor length and composition used in the device.

TABLE A-IA. Internal lead wires K value.

Composition	"K" values for bond-to-bond total conductor length	
	Length ≤ 0.040 inch (0.10 cm)	Length > 0.040 inch (0.10 cm)
Aluminum	22,000	15,200
Gold	30,000	20,500
Copper	30,000	20,500
Silver	15,000	10,500
All other	9,000	6,300

A.3.5.5.4 Verification of glassivation layer integrity. Where the current density of aluminum metallization for a device type to be qualified exceeds the allowable current density for unglassivated aluminum, the device type shall be subjected to and pass the requirements of TM 2021 of MIL-STD-883 prior to qualification and the glassivation layer integrity sample used along with and a photograph of the etched die shall be documented and maintained. One resubmission is permitted at twice the sample size. Unless otherwise specified by the qualifying activity (QA), the device type shall be tested after sealing (or after exposure to the time/temperature sealing profile) in the package type that receives the highest temperature range during sealing for which the device type is to be qualified. Changes in design, materials, or process, which affect current density or glassivation, shall also be evaluated using TM 2021 of MIL-STD-883. This evaluation applies only when the current density requirements for unglassivated aluminum are exceeded.

A.3.5.6 Package element material and finish.

A.3.5.6.1 Package material. Package body material shall be metal, glass, or ceramic in accordance with A.3.5.1.

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A.3.5.6.2 Lead or terminal material. Lead or terminal material shall conform to one of the following compositions:

a. Type A: Iron-nickel-cobalt alloy: SAE-AMS-I-23011, class I, ASTM F15.
b. Type B: Iron-nickel alloy (41 percent nickel): SAE-AMS-I-23011, class 5, ASTM F30.
c. Type C: Co-fired metallization such as nominally pure tungsten. The composition and application processing of these materials shall be subject to QA approval and submitted with application to test and as otherwise requested by the QA.
d. Type D: Copper-core, iron-nickel ASTM F30 alloy (50.5 percent nickel). The core material shall consist of copper (oxygen-free), ASTM B170, grade 2.
a. Type E: Copper-core ASTM F15 alloy. The core material shall consist of copper (oxygen-free) ASTM B170, grade 2.
f. Type F: Copper (oxygen-free) ASTM B170, grade 2. This material shall not be used as an element of any glass-to-metal seal structure.
g. Type G: Iron-nickel alloy (50.5 percent nickel): SAE-AMS-I-23011, class 2, ASTM F30.
h. Type H: Tin-lead alloy solder balls, bumps or columns for Ball grid array (BGA) and column grid array(CGA) packages.
i. Type J: Tin-lead alloy with copper spiral columns.

A.3.5.6.3 Microcircuit finishes. Finishes of all external leads or terminals and all external metal package elements shall conform to either A.3.5.6.3.2 or A.3.5.6.3.3, as applicable. The use of pure tin, as an underplate or final finish, is prohibited both internally and externally. The tin content of solder shall not exceed 97 percent. Tin shall be alloyed with a minimum of 3 percent lead by weight. However, the use of lead-free solder bumps internal to the device with underfill or encapsulation and mitigated per H.3.4.4.1.2.1 are allowed. Lead-free solder bumps shall have a control plan documented in the PIDTP for QA approval. The lead finish designator (see A.3.6.2.7) shall apply to the finish of the leads or terminals. The leads or terminals shall meet the applicable solderability and corrosion resistance requirements. The other external metallic package elements (including metalized ceramic elements) shall meet the applicable corrosion resistance requirements. Finishes on interior elements (e.g., bonding pads, posts, tabs) shall be such that they meet the lead bonding requirements and applicable design and construction requirements. The use of strike plates is permissible to the maximum thickness of 10 microinches (0.25 micrometer). All plating of finishes and undercoats shall be deposited on clean, nonoxidized metal surfaces. Suitable deoxidation or cleaning operations shall be performed before or between plating processes. All parts shall be capable of meeting the following requirements of MIL-STD-883:

a. Test method 2004, lead integrity, test condition B1, B2, or D, or test method 2028, pin-grid package destructive lead pull test, as applicable.
b. Test method 1009, salt atmosphere.
c. Test method 2003, solderability (plus time/temperature exposure of burn-in except for devices which have been hot solder dipped or have undergone tin fusing after burn-in).
d. Test method 2025, adhesion of lead finish.

Note: Compliance to the above requirements shall be demonstrated when and as specified.

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A.3.5.6.3.1 Finish thickness measurements. Lead finish thickness measurements shall be taken at the seating plane on surface mount leads (such as J-bend and gull-wing type leads) and approximately halfway between the seating plane and the tip of the lead on all round shape lead types. (This requirement is to avoid having the inspector select a non-typical portion of the lead on which to perform the measurement.) On all lead shapes other than round, the finish thickness measurement shall be taken at the crest of major flats. Measurements taken on the shorting bar shall be correlated by direct measurement on the lead. Finish thickness measurements for package elements other than leads shall be taken at the center of major flats. Finish thickness measurements shall be performed in accordance with one of the following procedures:

a. ASTM B487.
b. ASTM B567.
c. ASTM B568.

The aforementioned ASTM methods are provided as reference methods to be used when the failure to pass other finish requirements suggests deficiencies in plating thickness. Compliance to the finish thickness requirements shall be demonstrated when and as specified.

A.3.5.6.3.2 Lead finish. The finish system on all external leads or terminals shall conform to one of the combinations listed in table A-II, and to the thickness and composition requirements of table A-III. The finish system shall also conform to the requirements of A.3.5.6.3.4 and A.3.5.6.3.5, where applicable.

A.3.5.6.3.3 Package element (other than lead or terminal) finish. External metallic package elements other than leads and terminals (e.g., lids, covers, bases, and seal rings) shall meet the applicable environmental requirements without additional finishing of the base materials or else they shall be finished so they meet those requirements using a finish system conforming to one of the combinations listed in table A-IV, and conforming to the thickness and composition requirements of table A-III. The finish system shall also conform to the requirements of A.3.5.6.3.4 and A.3.5.6.3.5, where applicable.

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A.3.5.6.3.4 Hot solder dip. The hot solder dip shall be homogeneous and shall be applied as follows:

a. All outlines with hot solder dip over compliant coating. The hot solder dip shall extend beyond the effective seating plane. If the seating plane is not defined, the hot solder dip shall extend to within 0.040 inch (1.02 mm) of the lead/package interface and is bound by the lead/package interface and shall not touch interface of lead/package body. For dual in line type termination forms (through hole and surface mount), the plane of the two longest lead/package interfaces will define this bound. For leadless chip carrier devices, the hot solder dip shall cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch, except the index feature, if not connected to the castellation. Terminal area intended for device mounting shall be completely covered.

   For top brazed and bottom brazed flat pack packages, the hot solder dip shall be within 0.070 inch (1.78 mm) to the lead/package interface. For all brazed flat pack packages, the solder finish may be on the brazed pad interface area.

b. All outlines with hot solder dip over base metal or noncompliant coating. The solder shall extend to the glass seal or point of emergence of the metallized contact or lead through the package wall. If solder is applied up to the seal, a hermeticity test (TM 1014 of MIL-STD-883, and TABLE IA. footnote 20/ herein shall subsequently be performed and passed. For leadless chip carrier devices, the hot solder dip shall completely cover the metallized side castellation or notch and metallized areas above and below the notch, except the index feature if not connected to the castellation.

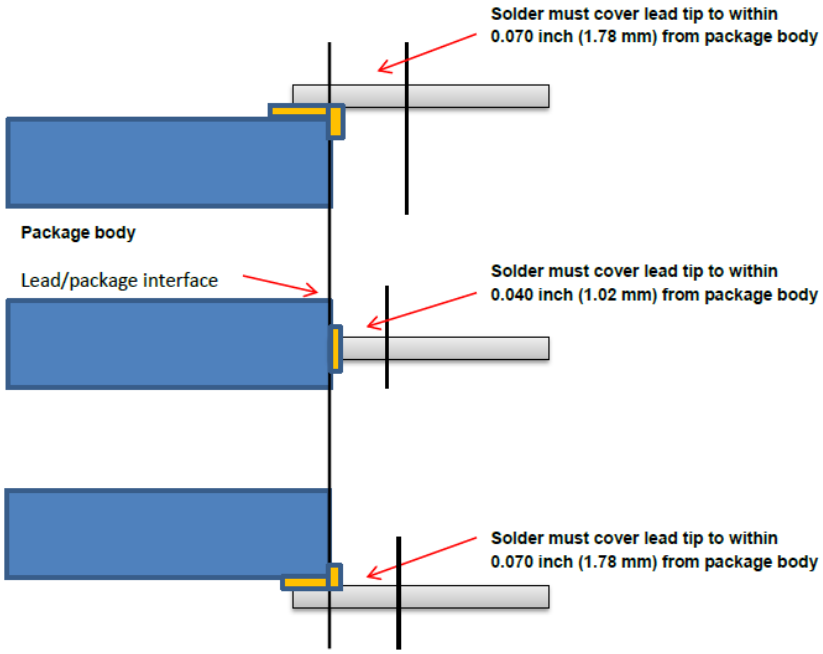

FIGURE A-1. Solder dipping area when seating plane is not defined .

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A.3.5.6.3.5 Tin-lead plate. Tin-lead plate may be fused after plating before or after burn-in by heating above its liquidus temperature. Tin-lead plate shall be visually inspected after fusing and shall exhibit a dense, homogeneous, and continuous coating. The visual inspection after fusing shall be conducted on a sample basis by the manufacturer as an in-process control. Visual inspection of the fusing shall be performed at a frequency sufficient to assure continuous compliance with these requirements on the finished product. The manufacturer shall monitor the tin-lead content of the leads to assure a minimum of 3 percent lead by weight.

A.3.5.7 Die plating and mounting. Pure glass shall not be used for microcircuit die mounting. Metal glass die mounting and Silver Cyanate Ester (see Rome Labs letter 31 May 1994 for guidelines) are acceptable with QA approval. (Contact the preparing activity for the Rome Labs letter.) Electroplated and electroless plated gold backing on dice shall not be used, with the exception of gallium arsenide (GaAs) dice which may use electroplated gold backing.

TABLE A-II. Lead finish systems.

Finish	Applied over	Required underplate		
	Gold plate	Electroplated nickel	Electroless nickel 1/	None
Hot solder dip 2/				X
Hot solder dip 2/		X		
Hot solder dip 2/			X	
Hot solder dip 2/	X	X		
Hot solder dip 2/	X		X	
Tin-lead plate 3/				X
Tin-lead plate 3/		X		
Tin-lead plate 3/			X	
Gold plate		X		
Gold plate			X	
Palladium		X		
Gold flash palladium		X		

1/ Electroless nickel shall not be used as the undercoat on flexible or semi-flexible leads (see 3.3.1 and 3.3.2 of TM 2004 of MIL-STD-883) and shall be permitted only on rigid leads or package elements other than leads.
2/ Hot solder dip shall be applied in accordance with A.3.5.6.3.4.
3/ Fusing of tin-lead plating is permitted in accordance with A.3.5.6.3.5.

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TABLE A-III. Coating thickness and composition requirements.

Coating	Thickness (microinch/micrometer)		Coating composition requirements
	Minimum 1/	Maximum 2/	
Hot solder dip (for all round leads) 3/	60/1.52	NS	The solder bath shall have a nominal composition of Sn60 or Sn63.
Hot solder dip (for all shapes other than round leads which have ≤ 25 mil pitch) 3/	150/3.80	NS	The solder bath shall have a nominal composition of Sn60 or Sn63.
Hot solder dip (for all shapes other than round leads with > 25 mil pitch) 3/	200/5.08	NS	The solder bath shall have a nominal composition of Sn60 or Sn63.
Tin-lead plate (as plated) 4/	300/7.62	NS	Shall consist of 3 to 50 percent by weight lead (balance nominally tin) homogeneously co-deposited. Shall contain no more than 0.05 percent by weight co-deposited organic material measured as elemental carbon. 5/
Tin-lead plate (fused) 4/	200/5.08	NS	
Gold plate	50/1.27	225/5.72	Shall contain a minimum of 99.7 percent gold. 6/
Nickel plate (electroplate)	50/1.27	350/8.89	The introduction of organic addition agents to nickel bath is prohibited. Up to 40 percent by weight cobalt is permitted as a co-deposit.
Nickel plate (electroless)	50/1.27	250/6.35	The introduction of organic additive agents to nickel bath is prohibited.
Nickel cladding	50/1.27	350/8.89	
Palladium	20/0.51	84/2.13	
Gold flash palladium	20/0.51	84/2.13	

1/ Package elements having noncompliant coatings are permitted provided they are subsequently hot solder dipped in accordance with A.3.5.6.3.4b.
2/ NS = Not specified.
3/ See A.3.5.6.3.4.
4/ See A.3.5.6.3.5.
5/ The maximum carbon content (and minimum lead content in tin-lead plate) shall be determined by the manufacturer on at least a weekly basis. The determination of carbon and lead content may be made by any accepted analytical technique (e.g., for carbon: pyrolysis, infrared detection (using an IR212, IR244 infrared detector, or equivalent); for lead: X-ray fluorescence, emission spectroscopy) so long as the assay reflects the actual content in the deposited finish.
6/ Electrodeposited gold plating purity, hardness, and alloy materials shall be in accordance with MIL-DTL-45204, Type III, Grade A.

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TABLE A-IV. Package element (other than leads/terminals) finish systems.

Finish	Applied over	Required underplate			
	Gold plate	Electroplated nickel 1/	Electroless nickel 1/	Nickel cladding 1/	None
Hot solder dip					X
Hot solder dip		X			
Hot solder dip			X		
Hot solder dip				X	
Hot solder dip	X	X			
Hot solder dip	X		X		
Hot solder dip	X			X	
Tin-lead plate 2/					X
Tin-lead plate 2/		X			
Tin-lead plate 2/			X		
Tin-lead plate 2/				X	
Gold plate 3/		X			
Gold plate 3/			X		
Gold plate 3/				X	
Electroplated nickel 1/					X
Electroless nickel 1/					X
Nickel cladding 1/					X
Palladium		X			
Gold flash palladium		X			

1/ Combinations of electroplated nickel and electroless nickel and nickel cladding are permitted.
2/ Fusing of tin-lead plate is permitted in accordance with A.3.5.6.3.5.
3/ Multilayer gold and nickel finish structures are acceptable provided the outer gold layer meets a minimum thickness of 25 microinches (0.635 micrometer), the total of the gold layers meet a minimum thickness of 50 microinches (1.27 micrometers), and each of the nickel undercoats meet the thickness requirements of table A-III with the total nickel thickness not to exceed 450 microinches (11.43 micrometers). For multilayer finish structures, nickel plate, nickel cladding, or gold plate are permitted on the base metal.

A.3.5.8 Glassivation. All microcircuits shall be coated with a transparent glass or other approved coating, except where glassivation is omitted by documented design rules (e.g., probe opening, fuse pads, etc.) The minimum glassivation thickness shall be 6,000 Å (600 nm) for $Si0_2$, 2,000 Å (200 nm) for Si_3N_4, or approved thicknesses for approved coatings. The composition and minimum thickness of other approved coatings are subject to approval by the QA, and must be included in the manufacturer's QM plan. The glassivation/nitridation shall cover all electrical conductors except the bonding or test pads. NOTE: For GaAs microwave microcircuits, the glassivation or nitride dielectric shall cover the semiconductor regions (e.g., field effect transistor (FET)) of the device and planar thin film resistors as a minimum. Furthermore; for class level S devices, the glassivation or nitride dielectric shall cover regions where conductors are separated by less than the minimum 1 mil particle size detectable by a PIND test. For RF/microwave GaAs microcircuits, the manufacturer shall define appropriate glassivation thickness requirements for the technology in the internal baseline documentation.

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A.3.5.9 Die thickness. Appropriate die thickness requirements for each product or process shall be defined in the manufacturer's baseline documentation. This thickness shall be sufficient to avoid die cracks due to handling, die attach, wire bonding or other process stresses, which could lead to latent field failure.

A.3.5.10 Laser scribing. Laser scribing may be used for wafer grooving before using traditional diamond saw for die separation, or for full grooving for die separation. If the manufacturer uses laser scribing for die grooving, the applicable inspections shall be performed for checking damage in the die active region and seal ring. Laser trim of resistors and shorting bars and laser scribed package external markings are not prohibited unless otherwise specified.

A.3.5.11 Internal lead separation for class level S devices. For class level S devices, the minimum separation of the internal leads (excluding conductors which are at the die or substrate potential) from the unglassivated surface of the die shall be a minimum of 1.0 mil. This design requirement shall be verified during design verification, qualification and during group B internal visual and mechanical tests in accordance with TM 5005 of MIL-STD-883.

A.3.6 Marking of microcircuits. Marking shall be in accordance with the requirements of this appendix, and the identification and marking provisions of the device specification or drawing. The marking shall be legible and complete, and shall meet the resistance to solvents requirements of TM 2015 of MIL-STD-883. When laser marking is performed, it shall be clearly visible through those conformal coatings approved for use in MIL-I-46058, (see TM 2015 of MIL-STD-883 if contrasting material or ink is used to highlight the trace). Laser marked metal surfaces shall have been submitted to and passed all group D test requirements. If any special marking is used, it shall in no way interfere with the marking required herein, and shall be visibly separated from the required marking. The following marking shall be placed on each microcircuit. If any special marking (e.g., altered item drawing number) is used by the device supplier or user/equipment contractor, it shall be in addition to the existing/original marking as required herein and shall be visibly separate from, and in no way interfere with, the marking required herein. The following shall be placed on each microcircuit:

a. Index point (see A.3.6.1).

b. PIN (see A.3.6.2).

c. Identification codes (see A.3.6.3).

d. Manufacturer's identification (see A.3.6.4 and A.3.6.5).

e. Country of origin (see A.3.6.6).

f. Compliance indicators (see A.3.6.7).

g. Serialization, when applicable (see A.3.6.8).

h. Special marking (see A.3.6.9, A.3.6.9.1).

i. Electrostatic discharge (ESD) sensitivity identifier, if applicable (see A.3.6.9.2).

NOTE: All devices shall be marked by the manufacturer in such a manner as to leave space for additional unique marking (assigned and applied by the user or called out in the order or contract).

A.3.6.1 Index point. The index point, tab, or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified (see MIL-STD-1835) and shall be designed so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline or solid equilateral triangle(s) (Δ) which may be used as an electrostatic identifier (see A.3.6.9.2), may also be used as the pin 1 identifier.

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A.3.6.2 PIN. Each microcircuit shall be marked with the complete PIN. The PIN may be marked on more than one line provided the PIN is continuous except where it "breaks" from one line to another. The PIN system shall be as described in 3.6.2a and 3.6.2b for microcircuits produced in accordance with this appendix and either an SMD, or device specification. For devices produced in accordance with this appendix, which are not documented on SMDs, the PIN shall be the vendor's generic part number or the contractor's part number as applicable.

A.3.6.2.1 Military designator. Any device that does not meet all the requirements of this appendix and the applicable device specification, except as allowed by H.3.3, shall not be marked M38510 and shall not make reference to MIL-M-38510 or MIL-PRF-38535.

A.3.6.2.2 RHA designator. A "/" or "-" indicates no radiation hardness assurance. Letters M, D, P, L, R, F, G, or H designator levels are defined in A.3.4.1.3.

A.3.6.2.3 Device specification. When used in association with this specification or appendix (e.g., QML), the M38510 device specification shall consist of three digits from 001 to 999 as applicable.

A.3.6.2.4 Device type. The device type number shall be as specified in the device specification or SMD. The numbers shall consist of two digits assigned sequentially, from 01 to 99, within each device specification or SMD.

A.3.6.2.5 Device class. The device class shall be designated by a single letter identifying the quality assurance level. For devices built compliant to this appendix and documented on a one part-one part number SMD, the device class designator shall be an 'M'.

A.3.6.2.6 Case outline. The case outline shall be designated by a single letter assigned to each outline.

A.3.6.2.7 Lead finish. Lead frame or terminal material and finish shall be as specified in A.3.5.6. The lead finish shall be designated by a single letter in table A-V.

TABLE A-V. Lead finish.

Lead finish letter	Lead frame or terminal material and finish (see note below)
A	Types A, B, C, D, E, F, or G with hot solder dip
B	Types A, B, C, D, E, F, or G with tin-lead plate
C	Types A, B, C, D, E, F, or G with gold plate
D	Types A, B, C, D, E, F, or G with palladium
E	Types A, B, C, D, E, F, or G with gold flash palladium
F	Types H, J with tin-lead alloy as applicable to BGA and CGA device document.
X	Types A, B, C, D, E, F or G with finishes A, B, or C (see note below)

NOTE: Finish letter "X" shall not be marked on the microcircuit or its packaging. This designation is provided for use in drawings, part lists, orders, or other documentation where lead finishes A, B, or C are all considered acceptable and interchangeable without preference. For Government logistic support, the A lead finish shall be acquired and supplied to the end user when the X is included in the PIN for lead finish. If the PIN is not available with the A lead finish, the same PIN shall be acquired except with the B or C lead finish designator as determined by availability. Type C terminal material is a fired on metallization used with leadless chip carriers.

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A.3.6.2.8 Drawing designator. For new one part-one part number drawings without existing device specifications, the first two characters of the drawing designator shall consist of the last two digits of the year and the last three characters shall consist of unique characters assigned to the drawing by DLA Land and Maritime. When an existing MIL-M-38510 device specification PIN is converted to a one part-one part number PIN via a substitution statement, the first two characters of the drawing designator of the one part-one part number shall be replaced with the first two digits of MIL-M-38510 (e.g., 38), and the last three characters of the one part-one part number shall be replaced with the three digit identifier assigned to the device specification (e.g., M38510/00101BAC shall become 5962-3800101BAC).

A.3.6.3 Identification codes. Identification codes shall be as follows:

A.3.6.3.1 Class level B die fabrication date code. Class level B microcircuits may be marked with a unique code to identify the year and quarter in which the die fabrication was started (or completed at the manufacturer's predesignated option). The first character of the code shall be the last digit of the year in which die fabrication started (or completed at the manufacturer's predesignated option). The second character of the code shall be a letter (A, B, C, or D) respectively designating the first quarter (weeks 1 - 13), the second quarter (weeks 14 - 26), third quarter (weeks 27 - 39), or fourth quarter (weeks 40 - 52 or 53) of the calendar year of die fabrication.

A.3.6.3.2 Inspection lot identification code for class levels S and B. Microcircuits shall be marked with a unique code to identify the inspection lot (see A.3.1.3.6 and A.3.1.3.7) and identify the first or the last week of the period (6 weeks maximum) during which devices in that inspection lot were sealed. At the option of the manufacturer, the actual week of seal may be used. The first two numbers in the code shall be the last two digits of the number of the year, and the third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the year and week, in that order. When two or more different inspection lots (or class level S sublots), each having the same part number, are to be marked with the same identification code, a unique suffix letter representing each additional inspection lot (or class level S sublot) shall appear immediately following the identification code except the unique suffix letter may be omitted when an alternate lot identifier is used which maintains the unique traceability required. Once assigned, the inspection lot identification code shall not be changed.

NOTE: These die fabrication date codes may be combined with the inspection lot identification code as shown:

FAB YR	FAB QTR	ASSY YR	ASSY WK	Unique suffix
6	B	87	10	A
1986	2nd qtr	1987	10	First lot

A.3.6.4 Manufacturer's identification. Microcircuits shall be marked with the name or trademark of the manufacturer. The identification of the equipment manufacturer may appear on the microcircuit only if the equipment manufacturer is also the microcircuit manufacturer.

A.3.6.5 Manufacturer's designating symbol. The microcircuit manufacturer's designating symbol or CAGE code may also be marked on each device in addition to the manufacturer's identification. If the microcircuit manufacturer's designating symbol or CAGE code number is marked, it shall be as assigned by the Defense Logistics Information Service (DLIS). The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at that manufacturer's plant. In the case of small microcircuits, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

A.3.6.6 Country of origin. The identifier of the country in which assembly is performed shall be marked on all devices supplied under this appendix. If abbreviations are used, a cross reference should be published in the manufacturer's data books or catalogs.

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A.3.6.7 Compliance indicator/certification mark. The compliance indicator "C" shall be marked on all devices built in compliance to this appendix. The “D” certification mark shall be used for diminishing manufacturing sources (DMS) product using the alternate die/fab requirements (see A.3.2.2) in lieu of the “C” certification mark for product built to this appendix. The compliance indicator "C" shall be replaced with a "Q" or "QML" certification mark or the "Q" or "QML" certification mark added when product is built to a QML process (see A.3.1). The "J" or "JAN" certification mark may not be used on devices built in compliance to this appendix.

A.3.6.8 Serialization. Prior to the first recorded electrical measurement in screening each class level S microcircuit, and when specified, each class level B microcircuit shall be marked with a unique serial number assigned consecutively within the inspection lot. This serial number allows traceability of test results down to the level of the individual microcircuit within that inspection lot. For class level S, inspection lot records shall be maintained to provide traceability from the serial number to the specific wafer lot from which the devices originated.

A.3.6.9 Marking location and sequence. The certification mark, the PIN, identification codes and ESD identifier shall be located on the top surface of leadless or leaded chip carriers, pin grid array packages, flat packages, or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations). When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the backside of the package may be used for these markings except the ESD identifier, if marked, shall be marked on the top. Button cap flat packs with less than or equal to 16 leads may have the identifier marked on the ceramic. Backside marking with conductive or resistive ink shall be prohibited.

A.3.6.9.1 Beryllium oxide package identifier. If a microcircuit package contains beryllium oxide (see A.3.5.1 note), the part shall be marked with the designation "Be0".

A.3.6.9.2 Electrostatic discharge (ESD) sensitivity identifier. Microcircuits shall be ESD classified in accordance with A.3.4.1.4, however, ESD classification marking is not required. The manufacturer shall have an option of no ESD marking, marking a single ESD triangle symbol or marking in accordance with the ESD device classification defined in test method 3015 of MIL-STD-883. Because it may no longer be possible to determine the ESD classification from the part marking, the device Discharge Sensitivity Classification shall be as listed in MIL-HDBK-103 or QML-38535 or can be found from DLA Land and Maritime web link “ standard microcircuits cross reference (SMCR)”. If manufacturer is using the HBM or CDM or both method for ESD classification, it shall be reported in the device specification or standard microcircuit drawing (SMD) devices certificate of compliance (CofC).

A.3.6.10 Marking on container. See A.5.2.2 for additional marking requirements.

A.3.6.11 Marking option for controlled storage of class level B. Where microcircuits are subjected to testing and screening in accordance with some portion of the quality assurance requirements and stored in controlled storage areas pending receipt of orders requiring conformance to the same or a different level, the inspection lot identification code shall be placed on the microcircuit package along with the other markings specified in 3.6 sufficient to assure identification of the material. As an alternative, if the microcircuits are stored together with sufficient data to assure traceability to processing and inspection records, all markings may be applied after completion of all inspections to the specified level.

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A.3.6.12 Marking option for qualification or quality conformance inspection (QCI). The manufacturer has the option of marking the entire lot or only the sample devices to be submitted to qualification or groups B, C, and D (and E if applicable) QCI, as applicable. If the manufacturer exercises the option to mark only the sample devices, the procedures shall be as follows:

a. The sample devices shall be marked prior to performance of groups B, C, and D (and E if applicable) qualification or QCIs, as applicable.

b. At the completion of inspection, the marking of the sample devices shall be inspected for conformance with the requirements of A.3.6.

c. The inspection lot represented by the conforming qualification or quality conformance sample shall then be marked and any specified visual and mechanical inspection performed.

d. The marking materials and processing applied to the inspection lot shall be to the same specifications as those used for the inspection sample.

A.3.6.13 Remarking. If sealed devices are remarked (to change or correct the marking as specified in A.3.6), the reason for remarking, and a description of the process shall be recorded in the qualification test report and quality conformance test record. In addition to the tests described below for qualification of the remarking procedure, subgroup B-2 and internal visual and mechanical tests (TM 2014 of MIL-STD-883 with sample size/(accept no.) of 1(0) for class B devices and subgroups B-2a and B-2b (TM 2014 of MIL-STD-883 only) for class level S devices shall be performed on each remarked lot to assure marking permanency and that markings and device type coincide. An appropriate group A test, with a sample size/(accept no.) of 116(0), (100 percent for class level S) may be performed, in lieu of internal visual and mechanical tests, to demonstrate that the markings and device types coincide. Remarking procedures shall be approved by the qualifying activity. Approval shall be required once only for each package material (e.g., lid, base) composition (regardless of package configuration), or at change of remarking procedures or materials. For qualification of the remarking procedure, a sample of remarked devices shall be tested to the following test methods according to TM 5005 of MIL-STD-883:

a. TM 2015, resistance to solvents (3 devices).

b. TM 1011, thermal shock (test condition B, 15 cycles minimum).

c. TM 1004, moisture resistance.

d. TM 1009, salt atmosphere.

NOTE: Electrical tests are not required. Visual inspection, after each test in accordance with applicable failure criteria, shall be conducted.

A.3.7 Workmanship. Microcircuits shall be manufactured, processed, and tested in a careful and workmanlike manner in accordance with good engineering practice, with the requirements of this appendix, and with the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the quality assurance program (see A.4.8 herein).

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A.3.7.1 Rework provisions. All rework (see A.3.1.3.15) permitted on microcircuits acquired under this appendix shall be accomplished in accordance with procedures and safeguards documented in accordance with A.4.8.1.1.6 and available for review by the preparing and acquiring activity. In addition, all rework operations shall be clearly identified on each process flowchart. Allowable rework of sealed packages includes recleaning of any microcircuit or portion thereof, any rebranding (see A.3.6.13) to correct defective marking and lead straightening (provided the reworked devices meet the requirements of A.4.6.2 for conditions of leads). For monolithic wafers of any class, the strip and redeposition of a layer or additional processing to correct a nonconformance to a specification limit is not allowed, except for the strip and redeposition of sacrificial layer(s) used exclusively as a masking function (e.g., photoresist, nitride, nitride glass). Documenting rework of these sacrificial layers on the flow chart is not required. Continuation of processing is permitted and is considered allowable rework provided the manufacturer assures, through evaluation, that no alteration in material film properties occurs (e.g. oxidation, corrosion, grain size, film stress, adhesion) and baselined limits are met. Manufacturer shall document rework/continuation process work. The strip and redeposition of backside metallization is considered allowable rework. No delidding or package opening for rework shall be permitted for microcircuits of any class. For monolithic microcircuit wafers of any class, the strip and redeposition of a layer or additional processing to correct a nonconformance to a specification limit is not allowed, except as specified above. For class level S, any assembly rework operation prior to package seal is not allowed, except as specified in A.3.7.1.1. Other than already stated in the rework provisions above, rework is not allowed for class level S product without substantiating data and written approval of the qualifying activity.

A.3.7.1.1 Rebonding of monolithic devices. Visual criteria for rebonding and rebonding limitations for class level B monolithic microcircuits shall be in accordance with TM 2010, Internal Visual (Monolithic), of MIL-STD-883, (see 3.2.1.4i and 3.2.1.5 of TM 2010 of MIL-STD-883). For class level S devices, rebonding is not allowed without substantiating data and written approval of the qualifying activity. Rebonding of class level B shall be limited to the bonding operation only.

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A.4 VERIFICATION

A.4.1 Responsibility for inspection. Unless otherwise specified in the contract or order, the contractor is responsible for the performance of all inspection requirements as specified herein and in the device specification or drawing.

A.4.1.1 Inspection during manufacture. The manufacturer shall establish and maintain in-process production controls, quality controls and inspections at appropriately located points in the manufacturing process in accordance with the procedures described in A.4.8.1.1 to assure continuous control of quality of materials, subunits, and parts during manufacture and testing. These controls and inspections shall be adequate to assure compliance with the applicable acquisition documentation and quality standards of microcircuits manufactured to this appendix and the applicable device specification or drawing.

A.4.1.1.1 Metal package isolation test for class level S devices. Prior to die mounting, each metal-bodied package with leads glass-isolated within .005 inch (0.13 mm) of the metal body shall have 600 V dc applied between the case and leads not connected to the case. Packages which exhibit leakage greater than 100 nA shall be rejected.

A.4.1.2 Control and inspection of acquisition sources. The manufacturer shall be responsible for assuring that all supplies and services used in the manufacture and test of microcircuits conform to all the requirements of this appendix, the device specification or drawing, and other provisions of the applicable acquisition documentation.

A.4.1.3 Control and inspection records. The manufacturer shall maintain objective evidence documenting that each lot has been subjected to all processing controls, inspections, and tests accomplished in accordance with A.3 and A.4 herein. Records shall be retained as specified in A.4.8.1.2.

A.4.1.4 Government source inspection (GSI). Source inspection (GSI and contractor source inspection (CSI)) shall be required only when specified in the order or subcontract. Notification of test initiation shall be given to the acquiring activity.

A.4.1.5 Manufacturer control over its distributors. The manufacturer shall be responsible for assuring that its distributors maintain adequate controls to assure that products sold are of the same quality as products acquired directly from the manufacturer.

A.4.1.6 Distributor inventory, traceability and handling control. Distributors shall, as a minimum, maintain adequate inventory control system, traceability documentation required by this specification and their appropriate certification, adequate handling, storage, and repackaging methods to protect quality and prevent damage and degradation of products.

A.4.2 Solderability. All parts shall be capable of passing the solderability tests in accordance with TM 2003 of MIL-STD-883, on delivery.

A.4.3 General inspection conditions. The general requirements of MIL-STD-883 shall apply.

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A.4.3.1 Classification of inspections and tests. The inspections and tests required to assure conformance to the specified quality assurance levels of microcircuits or lots thereof are classified as follows:

Requirement	Paragraph
Qualification procedures	A.4.4
Quality conformance inspection	A.4.5
Screening	A.4.6
Test results	A.4.7
Quality Assurance Program	A.4.8

A.4.3.2 Sampling. Statistical sampling for qualification and quality conformance inspections (QCIs) shall be in accordance with the sampling procedures of APPENDIX D of this specification, and as specified in the device specification or drawing, as applicable. Reserve sample devices may be tested with the subgroups to provide replacements in the case of test equipment failure or operator error (see A.4.3.5 and A.4.4.2.1.1). These devices shall be used in predesignated order. Initial samples (and added samples, when applicable) shall be randomly selected from the inspection lot or sublot, as applicable. After a test has started, the manufacturer may add an additional quantity to the initial sample, but this may be done only once for any subgroup with a specified sample size number (accept number). Add-on samples are not allowed for fixed sample size subgroups or for resubmitted lots. The added samples shall be subjected to all the tests within the subgroup. The total samples (initial and added samples) shall determine the new acceptance number. The total defectives of the initial and second sample shall be additive and shall comply with the specified sample size number (accept number). The manufacturer shall retain sufficient microcircuits from the lot to provide for additional samples.

A.4.3.2.1 Disposal of samples. Devices subjected to destructive tests or which fail any test shall not be shipped on the contract or order as acceptable product. They may, however, be delivered at the request of the acquiring activity if they are isolated from, and clearly identified so as to prevent their being mistaken for acceptable product. Sample microcircuits, from lots which have passed quality assurance inspections or tests and which have been subjected to mechanical or environmental tests specified in groups B, C, and D inspection and not classified as destructive, may be shipped on the contract or order provided the test has been proved to be nondestructive (see A.4.3.2.3) and each of the microcircuits subsequently passes final electrical tests in accordance with the applicable device specification.

A.4.3.2.2 Destructive tests. The following MIL-STD-883 tests, or other test as specified, shall be classified as destructive:

Internal visual and mechanical (TM 2014).
Bond strength.
Solderability (for lead finishes B and C).
Moisture resistance.
Lead integrity.
Salt atmosphere.
SEM inspection for metallization.
Steady-state life test (accelerated).
Die shear strength test.
Total dose radiation hardness test.
Neutron irradiation.
Electrostatic discharge (ESD) sensitivity classification test.
Lid torque test.
Adhesion of lead finish.
Vibration, variable frequency.
Internal gas analysis (IGA) test.
Single-event-effects (ASTM F1192 or JESD57)
Dose-Rate Upset
Solder column pull test (TM 2038)

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All other mechanical or environmental tests (other than those listed in A.4.3.2.3), shall be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified test on the same sample of product, without evidence of cumulative degradation or failure to pass the specified test requirements in any microcircuit in the sample, is considered sufficient evidence that the test is nondestructive. Any test specified as a 100 percent screen shall be considered nondestructive for the stress level and duration or number of cycles applied as a screen.

A.4.3.2.3 Nondestructive tests. The following tests are classified as nondestructive:

Barometric pressure
** Steady-state life
** Intermittent life
*** Solderability (for lead finish A only)
Seal
External visual
Internal visual (pre-cap)
** Burn-in screen
Radiography
Particle impact noise detection (PIND)
Physical dimensions
Nondestructive 100 percent bond pull test where stress does not exceed the specified pull force and positive tolerance
Resistance to solvents
SAM (TM 2030)

** When the test temperature exceeds the maximum specified junction temperature for the device (including maximum specified for operation or test), these tests may be considered destructive. To ship these tested devices, the manufacturer shall have data to support that the test is not destructive and has not degraded the device.

*** For glass sealed devices, lead finish A shall be considered nondestructive unless electrical test, visual inspection, or other evaluation shows that package integrity or electrical performance has been degraded.

A.4.3.3 Formation of lots. Microcircuits shall be segregated into identifiable production lots as defined in A.3.1.3.5 as required to meet the production control and inspection requirements of A.4.8. Microcircuits shall be formed into inspection lots as defined in A.3.1.3.6 and A.3.1.3.7 as required to meet the quality assurance inspection and test requirements of this specification.

Wafer lot processing, as a homogeneous group (see A.3.1.3.10), shall be accomplished by any of the following procedures, providing process schedules and controls are sufficiently maintained to assure identical processing in accordance with process instructions of all wafers in the lot:

a. Batch processing of all wafers in the wafer lot through the same machine process step(s) simultaneously.

b. Continuous or sequential processing (wafer by wafer or batch portions of wafer lot) of all wafers through the same machine or process step(s).

c. Parallel processing of portions of the wafer lot through multiple machines or process stations on the same certified line, provided statistical quality control assures and demonstrates correlation between stations and separately processed portions of the wafer lot.

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A.4.3.3.1 Resubmission of failed lots. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. When any lot submitted for qualification or quality conformance inspection fails any subgroup requirement of group B, C, or D (and E if applicable) tests, it may be resubmitted once for that particular subgroup using tightened inspection criteria (as defined in D.4.2). Resubmission for group A inspection failure is not permitted. In case of group B, subgroup B-2a failure, the entire lot may be remarked as defined in A.3.6.13. The remarked lot shall not be acceptable for alternate group B (class level B only) coverage of a standard lot (see A.4.5.8.2 for recovery). For fixed sample size subgroups, lots may be resubmitted one time only at double the sample size with zero failures allowed. All submissions shall be subject to the sampling requirements of A.4.3.2. A second resubmission (class level S lots shall be resubmitted one time only) using a second tightened inspection criteria is permitted only if failure analysis is performed to determine the mechanism of failure for each failed microcircuit from the prior submissions and it is determined that failure(s) is (are) due to:

a. A defect that can be effectively removed by rescreening or reworking the entire lot (see A.3.7.1).
b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault or non-screenable defects, the lot shall not be resubmitted.

A.4.3.4 Test method deviation. Deviations from test methods or test circuits specified are allowed provided that it is demonstrated to the preparing activity that such deviations in no way relax the requirements of this appendix and that they are approved by the preparing activity before testing is performed. The preparing activity shall be notified by the device manufacturer of any proposed test method deviation. For proposed electrical test deviations, schematic wiring diagrams of the test equipment shall be made available for review.

A.4.3.5 Procedure in case of test equipment failure or operator error. Whenever a microcircuit is believed to have failed as a result of faulty test equipment or operator error, unless otherwise specified in the test method, the failure shall be entered in the test record which shall be retained for review along with a complete explanation verifying why the failure is believed to be invalid.

NOTE: ESD failures shall be counted as rejects and not be attributed to equipment/operator error for screening, group A, and end-point electrical tests of TM 5005 of MIL-STD-883.

A.4.3.5.1 Procedure for sample tests. When it has been established that a failure is due to test equipment failure or operator error and it has been established that the product has not been damaged or degraded, a replacement microcircuit from the same inspection lot may be added to the sample. The replacement microcircuit shall be subjected to all those tests to which the discarded microcircuit was subjected prior to its failure and to any remaining specified tests to which the discarded microcircuit was not subjected prior to its failure. The manufacturer, at their own risk, has the option of replacing the failed microcircuit and continuing with the tests before the validity of the test equipment failure or operator error has been established.

A.4.3.5.2 Procedure for screening tests. When it has been established that lot failure(s) during screening test(s) are due to operator or equipment error and it has been established that the remaining product has not been damaged or degraded, the lot or surviving portion of the lot, as the case may be, may be resubmitted to the corrected screening tests(s) in which the error occurred. Failures verified as having been caused by test equipment failure or operator error shall not be counted in the PDA calculation (when applicable).

A.4.3.5.3 Failure and corrective action reports. When the procedures of A.4.3.5.1 and A.4.3.5.2 are utilized in continuing sample tests or resubmitting lots for screening tests, the manufacturer shall document the results of their failure investigations and corrective actions and shall make this information available to the Government Quality Assurance Representative (QAR), the acquiring activity, or the qualifying activity, as applicable.

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A.4.3.6 Electrical test equipment verification. The manufacturer shall verify the measurement/operation characteristics of the electrical test equipment in accordance with 4.5 of MIL-STD-883.

A.4.3.7 Manufacturer imposed tests. Any manufacturer imposed test(s) (e.g., gross and fine leak) which exceed the minimum class level B requirements herein shall be documented on the manufacturer's process baseline. If any manufacturer imposed test(s) detects a problem, the manufacturer shall submit all devices in the lot to those tests to eliminate rejects and shall take steps to determine and eliminate the cause of failure (e.g., rough handling which has produced gross leaks).

A.4.4 Qualification procedures.

A.4.4.1 General. The manufacturer shall perform sufficient qualification inspection to assure that the devices supplied to this appendix meet the minimum class level B or S performance requirements as defined herein. Qualification to a given quality assurance level qualifies the product for all lower quality assurance levels provided the product for all levels is manufactured on the same line and meets all the requirements of the lower level.

A.4.4.2 Qualification. A manufacturer shall qualify individual devices by subjecting them to, or assuring that, they satisfy all the groups A, B, C, and D (and E if applicable) requirements as specified herein or TM 5005 or TM 5010, as applicable of MIL-STD-883 for the specified device class and type of microcircuits. A.4.4.2.1 through A.4.4.2.7 herein should be used as guidelines.

A.4.4.2.1 Inspection routine. Except where the use of electrical rejects is allowed, all microcircuits subjected to groups B, C, and D (and E if applicable) tests shall have previously been subjected to and passed all tests of group A inspection specified as end-point electrical parameters. The microcircuits should then be divided into the subgroups for groups B, C, and D (and E if applicable) inspection. When necessary to meet subsequent sample requirements, all failures found in the course of group A inspection shall be replaced by microcircuits which have passed group A tests prior to subjection to group B, C, or D (and E if applicable) tests. All tests shall be applied to and all acceptance criteria referenced to the entire lot or sublot as applicable, not to an arbitrary quantity of devices tested.

A.4.4.2.1.1 Sample. The number of microcircuits to be tested shall be chosen (independent of lot size) by the manufacturer and should be adequate to demonstrate conformance to the inspection criteria for each subgroup of groups A, B, C, and D (and E if applicable) inspection. All qualification test samples for subgroups which require variables data should be serialized prior to qualification tests.

A.4.4.2.2 Group A electrical testing. The parameters, conditions of test, and limits for group A testing shall be as specified in Table III herein or test method 5005 of MIL-STD-883 and the applicable device specification or drawing. Group A testing may be performed in any order. If an inspection lot is made up of a collection of splits or class level S inspection sublot, each split or class level S inspection sublot should pass group A inspection as specified.

A.4.4.2.3 Group B testing. Group B tests should be as specified in Table II herein or TM 5005 of MIL-STD-883.

A.4.4.2.4 Groups C and D testing. Groups C and D tests shall be as specified in Table IV and Table V herein or TM 5005 of MIL-STD-883.

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A.4.4.2.5 Group E testing. Group E tests shall be conducted as specified in Table C-I herein or TM 5005 of MIL-STD-883. Group E is required for initial qualification and after process or design changes that may affect radiation hardness (see A.3.4.2). Qualification for RHA shall be for a specific microcircuit die and package type, except as authorized by the qualifying activity. Microcircuits which pass the quality assurance and RHA requirements to a higher reliability or RHA level shall be acceptable to a lower level or as non-RHA parts if all other applicable requirements and pre- and post irradiation electrical parametric and timing limits are met.

A.4.4.2.6 Approval of other lead finishes. After qualification of one package type with a single lead finish, other lead finishes may be approved by submitting a single device type for each additional lead finish in the previously approved package family to group B, subgroup 3 and group D, subgroups 1, 3, 5, and 7 tests. Subgroup D-7 testing should not be required for hot solder dip over lead finishes B or C (tin-lead, gold plate) which have been qualified on the same package family.

A.4.4.2.7 Approval of other lead material. After the first lead material is qualified with a particular package family, the new lead material for the package family can be considered qualified provided the required lead finish tests specified (see A.4.4.2.6) with the addition of subgroup D-2, are successfully performed. Subgroup D-6 should be completed when the lead frame extends into the die cavity.

A.4.4.2.8 Electrostatic discharge (ESD) sensitivity. ESD sensitivity testing shall be performed in accordance with TM 3015 of MIL-STD-883 and the device specification. The testing procedure defined within ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) may be used as an option in lieu of TM 3015 for applicable devices (e.g. high pin count devices wherein parasitic charge may effect ESD failures). However, manufacturers shall document such ESD testing procedure in the QM plan that require QA approval. The reported ESD sensitivity classification levels shall be documented in the device specification (see 3.6.7.2). In addition, unless otherwise specified, Human Body Model (HBM) and Charge Device Model (CDM) tests shall be performed for initial qualification and product redesign as applicable. If manufacturer is using the HBM or CDM or both method for ESD classification, it shall be reported in the device specification or standard microcircuit drawing (SMD) devices certificate of compliance (CofC).

A.4.5 Quality conformance inspection (QCI).

A.4.5.1 General. Quality conformance inspection shall be conducted in accordance with the applicable requirements of groups A, B, C, and D (and E if applicable) as specified herein or TM 5005 (or TM 5010 when applicable) of MIL-STD-883, for the specified device class and TM 5007 of MIL-STD-883, when applicable. Inspection lot sampling shall be in accordance with APPENDIX D of this specification. Test results shall be recorded by inspection lot identification code (see A.3.6.3) for each inspection lot.

A.4.5.2 Group A inspection. Group A inspection shall be performed on each inspection lot in accordance with MIL-STD-883 and shall consist of electrical parameter tests specified for the specified device class. If an inspection lot is made up of a collection of class level B splits or class level S inspection sublots, it shall be recombined into an inspection lot before the group A inspection sample is taken or a group A inspection sample shall be taken from each split or class level S inspection sublot.

A.4.5.3 Group B inspection. Group B inspection shall be performed in accordance with MIL-STD-883 on each inspection lot for each package type and lead finish. As an alternate, except for class level S (at the manufacturer's option) group B inspection may be performed on each package type and lead finish in accordance with 3.5.2 of TM 5005 or 3.4.2.1 of TM 5010 of MIL-STD-883. For class level S, group B, subgroups 1A, 2, 3, and 4 inspections shall be performed on each sublot (split) when the manufacturer elects to keep the sublots (splits) separate from each other after screen tests are completed. Except as otherwise specified in TM 5005 of MIL-STD-883, samples for this inspection shall be completed and fully marked devices from lots which have been subjected to and passed the post burn-in +25°C final electrical static tests (subgroup 1). Class level S steady-state life test, subgroup B-5, results shall not be used to support class level B shipments.

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A.4.5.4 Group C inspection for class level B only. Group C inspection (die-related tests) shall be in accordance with MIL-STD-883 and shall include those tests specified which are performed periodically. Group C shall have been completed on product with a die fabrication date code within four calendar quarters prior to the die fabrication date code of product being submitted for acceptance. Group C tests are required for devices from each microcircuit group (see A.3.1.3.12) in which a manufacturer is supplying product. Group C tests for each microcircuit group shall be performed on one inspection lot of the most complex device type available at the time of selection from production devices produced on each certified die fabrication line once per calendar year.

A.4.5.4.1 Group C sample selection. Samples selected for group C inspection shall meet all of the following requirements:

a. Shall be chosen at random from any inspection lot comprised only of die from the quarter of the year (see A.3.6.3.1) for which quality conformance inspection is being established in a particular microcircuit group (see A.3.1.3.12 and tables A-VI, A-VII, A-VIII, and A-IX) for each certified die fabrication line.

b. Shall be chosen from an inspection lot that has been submitted to and passed group A quality conformance inspection (QCI) (regardless of whether that inspection lot has been submitted and passed group B QCI).

c. The inspection lot from which the samples are selected shall be the one with the most complex device type available at the time of selection.

d. On multichip microcircuits, the group C die fabrication date code requirement shall be determined by considering only the latest date code of the most complex die contained within the package.

A.4.5.4.1.1 Microcircuit group assignments. Microcircuits group assignments and technologies/die family assignments shall be as specified in tables A-VI, A-VII, A-VIII, A-IX, and A.3.1.3.12. Microcircuit groups shall be structured such that they appropriately group all of the devices produced by the manufacturer, including those that do not coincide with any of the current microcircuit groups listed. In the tables, each number represents a different microcircuit group. Each letter in the top row of the table represents a different technology group. Each table entry in the line below the technologies (e.g., Standard TTL, Schottky TTL, CMOS, etc.) represent a separate die family (e.g., 93, 93H, LS, etc).

A.4.5.4.1.2 Product acceptable for delivery. Product shall be acceptable for delivery only after the successful completion of all group C testing and shall be comprised of die meeting the following requirements:

a. Manufactured on the same die fabrication line as the sample selected for A.4.5.4.1.

b. In the same microcircuit grouping as the sample selected in A.4.5.4.1.

c. Which was started (or completed, at the manufacturer's pre-designated option) within the same year the sample selected in A.4.5.4.1.

d. Group C coverage is required for each year of die or device production on each microcircuit group.

NOTE: The above group C inspection and corresponding marking system shall be implemented on all devices with an inspection lot date code (seal week) of 8840 and later for JAN product and 8939 and later for non-JAN product. Inspection lots formed using die fabricated prior to 1988 for JAN product and prior to 1989 for non-JAN product shall be grandfathered according to the previous group C QCI requirements and marked with "GF" for the die fab symbolization (see A.3.6.3.1).

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A.4.5.5 Group D inspection. Group D inspection (package related tests) shall be in accordance with table V as specified herein or test method 5005 of MIL-STD-883 and shall include those package or case related tests which are performed periodically. Group D tests shall be performed every 26 calendar weeks on each package family for each assembly line (traceable to the inspection lot identification code of the week tested). If no production is performed for an extended period of time, coverage can be reestablished on the next available production run for the package family in need of coverage. Group D results can be used to support any class provided all of the group D sampling criteria are met. Each additional lead finish for each package family shall be subjected to subgroups 3, 5, and 7 of group D. Subgroup D-7 testing is not required for hot solder dip over lead finishes B or C (tin-lead, gold plate) which have been periodically tested for quality conformance inspection on the same package family. For hot solder dipped leadless chip carriers, the B3 and L3 dimensions may be measured prior to solder dip. In addition, laser marked devices for each package family, which do not have group D coverage for laser marking, shall be subjected to subgroups 3 and 5 of group D.

TABLE A-VII. Digital microcircuits.

Technology group	A				B	C			L	M
Technologies	Standard TTL	Schottky TTL	Low power TTL	DTL	ECL	CMOS	PMOS	NMOS	Combination Bipolar and CMOS	Integrated
Die family	93,93H, 54,54H	S,LS, F,ALS	93L, 54L			54HC54A, 4xxx			54BCT, 54ABT	Injection logic
Functions										
Gates	1	8	15	22	29	36	NA	NA	125	NA
Buffers	2	9	16	23	30	37	NA	NA	126	NA
Flip-Flops	3	10	17	24	31	38	NA	NA	127	NA
Combinational gates	4	11	18	25	32	39	NA	NA	128	NA
Sequential registers/ counters	5	12	19	26	33	40	45	48	129	97
RAM	6	13	20	27	34	41	43	46	130	98
ROM/PROM/PLA	7	14	21	28	35	42	44	47	131	99
Microprocessors interface peripherals FIFO	100	101	102	103	104	105	106	107	132	108

NA - None assigned; to be assigned at a later date as necessary.

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TABLE A-VII. Linear microcircuits. 1/

Technology group	D	E	F	G
Technologies	Bipolar	J-FET	CMOS	Combinational
Functions				
Operational amplifiers	49	61	73	85
Comparators	50	62	74	86
Sense amplifiers	51	63	75	87
Regulators	52	64	76	88
Line drivers/receivers	53	65	77	89
Timers	54	66	78	90
Core drivers	55	67	79	91
D/A converters	56	68	80	92
A/D converters	57	69	81	93
Analog switches/multiplexers	58	70	82	94
Voltage reference	59	71	83	95
Sample and hold	60	72	84	96
Active filters	109	112	115	118
Telecommunications	110	113	116	119
Electro-optics	111	114	117	120

1/ Die families are defined as microcircuit groups shown.

TABLE A-VIII. Other microcircuits.

Technology group	Function
H	Multichip

TABLE A-IX. Application specific microcircuits. 1/

Technology group	K	
Technologies	Bipolar	CMOS
Function		
Gate array	121	123
Linear array	122	124

1/ Die families are defined as microcircuit groups shown.

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A.4.5.5.1 Group D sample selection. Sample selection for group D shall be as follows:

a. The package types selected for group D inspection shall be either rotated among the package types available at the time of sample selection from the allotted package family or worst case available from the allotted package family. Worst case shall be determined by the manufacturer based on an incoming vendor material control program (see A.4.5.5.2). For glass-sealed packages (e.g., cerdips, cerpacks), worst case is based on the minimum seal area and the maximum cavity size (in most cases this shall be two packages). Under the rotation option, if a package type has not been tested for 3 years, then the next assembled lot of that package type shall receive group D inspection. If the manufacturer has a single package, which cannot be grouped into a package family, the manufacturer has the option to perform the group D testing once per calendar year on that package.

b. The product accepted for delivery shall be the inspection lot identification codes of the 36 successive weeks, except as allowed in A.4.5.5.1a, beginning with the inspection lot identification code of the successful group D sample for the package family.

c. Different device types may be used for different subgroups. Testing of a subgroup using a single device type enclosed in the intended package type shall be considered as complying with the requirements for that subgroup for all the device specifications or drawings utilizing the qualified package family and lead finish.

d. Technical justification shall be given for device selections for subgroups D-3 and D-4 in regards to device technology electrical performance and package interaction. If a package and technology interaction is present, subgroup D-3 and D-4 shall be performed on the affected combination separately or used as coverage for the whole package family. Rotation of device technology is allowed to address this requirement. For nonconformance see A.4.5.8.

A.4.5.5.2 Incoming vendor material control program. The manufacturer who utilizes the worst case group D option shall have in place an incoming vendor material control program for the piece parts used in packaging (e.g., vendor SPC program). The methods and procedures used to control inspection, storage, and handling of incoming materials shall be documented.

A.4.5.6 Group E inspection. Group E inspection shall be in accordance with table C-I as specified herein or test method 5005 of MIL-STD-883 and, at the contractor's option, is allowed anytime following completion of wafer fabrication. A device type which fails group E inspection may not be certified as an RHA microcircuit at the failed or higher level, but may be used as a non-RHA microcircuit or certified at another (lower) level if the microcircuit meets the lower level requirements and all other applicable requirements including pre- and post-irradiation electrical and timing parametric limits.

A.4.5.6.1 Group E sample selection. Sample selection shall be in accordance with table C-I as specified herein or test method 5005 of MIL-STD-883 and shall be from each wafer prior to assembly or from each inspection or wafer lot. QCI requirements for class level B wafer lots shall be satisfied if all wafers used in that lot have been tested individually in accordance with class level S requirements. For traceability, see A.3.4.6.

A.4.5.7 End-point tests for groups B, C, and D (and E if applicable) inspections. End-point measurements and other specified post-test measurements shall be made for each microcircuit of the sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the device specification or drawing. Any additional end-point electrical measurements that may be performed at the discretion of the manufacturer, shall be accomplished in accordance with A.3.4.3 (e.g., tests performed on sample devices subjected to groups B, C, and D (and E if applicable) tests shall be performed as a 100-percent screen on all production devices represented by the sample) and shall be documented on the test travelers.

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A.4.5.8 Nonconformance. Lots that fail subgroup requirements of groups B, C, and D (and E if applicable) may be resubmitted in accordance with the provisions of A.4.3.3.1. A failed lot that is reworked (see A.3.7.1) or is rescreened (resubmittal to inadvertently missed process steps is not considered a rescreen) may not be resubmitted to the failed subgroups (and shall be counted as a failure) for periodic group B, C, or D (or E if applicable) quality conformance inspection (QCI) coverage. The lot may be resubmitted only to the failed subgroup to determine its own acceptance. If a lot is not resubmitted or fails the resubmission, the lot shall not be shipped, and all references to MIL-PRF-38535, or this appendix, shall be removed. For RHA microcircuits where group E tests are performed, and a sample plan of 18(1) and 38(1) is utilized for two successive lots of the same device type or for more than 10 percent of the lots during the preceding 18 months, data as specified herein shall be provided. Resubmission for RHA qualification inspection, in this case, may be required. Lots that are not resubmitted, fail the resubmission, are withdrawn from compliance consideration, reworked, or rescreened (excluding resubmittal to final electricals when test conditions or limits are not changed) due to the failure of a PDA or QCI requirement of this appendix shall be recorded and properly dispositioned. The reporting of these lots shall include the following, as applicable:

a. PIN.

b. Inspection lot identification code.

c. Quantity of lot.

d. Point of scrap in manufacturer's flow.

e. Test results and date of failure (including all rescreening, reworks, and resubmissions).

f. Reason for failure or scrapping including applicable test results.

g. Date of scrapping or withdrawal from military consideration.

h. Disposition action of affected lots.

NOTE: The Government reserves the right to request and receive information concerning implementation of corrective actions and justification for rework and rescreening.

A.4.5.8.1 Group B failure. When a lot failure occurs for a group B subgroup, then all other sublots within the inspection lots shall be submitted to the failed subgroup.

A.4.5.8.2 Alternate group B failure. When a failure has occurred in group B using the alternate group B procedure, samples from three additional inspection lots of the same package type, lead finish and week of seal as the failed package shall be tested to the failed subgroups. If all three inspection lots pass, then all devices manufactured on the same assembly line using the same package type and lead finish and sealed in the same week may be accepted for group B inspection. If one or more of the three additional inspection lots fails, then no inspection lot containing devices manufactured on the same assembly line using the same package type and lead finish sealed in the same week shall be accepted for group B inspection until each inspection lot has been subjected to and passed the failed subgroups.

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A.4.5.8.3 Group C failure. When a group C failure occurs, samples from subsequent wafer lots submitted for acceptance in the same microcircuit group (see A.3.1.3.12), produced on the same die fabrication line, and started (or completed at the manufacturer's option) die fabrication during the same year shall be subjected to group C. The testing shall be performed on a wafer-lot-by-wafer-lot basis until three consecutively tested wafer lots from the same microcircuit group and year of fabrication pass group C; the testing may then return to periodic testing. A device type that fails a group C inspection shall not be accepted until the device type that failed successfully completes group C. In addition, any other inspection lots using die from the same failed wafer lot shall successfully complete group C prior to shipment until three successive inspection lots from the same wafer lot have passed group C using a tightened sample size number (accept number) with C = 0. In the event of a group C failure, the manufacturer shall evaluate the possible impact on product that has been manufactured since the last acceptable group C test (based on wafer fab code), from the failed microcircuit group.

A.4.5.8.4 Group D failure. When a failure occurs for a group D subgroup(s), samples from subsequent lots submitted for acceptance of the same package family and lead finish shall be subjected to all the tests in the failed subgroup(s). The testing shall be performed on a lot-by-lot basis until three successive lots of the same package family pass the failed subgroup(s). Testing of the package family may then return to periodic testing. The package type that failed the group D subgroup(s) shall be tested on a lot-by-lot basis until three successive lots pass the failed subgroup(s) at which time it may return to periodic inspection coverage. Under the worst case conditions option, when a glass sealed package fails, every package type in the package family shall pass the failed group D subgroup, prior to shipping the device. Failed package types shall be tested on a lot-by-lot basis until three successive lots of the same package type pass the failed subgroup(s) at which time it may return to periodic inspection. In the event of a group D failure, the manufacturer shall evaluate the possible impact on product that has been manufactured since the last acceptable group D (based on seal or encapsulation date code), for the failed package family.

A.4.6 Screening. Each microcircuit shall have been subjected to and passed all the screening tests detailed in TABLE IA. as specified herein or TM 5004 or TM 5010, as applicable, of MIL-STD-883 for the specified quality assurance level and type of microcircuit in order to be acceptable for delivery. When a PDA (see A.3.1.3.13 and TM 5004 or TM 5010 of MIL-STD-883) or delta limits (see A.3.1.3.14) has been specified or other conditions for lot acceptance have been imposed, the required data shall be recorded and maintained as a basis for lot acceptance. Devices that fail any test criteria in the screening sequence shall be removed from the lot at the time of observation or immediately at the conclusion of the test in which the failure was observed. Once rejected and verified as a device failure, no device may be retested for acceptance.

A.4.6.1 Burn-in. Burn-in shall be performed on all microcircuits where specified and the specified pre- and post-burn-in electrical parameters shall be measured. The manufacturer’s Technology Review Board (TRB) shall establish appropriate burn-in and life test methodology for new product families or technology by using JEDEC publication JEP163 in order to meet the quality and reliability performance requirements of MIL-PRF-38535. The burn-in and life test methodology shall be documented to the manufacturer’s Quality Management (QM) plan and devices specification e.g. standard microcircuit drawing (SMD). However, JEP163 requirement shall not be applicable for legacy/heritage products and technologies.

A.4.6.1.1 Lots and sublots resubmitted for burn-in. Inspection lots, lot splits, and class level S sublots may be resubmitted for burn-in one time only and may be resubmitted only when the observed percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater. Any lot that exceeds the allowable resubmission PDA, (greater than 10%, but less than 20%), the manufacturer may resubmit the lot provided analysis is performed to a level sufficient to determine the mechanism of failure for the lot with TRB approval and written notification (letter or email) to the Qualifying Activity prior to shipment. The lot may be resubmitted using tightened inspection criteria. Resubmitted inspection lots, lot-splits, and class level S sublots shall contain only parts which were in the original lot or sublot. Resubmitted inspection lots, lot splits, and class level S sublots shall be kept separate from new lots and sublots and shall be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the sample size series (see appendix D), or one device, whichever is greater.

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A.4.6.1.2 Burn-in acceptance criteria. The PDA for each inspection lot or class level S sublot submitted to burn-in and interim (post burn-in) electrical parameters (see test method 5004 of MIL-STD-883) shall be 5 percent (or one device, whichever is greater) on all failures. In addition, for class level S, the PDA shall be 3 percent (or one device, whichever is greater) on functional failures. A manufacturer may elect to divide inspection lots into splits for burn-in and interim electrical parameter measurement and calculate a PDA for each split, or the manufacturer may elect to add all failures from the constituent splits together to calculate a PDA for the original inspection lot. If a PDA is calculated for each split, it shall be used as accept/reject criteria for that split only and shall not be combined with the PDA from any other lot or split for any reason related to lot or split acceptance. If a PDA is calculated for an inspection lot by adding the failures found in the various constituent splits, this PDA shall be used as accept/reject criteria for the entire lot and shall, in no way, be used as accept/reject criteria for any grouping of devices other than the entire lot. Delta limits shall be defined in the device specification or drawing. When the PDA applies to delta limits, the delta parameter values measured after burn-in (100 percent screening test) shall be compared with the delta parameter values measured prior to that burn-in. Lots may only be resubmitted when the observed percent defective does not exceed twice the specified PDA (10 percent) or 2 devices, whichever is greater. Any lot that exceeds the allowable resubmission PDA, (greater than 10%, but less than 20%), the manufacturer may resubmit the lot provided analysis is performed to a level sufficient to determine the mechanism of failure for the lot with TRB approval and written notification (letter or email) to the Qualifying Activity prior to shipment. The lot may be resubmitted using tightened inspection criteria. The delta criteria applying to such resubmissions shall be in accordance with the following procedure:

a. Devices having delta drift values in excess of the device specification or drawing limits shall be rejected.

b. The remaining devices shall then be submitted to the balance of inspections and tests as specified herein.

A.4.6.1.2.1 Failure analysis of burn-in screen failures for class level S devices. Catastrophic failures (e.g., shorts or opens measurable or detectable at +25°C) subsequent to burn-in shall be analyzed. Analysis of catastrophic failures may be limited to a quantity and degree sufficient to establish failure mode and cause and the results shall be documented and made available to the Government representative.

A.4.6.2 External visual screen. The final external visual screen shall be conducted in accordance with TM 2009 of MIL-STD-883 after all other 100 percent screens have been performed to determine that no damage to, or contamination of, the package exterior has occurred.

A.4.6.3 Particle impact noise detection (PIND) test for class level S devices. The inspection lot (or sublots) shall be submitted to 100 percent PIND testing a maximum of five times in accordance with test method 2020 of MIL-STD-883, condition A. PIND prescreening shall not be performed. The lot may be accepted on any of the five runs if the percentage of defective devices is less than 1 percent (zero failures allowed for lots of less than 100 devices). All defective devices shall be removed after each run. Lots that do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, shall be rejected and resubmission is not allowed.

A.4.6.4 Lead forming. When lead forming (bending) is specified for any device class, a sample fine and gross seal test shall be performed in accordance with TABLE IA. as specified herein or test method 5004 of MIL-STD-883 after the lead forming operations and prior to final visual inspection of these devices, and devices which fail any test shall be removed from the lot.

A.4.6.5 Nondestructive bond pull test for class level S devices. Nondestructive 100 percent bond pull test shall be performed for class level S devices. The total number of failed wires and the total number of devices failed shall be recorded. The lot shall have a PDA of 2 percent or less based on the number of wires pulled in specified lot. The test shall be performed in accordance with test method 2023 of MIL-STD-883. Devices from lots that have been subjected to the nondestructive 100 percent bond pull test and have failed the specified class level S, PDA requirement shall not be delivered as class level B product.

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A.4.7 Test results. The results of all qualification and quality conformance tests and inspections and the results of all required failure analysis shall be recorded and maintained in the manufacturer's facility in accordance with A.4.8. The Quality Assurance Program Plan, qualification test reports, summary of QCI data, and any other data reports required by the applicable acquisition document shall be maintained by the manufacturer (or submitted to the acquiring activity when specified in the purchase agreement). The disposition of all lots or samples submitted for wafer lot acceptance, screening (when PDA is specified), quality conformance inspection or qualification shall be fully documented and lots which fail any specified requirement shall be recorded as failed lots whether resubmitted or withdrawn. Disposition of resubmitted lots shall likewise be recorded so that a complete history is available for every lot tested from initial submission to final disposition including all failures, resubmissions, and withdrawals.

A.4.7.1 Screening test data for class level S microcircuits. When specified in the acquisition document, a copy of the attributes test data, a copy of the variables data, and the delta calculations resulting from the applicable delta parameter tests before and after each burn-in, and a copy of the X-rays required by the device specification or drawing shall accompany each lot of class level S microcircuits shipped. The manufacturer shall maintain one complete copy of all screening data for 10 years after delivery of the parts. This data shall be legible and shall be correlatable to the applicable PIN, the lot date code, and the individual serial number. The data shall be verified by the manufacturer's quality assurance organization and shall bear evidence of such verification.

A.4.8 Quality assurance program.

A.4.8.1 Manufacturer certification. The manufacturer shall establish, implement, and maintain a quality assurance program in accordance with A.4.8 through A.4.9.3.8 (summarized in table A-X) in order to be a manufacturer of class level B microcircuits. The manufacturer's quality assurance program shall demonstrate and assure that design, manufacture, inspection and testing of microcircuits are adequate to assure compliance with the applicable requirements and quality standards of this specification. Where the manufacture or any portion of the manufacturing and testing operation is other than the manufacturer's facility, it shall be the responsibility of the manufacturer to secure and prove the documentation and control of the quality assurance program as described herein. The program shall be documented as follows:

a. Design, processing, manufacturing, and testing instructions (A.4.8.1.1).

b. Records to be maintained (A.4.8.1.2).

c. Quality assurance program plan (A.4.8.1.3).

All required documentation shall be available at, and continually effective in, the manufacturer's plant while it is producing microcircuits which are intended to be offered for qualification and quality conformance inspections under this specification. All required program documentation and records shall be available for review by acquiring activity upon request. The acquiring activity shall have access to nonproprietary areas of the manufacturer's plant for the purpose of verifying its implementation, and the Government shall have access to all areas of the manufacturer's plant for the purpose of verifying its implementation.

Personnel performing quality functions shall have sufficient well defined responsibility, authority, and the organizational freedom to identify and evaluate quality problems and to initiate, recommend, and provide solutions.

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A.4.8.1.1 Design, processing, manufacturing, and testing instructions. The manufacturer shall have in effect documented instructions covering, as a minimum, these areas:

a. Conversion of customer requirements into manufacturer's internal instructions (see A.4.8.1.1.1).

b. Personnel training and testing (see A.4.8.1.1.2).

c. Inspection of incoming materials, utilities, and work in-process (see A.4.8.1.1.3).

d. Quality-control operations (see A.4.8.1.1.4).

e. Quality-assurance operations (see A.4.8.1.1.5).

f. Design, processing, manufacturing equipment, and materials instructions (see A.4.8.1.1.6).

g. Cleanliness and atmosphere control in work areas (see A.4.8.1.1.7).

h. Design, material, and process change control (see A.4.8.1.1.8).

i. Tool, gauge, and test equipment maintenance and calibration (see A.4.8.1.1.9).

j. Failure and defect analysis and feedback (see A.4.8.1.1.10).

k. Corrective action and evaluation (see A.4.8.1.1.11).

l. Incoming, in-process, and outgoing inventory control (see A.4.8.1.1.12).

m. Schematics (see A.4.8.1.1.13).

n. ESD handling control program (see A.4.8.1.1.14).

Detailed requirements for coverage of these items are stated in A.4.8.1.1.1 through A.4.8.1.1.14. These requirements shall normally be expected to be met by the manufacturer's standard drawings, specifications, process instructions, and other established manufacturing practices. If particular requirements are not covered by the manufacturer's established practices, suitable documentation shall be added to satisfy those requirements.

A.4.8.1.1.1 Conversion of customer requirements into manufacturer's internal instructions. The procedure by which customer requirements, as expressed in specifications, orders, etc., are converted into working instructions for the manufacturer's personnel shall be documented.

A.4.8.1.1.2 Personnel training and testing. The motivational and work training and testing practices employed to establish, evaluate, and maintain the skills of personnel engaged in reliability-critical work shall be documented as to form, content, and frequency of use.

A.4.8.1.1.3 Inspection of incoming materials and utilities, and of work in-process. Inspection operations shall be documented as to type of inspection, sampling and test procedures, acceptance rejection criteria, and frequency of use.

A.4.8.1.1.4 Quality control operations. Quality control operations shall be documented as to type, procedures, rating criteria, action criteria, records, and frequency of use.

A.4.8.1.1.5 Quality assurance operations. Quality assurance operations shall be documented as to type, procedures, equipment, judgment and action criteria, records, and frequency of use.

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TABLE A-X. Quality assurance program requirements..

In-house documentation covering these areas (see A.4.8.1.1)	In-house records covering these areas (see A.4.8.1.2)	A program plan covering these areas (see A.4.8.1.3)	Self-audit plan covering these areas (see A.4.9)
a. Conversion of customer requirements into manufacturer's internal instructions (see A.4.8.1.1.1) b. Personnel training and testing (see A.4.8.1.1.2) c. Inspection of incoming materials and utilities and of work in-process (see A.4.8.1.1.3) d. Quality control operations (see A.4.8.1.1.4) e. Quality assurance operations (see A.4.8.1.1.5) f. Design, processing, manufacturing equipment, and materials instructions (see A.4.8.1.1.6) g. Cleanliness and atmosphere control in work areas (see A.4.8.1.1.7) h. Design, material, and process change control (see A.4.8.1.1.8) i. Tool, gauge, and test equipment maintenance, and calibration (see A.4.8.1.1.9) j. Failure and defect analysis and feedback (see A.4.8.1.1.10) k. Corrective action and evaluation (see A.4.8.1.1.11) l. Incoming, in-process, and outgoing inventory control (see A.4.8.1.1.12) m. Schematics (see A.4.8.1.1.13) n. ESD handling control program (see A.4.8.1.1.14)	a. Personnel training and testing (see A.4.8.1.2.1) b. Inspection operations (see A.4.8.1.2.2) c. Failure and defect reports analysis (see A.4.8.1.2.3) d. Initial documentation and subsequent changes in design, materials, or processing (see A.4.8.1.2.4) e. Equipment calibrations (see A.4.8.1.2.5) f. Process utility and material controls (see A.4.8.1.2.6) g. Product lot identification (see A.4.8.1.2.7) h. Product traceability (see A.4.8.1.2.8) i. Self-audit report (see A.4.9.3.6)	a. Functional block organization chart (see A.4.8.1.3.1) b. Examples of manufacturing flowchart (see A.4.8.1.3.2) c. Proprietary documents identification (see A.4.8.1.3.3) d. Examples of design, material, equipment, visual standard, and process instructions (see A.4.8.1.3.4) e. Examples of records (see A.4.8.1.3.5) f. Examples of design, material, and process change control documents (see A.4.8.1.1.8 and as required in A.3.4.2) g. Examples of failure and defect analysis and feedback documents (see A.4.8.1.1.10) h. Examples of corrective actions and evaluations documents (see A.4.8.1.1.11) i. Manufacturer's internal instructions for internal visual inspection (see A.4.8.1.3.6) j. Examples of test travelers (see A.4.8.1.3.7) k. Examples of design and construction baselines (see A.4.8.1.3.8) l. Manufacturer's self-audit (see A.4.9.1)	a. Self-audit program (see A.4.9.3.1) b. Self-audit representatives (see A.4.9.3.2) c. Audit deficiencies (see A.4.9.3.3) d. Audit follow-up (see A.4.9.3.4) e. Audit schedules and intervals (see A.4.9.3.5) f. Self-audit report (see A.4.9.3.6) g. Self-audit areas (see A.4.9.3.7) h. Self-audit checklist (see A.4.9.3.8)

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A.4.8.1.1.6 Design, processing, manufacturing equipment, and materials instructions. Device design, processing, manufacturing equipment and materials shall be documented in drawings, standards, specifications, or other appropriate media which shall cover the requirements and tolerances for all aspects of design and manufacture including equipment test and prove-in, materials acquisition and handling, design-verification testing and processing steps. As a minimum requirement, detailed documentation shall exist for the following items and shall be adequate to assure that quantitative controls are exercised, that tolerances or limits of control (limits shall be established for baselined and other critical wafer fabrication process monitors used for acceptance of class levels B and S product) are sufficiently tight to assure a reproducible high quality product and that process and inspection records reflect the results actually achieved:

a. Incoming materials control (wafers, substrates, packages, active and passive chips or elements for hybrid or multichip microcircuits, wire, water purification, etc.).

b. Masking, photoresist, and mask registration.

c. Epitaxy and diffusion.

d. Oxidation and passivation.

e. Metallization and film deposition.

f. Die, element, and substrate attachment.

g. Bonding.

h. Rework.

i. Sealing.

A.4.8.1.1.7 Cleanliness and atmosphere control in work areas. The requirements for cleanliness and atmosphere control in each work area in which unsealed devices, or parts thereof, are processed or assembled shall be documented. During manufacture, transit, and storage, prior to seal, microcircuit die/wafers shall be protected from human contamination, machine overspray, or other sources of contamination which may occur due to human error or machine design which does not totally eliminate the possibility of overspray or other forms of contamination. Airborne particulate class limits shall be as defined by ISO 14644-1. A method for class verification and reverification shall be documented and implemented. ISO 14644-2 may be used as a guideline. The manufacturer shall establish action and absolute control limits (at which point work stops until corrective action is completed) based on historical data and criticality of the process in each particular area. For foreign material identification and control, see internal visual inspection requirements test method TM 2010 of MIL-STD-883.

A.4.8.1.1.8 Design, material, and process change control. The methods and procedures for implementation and control of changes in device design, material and processing, and for making change information available to the acquiring activity, when applicable, shall be documented.

A.4.8.1.1.9 Tool, gauge, and test equipment maintenance and calibration. The maintenance and calibration procedures, and the frequency of scheduled actions, for tools, gauges, manufacturing and test equipment shall be documented and in accordance with in-house requirements. ISO/IEC 17025 or equivalent should be used as a guideline. Failure to perform scheduled maintenance, repair and recalibration requirements critical to a process (as defined by the manufacturer) shall require corrective action.

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A.4.8.1.1.10 Failure and defect analysis and feedback. The procedures for identification, handling, and analysis of failed or defective devices and for dissemination of analysis data shall be documented, including the procedure for informing the qualifying activity of analysis results, when applicable.

A.4.8.1.1.11 Corrective action and evaluation. The procedure and responsibility for decisions regarding the necessity for corrective action as a result of failure or defect analysis, and for evaluation and approval of proposed corrective actions, shall be documented. If the procedure for evaluation and approval of changes proposed for other reasons, such as cost reduction or product improvement, differs from the above, it shall also be documented.

A.4.8.1.1.12 Incoming, in-process, and outgoing inventory control. The methods and procedures shall be documented which are used to control storage and handling of incoming materials, work in-process, and warehoused and outgoing product in order to (a) achieve such factors as age control of limited-life materials; and (b) prevent inadvertent mixing of conforming and nonconforming materials, work, or finished product. Tests and inspections performed by the manufacturers on acquired materials and supplies shall include verification of chemical, physical, and functional characteristics required by manufacturer drawings and specifications. Procedures shall be prepared and maintained for controlling the receipt of acquired materials and supplies. The procedures shall provide the following:

a. Withholding received materials or supplies from use pending completion of the required inspection or tests, or the receipt of necessary reports.

b. Segregation and identification of nonconforming materials and supplies from conforming materials and supplies and removal of nonconforming subassemblies and parts.

c. Identification and control of limited-life materials and supplies.

d. Identification and control of raw materials.

e. Assurance that the required test reports, certification, etc., have been received.

f. Clear identification of materials released from receiving inspection and test to clearly indicate acceptance or rejection status of material pending review action.

A.4.8.1.1.13 Schematics. Schematics pertaining to the testing of microcircuits shall be under document control. This includes device schematics or burn-in schematics in accordance with the applicable device specification or drawing.

A.4.8.1.1.14 ESD control program. ESD protection, control, grounding procedures and training programs are very important key points to mitigate ESD damage at the microcircuits manufacturing and testing process. QML microcircuits manufacturers/suppliers shall establish an ESD mitigation program to safeguard against discharge damage at all wafer fabrication, wafer bumping, wafer scribing, coring services, automatic handling equipment's, assembly facilities, testing station, packaging and handing of dice and devices in accordance with JESD625 or ANSI/ESDA S20.20. The established ESD control program documentation shall be under document control and TRB shall review and inspect periodically.

A.4.8.1.2 Records to be maintained. The records required by this section shall be continuously maintained during the manufacture of microcircuits that are intended to be submitted for quality conformance inspection under this specification. The records pertaining to production processes, incoming and in-process inspections shall be retained as detailed in A.4.8.1.2.b. Those pertaining to screening and quality conformance inspection shall be retained for a minimum of 10 years after performance of the inspections. Records shall be maintained as a minimum for:

a. Personnel training and testing (see A.4.8.1.2.1) (1-year active file retention; 5-year total record retention).

b. Inspection operations (see A.4.8.1.2.2) (1-year record retention for production processes, incoming and in-process; 10-year record retention for screening, qualification, and quality conformance inspection).

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c. Failure and defect reports and analyses (see A.4.8.1.2.3) (5-year record retention).

d. Initial documentation and subsequent changes in design, materials, or processing (see A.4.8.1.2.4) (5-year record retention).

e. Equipment calibrations (see A.4.8.1.2.5) (see ISO/IEC 17025 for records).

f. Process, utility, and material controls (see A.4.8.1.2.6) (1-year record retention).

g. Product lot identification (see A.4.8.1.2.7) (10-year record retention).

h. Product traceability (see A.4.8.1.2.8) (10-year record retention).

i. Self-audit report (see A.4.9.3.6) (4-year retention).

Note: Altered records shall not be considered acceptable data unless documented instructions are followed which shall include:

j. For changed data:

(1) Identification of individual making new entry.

(2) Maintain identity of all original data entries (white out is not permitted).

(3) Justification and date noted for change and verification by a second party (QA shall verify screening, qualification and quality conformance inspection records) when change affects lot jeopardy (e.g., lot originally considered to be rejected is changed to pass status).

k. For transferred data to new test record:

(1) Identification of individual transferring data.

(2) All original record entries shall be transferred.

(3) New test record entries shall be verified against the original test record by a second party.

l. Computerized records are optional provided they clearly and objectively indicate that all the requirements, of the specified device class, of this appendix have been met. The computerized records for traceability, screening and quality control inspection shall be readily accessible and available to Government personnel for review and an appropriate electronic/hard copy provided when required. The requirements below shall be met.

(1) Entry verification:

(a) Each individual making shall be uniquely identified.

(b) All manually entered data shall be verified at the time of entry by the same operator.

(c) All accepted transactions (e.g., entered data) shall be identified by time/date or date/entry sequence to protect against "out of sequence" entries. No recorded transactions shall be deleted or changed.

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(2) Control procedures for lot history records:

(a) Lot histories may be modified only by additions (e.g., original entries plus corrective addenda).

(b) All corrective addenda shall meet all the requirements of A.4.8.1.2 i.

(c) Only limited designated operators shall be able to access lot history computer records for corrective addenda. Documented security procedures shall be followed to assure that limited access is maintained (e.g., restricted terminals, passwords, etc.).

(d) A quality assurance representative shall verify screening, qualification, and quality conformance inspection records when corrective addenda affect lot jeopardy.

(3) Control of computerized lot history records:

(a) All computer lot history records shall have an accurate tape or equivalent backup generated prior to lot shipment. Within 3 months of lot shipment, the backup record shall be transferred to a secure location to be archived.

(b) These archived tapes or equivalent media shall be kept for a minimum of 10 years.

A.4.8.1.2.1 Personnel training and testing. Records shall cover the nature of training or testing given, the date thereof by week and length in hours, and the group(s) of personnel given work training and testing. Records are required only for product-related training and testing as distinguished from safety, first aid, etc.

A.4.8.1.2.1.1 Training of operators and inspectors. All critical processes and production inspection shall be performed by personnel who have been trained by the manufacturer to perform their assignment task in accordance with manufacturer's in-house standards, including a formal training (e.g., classroom or on the job training supervised by a certified trainer) and test procedure to assure the proficiency of each individual. Each individual shall be retested or retrained at the end of a designated period or when personnel performance indicates poor proficiency. Personnel shall not be used in critical processes or inspections until the required level of proficiency has been demonstrated.

A.4.8.1.2.2 Inspection operations. Records of inspection operations shall cover the tests or inspections made, the materials group (lot, batch, etc.) inspected, the controlling documentation, the date of completion of inspection, the amount of material tested, and acceptance, rejection, or other final disposition of the material.

A.4.8.1.2.3 Failure and defect reports and analyses. Records of failed or defective devices shall cover the source from which each device was received, the test or operation during which failure occurred or defects were observed, and prior testing or screening history of the device, the date of receipt, and the disposition of the device. Records of failure and defect analyses shall cover the nature of the reported failure or defect (failure or defect mode), verification of the failure or defect, the nature of any device discrepancies which were found during analysis (failure or defect mechanism), assignment of the failure-activating cause if possible, the date of completion of the analysis, identification of the group performing the analysis, disposition of the device after analysis, and the distribution of the record. The record shall also treat the relationship of observed failure or defect modes in related lots or devices and, where applicable, corrective action taken as a result of the findings.

A.4.8.1.2.4 Initial documentation and subsequent changes in design, materials, or processing. Records shall cover the initial documentation and all changes with the date upon which each change in design, materials, or processing becomes effective for devices intended to be submitted for quality conformance inspection under this specification, the documents authorizing and implementing the change, and identification of the first production and quality conformance inspection lot(s) (as applicable) within which product incorporating the change is included shall be maintained when the change requires notification of the qualifying activity (see A.3.4.2).

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A.4.8.1.2.5 Equipment calibrations. Records shall cover the scheduled calibration intervals for each equipment item, the dates of completion of actual calibration, identification of the group performing the calibration, and certification of the compliance of the equipment with documented requirements after calibration, (use ISO/IEC 17025 or equivalent, as a guideline).

A.4.8.1.2.6 Process, utility, and material controls. Records shall cover the implementation of devices such as control charts (e.g., X bar R charts) or other means of indication of the degree of control achieved at the points in the material, utility, and assembly process flow documented in the manufacturing instructions. Records shall also indicate the action taken when each out-of-control condition is observed, and the disposition of product processed during the period of out-of-control operation.

A.4.8.1.2.7 Product lot identification. Records shall be maintained to identify when each production or inspection lot or both was processed through each area. Records shall be capable of identifying for each production and acceptance inspection lot (as applicable) of finished product, these items as a minimum:

a. The acceptance inspection tests performed on the lot, and their results.

b. The serial numbers (when applicable) of all devices in the lot.

c. The date of completion of acceptance inspection of the lot.

d. Identification of the lot.

e. The pertinent device specification or drawing under which inspection was performed.

f. Final disposition of the lot (withdrawn, not accepted, accepted).

g. Acquiring activity source inspection consideration of the lot.

h. The number of devices, by device type, in each lot at the time of seal.

i. Independently identify, by device type, the number of devices shipped and the number of devices in stock inventory.

A.4.8.1.2.8 Product traceability. The traceability system shall be maintained such that the qualifying activity can trace and determine that the microcircuits passed the applicable screening, qualification, and quality conformance inspections; that the microcircuits were assembled on the proper certified assembly line, and processed on the correct wafer process line.

A.4.8.1.3 Quality assurance program plan. The quality assurance program plan shall be established and maintained by the manufacturer, and shall be reviewed by the qualifying activity (QA). It shall consist of a volume or portfolio, or series of same, which shall serve to demonstrate that the manufacturer's understanding of a complete quality assurance program, as exemplified by their documentation system, is adequate to assure compliance of their product with the applicable specifications and quality standards. If the quality assurance program exemplified is applied consistently to all product lines intended to be submitted for acceptance inspection under this specification, only one program plan is required for each manufacturing plant; any difference in treatment of different product lines within a plant shall be stated and explained in the program plan, or separate program plans prepared for such different lines. The program plan shall contain, as a minimum, these items:

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a. Documents representing the manufacturer's quality organization:

(1) Functional block organization chart (see A.4.8.1.3.1).

(2) Example of manufacturing flowchart (see A.4.8.1.3.2).

(3) Proprietary-document identification (see A.4.8.1.3.3).

(4) Examples of design, material, equipment, visual standard, and process instructions (see A.4.8.1.3.4).

(5) Examples of records (see A.4.8.1.3.5).

(6) Examples of design, material and process change control documents (see A.4.8.1.1.8).

(7) Examples of failure and defect analysis and feedback documents (see A.4.8.1.1.10).

(8) Examples of corrective action and evaluation documents (see A.4.8.1.1.11).

(9) Manufacturer's internal instructions for internal visual inspection (see A.4.8.1.3.6).

(10) Examples of test travelers (see A.4.8.1.3.7).

(11) Examples of design and construction baseline (see A.4.8.1.3.8).

(12) Manufacturer's self-audit program (see A.4.9).

NOTE: Where a manufacturer's lot/test traveler (see A.4.8.1.3.7) contains all the information required for a flowchart (see A.4.8.1.3.2), it may be used to satisfy the requirement for the flowchart.

b. Critical documents which are to be kept current and on file by the qualifying activity:

(1) SPC program plans/milestones, as applicable.
(2) Process flowcharts and baselines (wafer fabrication, assembly and test).
(3) General QCI procedures.
(4) Major change notification procedure.
(5) Internal visual inspection procedure.
(6) QM Plan

A.4.8.1.3.1 Functional block organization chart. This chart shall show, in functional block-diagram form, the lines of authority and responsibility (both line and staff) for origination, approval, and implementation of the several aspects of the quality assurance program. Names of incumbents are not required in this chart.

A.4.8.1.3.2 Examples of manufacturing flowchart. The flowchart for all devices shall reflect the complete manufacturing processes being used at the time and shall show all manufacturing, inspection, testing and quality verification points and the point where all materials or subassemblies enter the flow. The flowchart shall clearly show any utilization of third party activities. The chart shall identify all major documents pertaining to the inspection of materials, the production processes, the production environments, and production controls that were used. The documents shall be identified by name and number. Changes approved thereafter shall be treated in accordance with the approved document change control procedures in A.3.4.2.

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A.4.8.1.3.3 Proprietary-document identification. A listing of proprietary documents and areas shall be included in the program plan and maintained on a current basis (see A.4.8.1).

A.4.8.1.3.4 Examples of design, material, equipment, visual standard, and process instructions. An example of each type of design, material, equipment, visual standard, and process instruction used in the manufacture of microcircuits intended to be submitted for acceptance inspection under this specification shall be included in the program plan. These may be either dummies or actual working documents, but shall, in either event, show the form of the pertinent document; blank forms shall not be included.

A.4.8.1.3.5 Examples of records. Examples of records, complying with the requirements of A.4.8.1.3.4 for instructions, shall be included in the program plan.

A.4.8.1.3.6 Manufacturer's internal instructions for internal visual inspection. The manufacturer's internal instructions for internal visual inspection in accordance with test method 2010 or test method 2017, as applicable, of MIL-STD-883 for the applicable device class, shall be included in the program plan.

A.4.8.1.3.7 Examples of travelers. Wafer fab, assembly, screening, and groups A, B, C, D (and E, if applicable) travelers shall be included in the program plan and maintained on current basis. The traveler utilized for QCI lots may be the same traveler as used for qualification lots. When in-line inspections are allowed (e.g., alternate group A or B) the traveler shall include documentation of required inspections. The travelers shall include all manufacturer imposed tests. The test traveler shall include all the following minimum information (if applicable):

a. Identification as to whether the lot is qualification or QCI.

b. Name or title of operation and specification number of each process or test.

c. PIN, date code, and manufacturer internal lot identification number(s).

d. Date(s) of test and operator identification.

e. Calibration control number or equipment identification of all major equipment components used for test.

f. Quantity tested and rejected for each process or test and actual quantity tested, if sampled.

g. Serial numbers of passing and failing devices when applicable.

h. Time in and out of process or test if critical to process or test results (e.g., burn-in and 96-hour window).

i. Specific major conditions of tests that is verifiable by operator including times, temperatures, RPMs, etc. (Not required for screening and QCI traveler.)

j. The percent defective calculated for burn-in.

k. Burn-in/life test board serial number or test circuit identification number and revision.

l. All required variables data except for electrical tests (attachments permitted). (Not required for QCI traveler.)

m. For electrical tests, test program number and revision and identify when variables data is required.

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A.4.8.1.3.8 Examples of design and construction baseline. The design and construction baseline information (e.g., DSCC-VQC-42 “DSCC Microcircuit Materials and Construction Baseline Sheet”, or equivalent) shall be included in the manufacturer's program plan and maintained under document control. The baseline form shall clearly show any utilization of third party activities.

A.4.9 Self-audit requirements

A.4.9.1 Self-audit requirements. The intent of the self-audit program is to assure continued conformance to specification requirements.

A.4.9.2 Definitions

A.4.9.2.1 Self-audit. The performance of periodic survey by the device manufacturer's designated personnel to evaluate compliance to specifications.

A.4.9.2.2 Audit checklist. A form listing specific items which are to be audited.

A.4.9.3 General

A.4.9.3.1 Self-audit program. The manufacturer shall establish an independent self-audit program under the direction of the quality organization to assess the effectiveness of the manufacturer's compliance to all applicable specifications. The manufacturer's self-audit program which identifies key review areas, their frequency of audit, and the corrective action system to be employed when variations from the approved procedures or specification requirements are identified shall be included in the program plan. The self-audit program shall, as a minimum, incorporate the following requirements.

A.4.9.3.1.1 Correction of deficiencies. A system to identify and correct any deficiencies (e.g., processing and testing) or deviations from the specification requirements.

A.4.9.3.1.2 Deviation from critical documents. Provide for review of all deviations from critical documents, such as, baseline(s), flowchart(s), traveler(s), QCI procedures, etc.

A.4.9.3.1.3 Training and retraining of auditors. Specify the selection and training/retraining requirements for auditors.

A.4.9.3.1.4 Self-audit schedule and frequency. Specify the self-audit frequencies and require that a schedule be established and adhered to.

A.4.9.3.2 Self-audit representatives. The quality assurance representatives or the designated appointees shall perform all self-audits. The designated auditors shall be independent from the area being audited. If the use of an independent auditor is not practical, then as a minimum, another individual should be assigned to participate in the audit or review the results with the auditor from the area. The auditors shall be trained in the area to be audited, in the applicable specification requirement and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor(s) shall review the previous audit checklist to assure corrective actions have been implemented and are sufficient to correct the deficiencies.

A.4.9.3.3 Audit deficiencies. All audit deficiencies shall be documented on the appropriate form and a copy submitted to the department head for corrective action(s). All corrective actions shall be agreed to by the quality organization or Material Review Board.

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A.4.9.3.4 Audit follow-up. All audit reports shall be filed and maintained by the quality organization. The quality organization shall establish a procedure to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner. A system (e.g., Management Review) shall also be established to review the acceptability and timeliness of all corrective actions and to determine if any deficiencies have repeated since the last required self-audit. If any deficiencies have occurred two or more times in the predetermined time period, additional corrective actions shall be taken to assure immediate correction of the problem and the qualifying activity (QA) shall be notified. The self-audit team shall perform a follow-up verification within 6 months of corrective actions covering all deficiencies found during the QA audit and annual self-audit to assure corrective actions are adequate and maintained.

A.4.9.3.5 Audit schedules and intervals. The original audit interval shall be established with a schedule by the quality organization but in no case exceed 1 year for each area, unless authorized by the qualifying activity (QA). A self-audit shall be conducted and corrective actions completed prior to the initial QA audit. Changes to the audit schedule, due to being consistently above or below average performance on the self-audit, shall require approval of the QA.

A.4.9.3.6 Self-audit report. The self-audit report shall be signed by the quality assurance representative responsible for the quality assurance program's overall success or failure. The manufacturer shall make available to the qualifying activity, during audits, the self-audit report, deficiencies, and corrective actions taken. This report shall include a summary report of self-audit results categorized by deficiency type (e.g., nonconformance to specification requirement(s), occurrences affecting product reliability, recurring deficiencies).

A.4.9.3.7 Self-audit areas. The self-audit shall be performed to assure conformance to the checklist and specification in at least the following areas:

Calibration and preventive maintenance
Fabrication
Assembly operations
Electrical test
Test methods
Environmental control
Incoming inspection
Inventory control and traceability
ESD handling control program
Deionized (DI) water controls
Training
Failure analysis
Qualification/QCI system
Document control
Design change control
Statistical process control, as applicable
Third party subcontractors (see note)

NOTE 1: The QA approval of a subcontractor second and third party facility does not alleviate the manufacturer of validating product specific requirement.

NOTE 2: The self-audit shall include any activities performed by a subcontractor, and shall ensure full compliance by the subcontractor to this appendix and the device specification or drawing. Any deviations or questionable areas shall be brought to the attention of the qualifying activity. QA approval of subcontracted second party facilities may be used to satisfy the subcontractor audit requirement.

A.4.9.3.8 Self-audit checklist. The audit checklist shall be prepared by the quality organization and maintained under document control. The checklist shall assure that the quality assurance system is adequate and followed by all personnel in each area.

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APPENDIX A

A.5 PACKAGING

A.5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of material is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the military service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

A.5.2 Packaging requirements. The packaging of microcircuits shall prevent mechanical damage to the device during shipping and handling and the packaging material shall not be detrimental to the device. In addition, microcircuits which have been determined to require electrostatic discharge protection, category A or class 1 or 2 by test method 3015 of MIL-STD-883 (see A.4.4.2.8), shall be packaged in conductive material or packaged in accordance with one of the following:

Category A.

(1) Unit container suitable for ESD protection.
or

(2) Conductive noncorrosive rail with noncorrosive and conductive or antistatic foam plugs at both ends of each rail which prevents movement.
or

(3) Antistatic noncorrosive rail with noncorrosive and conductive or antistatic foam plugs at both ends of each rail which prevents movement. Antistatic rails shall be packaged in conductive, electrostatic field shielding material.

(Other packaging methods shall require the approval of the acquiring activity.)

NOTE: Rails (e.g., multiple carriers) coated but not impregnated with antistats shall be used only if the antistatic properties are proven to be intact on the surface. These measurements shall conform to A.3.1.3.21 and EIA541.

A.5.2.1 Carrier and container. When specified on the detail specification or order, microcircuits shall be supplied mounted in the carrier (unit or multiple) and carrier container, or carrier and unit container. Marking on the carrier or unit container shall be as specified in A.5.2.2.

A.5.2.2 Marking of container. All of the markings specified in A.3.6, except the index point and serialization, shall appear on the carrier, unit pack (e.g., individual foil bag), unit container, or multiple carriers (e.g., tubes, rails, magazines) for delivery. An industry standard symbol for identifying ESD sensitive items (e.g., JESD471 symbol) shall be marked on the carrier or container. However, if all the marking specified above is clearly visible on the devices and legible through the unit carrier or multiple carriers, or both, then the ESD marking only (in accordance with MIL-STD-1285) shall be required on the multiple carriers. These requirements apply to the original or repackaged product by the manufacturer or distributor.

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A.6 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

A.6.1 Intended use. Microcircuits conforming to this appendix are intended for use for Government microcircuit application and logistic purposes. For maximum cost effectiveness while maintaining essential quality and reliability requirements, it is recommended that, for initial acquisitions for original equipment complements, the device class appropriate to the need of the application (see A.3.4) be acquired.

A.6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. PIN and compliance identification (if applicable).

c. Test data to be furnished.

d. Packaging Requirements (see A.5).

e. Requirement for radiation hardness assurance testing (see A.4.4.2.5 and A.4.5.6).

A.6.2.1 Lead finish designator. For Government logistic support, the A lead finish will be ordered and supplied to the end user when X is used in place of the A, B, C, D, or E lead finish designator. If the device type is not available with lead finish A, the same PIN will be ordered except that B, C, D, or E will be used as the lead finish designator depending upon which is available.

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APPENDIX B

SPACE APPLICATION

B.1 SCOPE

B.1.1 Scope. This appendix presents the requirements that are to be used to supplement this specification and the other applicable appendices for space level microcircuits. The manufacturer's process may include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved by the qualifying activity after coordination with the government space community (e.g., DTRA, NASA, NRO, and AFSMC). The approach outlined in this appendix is a proven baseline that contains details of the screening and technology conformance inspection (TCI) procedures. Manufacturers are to be able to demonstrate a process control system that achieves at least the same level of quality as could be achieved by complying with this appendix. This appendix is intended for product to be used in space applications. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

B.2 APPLICABLE DOCUMENTS.

B.2.1 General. The documents listed in this section are specified in sections B.3 or B.4 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections B.3 and B.4 of this appendix, whether or not they are listed.

B.2.2 Government documents.

B.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-M-38510 - Microcircuits, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

B.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

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APPENDIX B

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 - Test Procedures for the Measurement of Single Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

B.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein(except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

B.3 REQUIREMENTS

B.3.1 General. Microcircuits supplied to this appendix shall be manufactured and tested in accordance with the approved DLA qualifying activity (QA) baselines and the applicable requirements specified herein. Upon approval from the Technology Review Board (TRB) and the qualifying activity (QA), screening and TCI tests may be modified/optimized for qualified manufacturer listing (QML) class V, class Y, or class P (class level S) product, provided substantiating data is submitted to demonstrate that the manufacturer has a defined capability on the manufacturing line which is under control, repeatable and reliable to and produces product that that meets the intent of the original requirements. These changes cannot affect any thermal, mechanical or electrical parameters, which affect form, fit, function or radiation hardness assurance level (when applicable) of the device, defined within the device specification or standard microcircuit drawing (SMD). The space community (e.g., DTRA, NASA, NRO, and AFSMC) and the customer shall be notified of major changes to the manufacturer's quality management (QM) plan. Any optimization proposed by the manufacturer must be presented to the qualifying activity and coordinated with the space community with accompanying supporting data to validate the proposed change. The optimization must be approved by the QA in writing prior to implementation. For class V, class Y, and class P (class level S) product marked with RHA designator required to meet appendix C and table C-I group E tests.

B.3.1.1 Acquiring activity. When specified by the acquisition document (purchase order), the acquiring activity may:

a. Require prior notification of major changes to the baselined processes, procedures, or testing.

b. Require independent verification of wafers (unprobed) or packaged devices (technology characterization vehicle (TCV), standard evaluation circuit (SEC), or actual devices) by original equipment manufacturer’s (OEM's) or Government agencies.

c. Request screening and TCI summary data is delivered with the devices.

B.3.2 Conflicting requirements. In the event of conflict between the requirements of this appendix and other referenced documents, the order of precedence shall be as follows:

a. The acquisition document (order).
b. Applicable device specification.
c. This appendix.
d. MIL-PRF-38535.
e. Specifications, standards, and other documents referenced in 2.1 of MIL-PRF-38535.

NOTE: The acquisition document may specify additional requirements, but shall not reduce or waive any requirements herein.

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B.3.3 Validation (certification). Validation of a manufacturing line for production of integrated circuits for use in space systems shall be accomplished by a team headed by DLA Land and Maritime with members from the space community (e.g., NASA, NRO, DTRA, and AFSMC), other interested services, and the customer as necessary.

B.3.4 Manufacturing verification. When specified, the manufacturing verification procedure for new technology shall include characterization of actual devices at -55°C and 125°C (or high and low temperature as specified in the device specification) with DC, AC and full functional electrical parameters. Life testing of new technologies shall be determined by the manufacturer based on characterization with full temperature testing and read and record measurements every 1000 hours. Characterization shall also include a complete evaluation of potential failure mechanisms and mitigations strategies, calculation/evaluation of activation energy and acceleration factors for voltage and temperature, and establishment of long term reliability failure rates. The life test may be modified based on the determination of failure mechanisms and activation energy (see TM 1016 for guidance with a goal of 15 year operating life at $+65°C \leq T_J \leq 95°C$. The manufacturer shall determine worst case for their devices). Additional requirements for characterization are included in appendices G and H (see H.3.1.9 c (v)), and are a requirement for class V, class Y, and class P (class level S) devices.

B.3.5 Design verification. When specified, a fully functional VHSIC Hardware Description Language (VHDL) model shall be available.

B.3.6 Part or identifying number (PIN). Each class V, class Y, and class P level QML microcircuit shall be marked with the device class designator "V", “Y”, or “P” in place of the "Q" designator in the PIN format, see 3.6.2a herein. Devices procured to MIL-M-38510 PINs shall be marked in the format in 3.6.2b herein with the device class designator "S".

B.3.7 Serialization. Prior to the first recorded electrical measurement in screening, each class V, class Y, and class P microcircuit shall be marked with a unique serial number assigned within the level of the individual microcircuit within that inspection lot.

B.3.8 Traceability. For class V, class Y, and class P, inspection lot records shall be maintained to provide traceability from the device serial number to the specific wafer lot or to the specific wafer when testing to any group E subgroup (see table C-I), is performed on a wafer by wafer basis.

B.3.9 New technology requirement. For class level S product, this is a product family, material, or process that has never been previously characterized and qualified by the manufacturer for space applications, and is detailed in the manufacturer’s new technology insertion program (see 3.4.1.1 and 6.4.43). Existing devices that meet the major change criteria of table A-I are to be evaluated in conjunction with the qualifying activity to determine if the change should be classified as a new technology, as defined in 3.4.1.1 prior to finalized qualification plan implementation.

B.3.10 Package integrity demonstration test plan (PIDTP) . Manufacturability, test, quality and reliability issues unique to specific assembly/package technologies intended for space applications must be addressed in a PIDTP at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan include: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, c) solder terminations and d) passive components. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP (see H.3.4.4.1).

B.3.11 Solder terminated microcircuits. Microcircuits employing solder terminations (e.g., Ball Grid Array-BGA or Column Grid Array- CGA) shall meet all applicable appendices and Appendix B herein and must be addressed in the package integrity demonstration test plan (PIDTP) (see H.3.4.4.1.3).

B.3.12 Assembly materials. For BGA and CGA packages material contents for solder balls, bumps and solder columns shall be specified on device SMDs and QM plan (see H.3.4.4.1.3) and organic materials shall be included in the PIDTP if applicable.

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B.3.13 Moisture sensitivity level (MSL) . Non-hermetic devices can exhibit sensitivity to moisture-induced stress and must be handled, packaged, and stored in a proper manner to avoid potential damage during assembly solder reflow attachment and/or repair operations. Moisture sensitivity levels are defined as a rating identifying a component's susceptibility to damage due to absorbed moisture when subjected to reflow soldering. The manufacturer shall be required to define the moisture sensitivity level (MSL) for each non-hermetic device in accordance with JEDEC J-STD-020.

B.4 VERIFICATION

B.4.1 Screening test for class V and class Y. In addition to the screening tests specified in the main body of this specification, the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

a. Nondestructive bond pull (NDBP) in accordance with TM 2023 of MIL-STD-883, or approved alternate verified during validation, on each interconnect bond. An alternate method, if necessary, shall consider a 100 percent visual inspection of the elements to be bonded (e.g., bond pads and posts) prior to the bonding operation, as one part of an overall alternate method. For flip chip package devices, Nondestructive bond pull (NDBP) test is not required.

b. Particle impact noise detection (PIND) in accordance with TM 2020, condition A of MIL-STD-883 on each device. For devices without a cavity such as class Y or flip chip devices with underfill, Particle impact noise detection (PIND) test is not applicable.

c. Radiograph inspection in accordance with TM 2012 of MIL-STD-883 on each device. Only one view is required for flat packages and leadless chip carriers having lead terminal metal on four sides.

d. For flip chip technology SAM inspection is required.

    i) SAM inspection shall be performed on each flip chip device in accordance with TM 2030 of MIL-STD-883.

    ii) SAM test shall be performed on each device when a heat sink or lid is attached directly to the back side of the flip chip die in accordance with TM 2030 of MIL-STD-883.

e. Seal test (TM 1014) is not required for class Y non-hermetic devices.

f. Burn-in test in accordance with TM 1015 of MIL-STD-883 shall be conducted on each device for 240 total hours at +125°C. For a specific device type, the burn-in duration may be reduced from 240 to 160 hours if three consecutive production lots of identical parts, from three different wafer lots pass percent defective allowable (PDA) requirements after completing 240 hours of burn-in. Sufficient analysis (not necessarily failure analysis) of all failures occurring during the run of the three consecutive burn-in lots shall not reveal a systematic pattern of failure indicating an inherent reliability problem which would require that burn-in be performed for a longer time. Other burn-in conditions may be considered by a class level S validation team. The manufacturer's burn-in procedures shall contain corrective action plans, approved by the validation team, for dealing with lot failures. PDA shall be in accordance with table IA as specified herein or TM 5004 of MIL-STD-883 for class level S. Static burn-in may be substituted for high temperature reverse bias burn-in based on device technology and must be approved by the QA. Moreover, burn-in test time-temperature regression table I of TM 1015 of MIL-STD-883 can be used for determination of reverse bias burn-in time and temperature.

g. Wafer lot acceptance testing in accordance with TM 5007 of MIL-STD-883 or an alternative which meets the minimum requirements of TM 5007 shall be conducted on each wafer lot producing class V or S devices (see H.3.2.1.4).

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B.4.2 Screening for solder termination microcircuits of class V, class P and class Y . In addition to the screening tests specified in the main body of this specification for solder terminated microcircuits, the screening tests specified below shall be performed, unless prior approval for deletion or modification is given by the qualifying activity.

B.4.2.1 Ball grid array (BGA) microcircuits . For BGA microcircuits post-assembly screening burn-in test may be performed before the solder balls have been attached to the package. Electrical test shall be performed across the full military temperature range after attachment of the solder balls on the package.

B.4.2.2 Column grid array (CGA) microcircuits . For CGA microcircuits post-assembly screening (including electrical test and burn-in) may be performed before the solder columns have been attached to the package. Electrical test shall be performed across the full military temperature range before attachment of the solder columns on the package.

After column attach, electrical test shall be performed at 25°C (Group A, subgroup 1) as a minimum to verify that no electrical/mechanical damage has been introduced due to the column attach process, and visual inspection shall be performed according to TM 2009 of MIL-STD-883.

B.4.3 Technology conformance inspection (TCI) for class V, class P and class Y. In addition to the TCI tests specified in the main body of this specification (see table II to table V), unless otherwise noted herein, the TCI requirements listed below apply on each lot of deliverable devices. The group and table references correspond to those contained herein. These requirements do not replace the normal TCI testing requirements of this specification. The following additions or exceptions apply to the TCI tests specified in the main body of this specification.

Table III, group A electrical test shall be performed on each deliverable lot using actual devices. For those lots having a quantity of less than 116 devices, the tests shall be imposed on a 100 percent basis and the lot accepted on zero test rejects. If a microcircuit fails a group A test parameter as a result of faulty test equipment or operator error, the cause shall be determined and documented, and corrective action shall be implemented and documented. The affected lot may then be accepted by being resubmitted to the failed test parameters using a 116/0 or 100 percent/0 sample.

If a microcircuit fails a group A test due to a previously unscreened parameter, the affected lot may be accepted by screening the lot 100 percent for the failed parameters, and resubmitting a group A sample to the failed subgroup using a 116/0 or 100 percent/0 sample. Any failures resulting from the second screen shall count toward the lot total percent defective. PDA shall be in accordance with table III herein or TM 5005 of MIL-STD-883 for class level S.

Group A electrical tests are not required to be performed when the following conditions are met:

(1) The final electrical tests of the 100 percent screening test (see table IA.) includes all required group A tests (see table III).
(2) The test setup and test conditions are verified by a certified monitor other than the test operator.
(3) Analysis of failures does not indicate a generic or lot related reliability problem.

Note: In no event shall the absence of separate group A testing result in a failure to satisfy the data requirements of section B.3.1.1c.

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a. **Table II, group B**, shall be performed on actual devices except as noted herein. Empty device packages or electrical rejects may be used for subgroups B-1 and B-3, and electrical rejects that have been subjected to the 100 percent screening tests may be used for subgroup B-2. The electrical rejects and empty packages shall have been produced under equivalent conditions as the production lot. The TRB shall determine that the intent of the tests is not violated.

For classes V and Y exceptions and additional requirements are as follows:

1. Resistance to solvents test is not required for laser marked device.

2. Device packages with lid/heat sink attached on the back side of a flip chip die require a lid shear or lid torque test. Manufacturers shall submit test procedures of lid shear test for approval of QA. Lid torque test shall be performed in accordance with TM 2024.

3. Device with solder terminations:

   (i) For ball grid array (BGA) packages, ball shear test shall be performed in accordance with JESD22-B117.

   (ii) For column grid array (CGA) packages, solder column pull test shall be performed in accordance with TM 2038.

b. Table IV, group C or group B, Subgroup 5 life test requirements shall be met using one of the procedures below.

(1) Life test may be performed on a quantity (accept) criteria of 22(0) for 2000 hours at 125°C or equivalent per TM 1005 to attain 44,000 device hours. For lots greater than 200, actual devices shall be used. For lots less than or equal to 200, the number of actual devices shall be the greater of 5 devices or 10 percent of the lot, and the SEC shall supplement actual devices to result in a sample of 22 unless acceptable group C data from the same lot of SEC is available for the previous 3 months. The SEC shall have been produced under equivalent conditions as the production lot and as close in time as feasible, but not to exceed a 3 month period.

Note: For ASICs, a sample size of 5 actual devices may be used with the balance being made up of the SEC.

(2) Group C life tests shall be performed on the initial production lot of actual devices from each wafer lot, in accordance with table IV herein. Group C life tests are not required to be performed on subsequent production lots when all the following conditions are met:

   (a) Subsequent production lots utilize die from the same wafer lot as the initial production lot.

   (b) Wafers or die remaining from the initial production lot are to be stored in dry nitrogen or equivalent controlled storage, and in covered containers.

   (c) No major changes to the assembly processes have occurred since the group C test was performed on the wafer lot.

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c. Table V, group D test requirements for package technology style characterization testing (see table H-IIA), and group D testing on the initial production lot utilizing the package family of interest, shall be in accordance with MIL-PRF-38535 and the manufacturer's approved QM plan. A package family consists of a set of package types with the same package configuration (e.g., BGA, CGA), material type (e.g., alumina, beryllium oxide (BeO)), package construction techniques (e.g., single layer, multilayer), ball (bumps) and column spacing with identical package assembly techniques (e.g., material and type of seal, ball attach, underfill, solder bumps or wire bond method and wire size, die attach method and material). All new alternate sources of package elements shall be qualified to the applicable group D tests and shall meet paragraph H.3.4.4.1.

d. Group E inspection shall be performed in accordance with table C-I of appendix C. Metal oxide semiconductor (MOS) microcircuits, when specified, shall be tested for time dependent effects post total dose irradiation. When 100 percent latch-up screen is specified, the PDA shall be 5 percent or one device, whichever is greater. The devices used for group E testing shall pass the specified group A electrical tests. An alternate procedure to table C-I group E test may be used upon approval of the qualifying activity.

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APPENDIX B

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APPENDIX C

RADIATION HARDNESS ASSURANCE

C.1 SCOPE

C.1.1 Scope. This appendix presents the requirements which are to be used to supplement MIL-PRF-38535 for device manufacturers supplying radiation hardness assurance (RHA) microcircuits. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

C.2 APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, or C.5 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections C.3, C.4, and C.5 of this appendix, whether or not they are listed.

C.2.2 Government documents.

C.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices.
MIL-HDBK-815 - Dose-Rate Hardness Assurance Guidelines.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

C.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

ASTM F1892 - Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

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JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.

JESD234- Test Standard for the Measurement of Proton Radiation Single Event Effects in Electronics Devices.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

C.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3 REQUIREMENTS

C.3.1 General. Microcircuits supplied to this document shall be manufactured and tested in accordance with approved baseline manufacturing flow and the requirements herein. RHA qualified manufacturer listing (QML) manufacturers shall meet all of the requirements of MIL-PRF-38535 and shall take into consideration all applicable radiation environments as specified herein (C.3.4.1) and the effects that may degrade the devices basic parametric limit or causes failure or damages due to radiation effects. The Technology Review Board (TRB) shall not make major changes to the baselined design rules, processes, procedures, or testing without notifying the qualifying activity prior to implementation of the change.

C.3.2 TRB duties. The TRB duties shall be as outlined in G.3.2.2.

C.3.2.1 TRB/RSS. In the case of a Radiation Source of Supply (RSS) (see 6.4.23), the RSS shall establish a TRB and representatives from the device manufacturer, assembly facility, and test facility shall be part of the TRB. The RSS TRB shall be responsible for all aspects of the device manufacturing process. Details of how all aspects of the device manufacturing processes are controlled shall be documented in the RSS quality management (QM) plan. These include conversion of customer requirements, design, wafer fabrication, assembly, test, RHA testing and verification, and characterization for device specification.

C.3.3 RHA QM plan. A RHA QM plan shall be developed to document the major elements of the manufacturer's QML process (G.3.3). The manufacturer shall establish a Radiation Hardness Assurance Capability Level (RHACL) for the environments and levels specified herein (C.3.4.1) for the procurement document, Standard Microcircuit Drawing (SMD) or data sheet. The RHA QM plan shall be kept current and changes in the RHACL may require a repeat capability demonstration as required by the TRB.

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C.3.3.1 Qualification testing to RHA levels Qualification to a RHA level shall consist of characterization to the highest offered RHA level of total ionizing dose (TID). The conditions for radiation testing shall consist of exposing the devices in a step-stress manner to the highest dose level offered and as a minimum the two next consecutive lower RHA levels. The levels are identified as follows: 3 krad(Si), 10 krad(Si), 30 krad(Si), 50 krad(Si), 100 krad(Si), 300 krad(Si), 500 krad(Si), 1 Mrad(Si). The radiation testing plan (QM Plan) and qualification to the appropriate quality and reliability assurance level for device classes B, Q, S, V, Y or T shall be submitted for QA approval. The designator RHA levels are defined below:

RHA levels:

RHA level designator (see 3.6.2.1)	Total ionizing dose (TID) level in Rad (Si)
/ or -	No RHA
M	3 krad(Si)
D	10 krad(Si)
P	30 krad(Si)
L	50 krad(Si)
R	100 krad(Si)
F	300 krad(Si)
G	500 krad(Si)
H	1 Mrad(Si)

C.3.3.1.1 Total Ionizing Dose (TID) test requirements. For characterization of radiation hardness assurance (RHA) devices of total ionizing dose level, manufacturers shall perform TID test in accordance with test method 1019 of MIL-STD-883. Radiation features and test condition shall be included in the device specification “standard microcircuit drawing (SMD)” and M38510 slash sheet. The following test conditions are the minimum requirements for performing total ionizing dose (TID) test.

(a) For pure CMOS technology (Digital CMOS) devices, manufacturers shall perform total ionizing dose (TID) test for irradiation dose rate between 50 to 300 rad(Si)/s (e.g. high dose rate (HDR) condition A) of test method 1019 of MIL-STD-883.

(b) For bipolar or BiCMOS linear or Analog mixed-signal devices, manufacturers shall perform total ionizing dose (TID) test for irradiation dose rate ≤ 10 mrad(Si)/s (e.g. low dose rate (LDR) condition D) and dose rate between 50 to 300 rad(Si)/s (e.g. high dose rate (HDR) condition A) of test method 1019 of MIL-STD-883. Characterization of enhanced low dose rate sensitivity (ELDRS) test is required in accordance with paragraph 3.13.1 of method 1019 of MIL-STD-883.

Note: For MOS devices only, if the maximum dose rate is < 50 rad(Si)/s for the intended application, the parties to the test may agree to perform the TID test at a dose rate ≥ the maximum dose rate of the intended application in accordance TM1019 of MIL-STD-883.

C.3.3.1.2 Accelerated annealing characterization testing. (a) For all MOS microcircuits as defined in section C.3.3.1.1 (a), an accelerated annealing characterization test shall be performed in order to measure and bound any time dependent effects (TDE). (b) For all other microcircuits as defined in section C.3.3.1.1 (b), the accelerated annealing characterization test is optional. The accelerated annealing test may be omitted during production RLAT if the part is acceptance tested at both high and low dose rate or at low dose rate only.

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C.3.3.1.3 Enhanced low dose rate sensitivity (ELDRS) effects test requirements. Microcircuits containing bipolar transistors e.g. Linear bipolar, or BiCMOS or Analog mixed signal device may be susceptible to enhanced low dose rate sensitivity (ELDRS). The low dose rate sensitivity diagnostic protocol outlined in this section is specified in MIL-STD-883 TM1019 but is included herein for reference. The protocol is required for all microcircuits containing bipolar transistors e.g. Linear bipolar, or BiCMOS or Analog mixed signal device as defined in section C.3.3.1.1 (b). If the diagnostic protocol has not been performed, a statement shall be included in the procurement document, Standard Microcircuit Drawing (SMD) alerting the procuring activity to the potential risk of microcircuit failure in low dose rate applications.

C.3.3.1.3.1 ELDRS characterization test to determine if a part exhibits ELDRS. For ELDRS characterization, select a minimum random sample of 21 devices from a population representative of recent production runs and have undergone burn-in .Divide the samples into four groups of 5 each and use the remaining part for a control which means 10 samples are HDR (high dose rate = 50- 300 rad(Si)/s) at 5 bias and 5 unbias; and 10 samples are LDR (low dose rate ≤ 10 mrad(Si)/s) at 5 bias and 5 unbias conditions.

Post irradiation electrical measurements and ELDRS calculation shall be performed in accordance to the paragraph 3.10 of TM1019 .

C.3.3.1.3.1.2 ELDRS parts to determine the irradiation conditions for production or lot acceptance testing. Upon characterization and determination of the parts that exhibit ELDRS, Manufacturer shall be marked those device type series 61, 61, 63 and so forth for the caution of the customer that devices are ELDRS susceptible.

(i) If the part type is known to exhibit ELDRS or has been shown to exhibit ELDRS by the characterization tests in paragraphs 3.13.1.1 then the parts production or radiation lot acceptance testing (RLAT) may be performed using the default low dose rate test at ≤ 10 mrad(Si)/s (Condition D) or an accelerated test (Condition E).

(ii) For the accelerated test a detailed characterization shall be performed to establish the test parameters for the test. The accelerated test approach may include one of the following methods:

(1) A room temperature low dose rate irradiation at a dose rate ≤ 10 mrad(Si)/s,

(2) An elevated temperature irradiation,

3) Combinations of high dose rate tests and elevated temperature anneals,

4) Switched dose rates, or some other form of accelerated testing (for guidance on characterization of ELDRS parts see ASTM F1892 Appendix X2).

The characterization testing of the ELDRS parts must demonstrate that the irradiation test procedure for production or lot acceptance testing will bound the low dose rate response for all critical electrical parameters at a dose rate of ≤ 10 mrad(Si)/s using a combination of overtest and/or parameter delta design margins. Hence the characterization testing shall include irradiation at ≤ 10 mrad(Si)/s, to the specification dose, as a baseline for comparison.

Note: Low dose rate sensitivity shall be indicated in the device specification for those devices that are susceptible to enhanced low dose rate sensitivity (ELDRS) effects. For device type series that are marked 61, 62, 63, and so forth, the designator shall indicate that the device has been characterized/tested for ELDRS and is ELDRS susceptible.

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C.3.3.2 Single event effects (SEE) qualification testing. Single event effects (SEE) testing shall be performed for all RHA designated microcircuits in accordance with the procurement document, Standard Microcircuit Drawing (SMD). Testing may include heavy ion testing and/or proton testing as applicable. The SEE tests shall be as specified in the procurement document and Standard Microcircuit Drawing (SMD) may include but are not limited to single-event latchup (SEL), single-event burnout (SEB), single-event gate rupture (SEGR), single-event upset (SEU), single-event transient (SET), single-event dielectric rupture (SEDR) and single-event functional interrupt (SEFI). SEL, SEB and SEGR are considered destructive effects while SEU and SET are considered non-destructive effects. SEFI is generally a nondestructive phenomenon but in some cases may result in latent damage and risk of subsequent early failure. SEFI shall be considered nondestructive unless otherwise demonstrated by accelerated life testing, at the manufacturer's option of SEE tested samples known to have exhibited SEFI. SEE qualification shall be performed on complete microcircuits or on process-based test structures such as a standard evaluation circuit(SEC) at initial microcircuit qualification and again after substantive design or process changes that may be expected to change the SEE response of the microcircuit. For heavy ion SEE test ASTM standard F1192 and JEDEC standard JESD57 may be used as guidelines, and for Proton SEE test JEDEC standard JESD234 may be used as guidelines.

C.3.3.2.1 SEE testing conditions. When performing SEE tests the manufacturer shall consider the following conditions as a minimum.

(a) The ion or proton beam angle shall be between normal to the die surface and 60° from the normal, inclusive (i.e. $0^o \leq$ angle $\leq 60^o$). Testing at glancing angles (80 – 90°) should be considered for technologies that could show sensitivity to long range low LET ions penetrating multiple structures. Shadowing of the beam by fixturing or package related effects shall be avoided or shall be taken into account if such avoidance is not practical.

(b) The minimum ion fluence shall be 1×10^7 ions/cm^2 or proton fluence of 1×10^{11} protons/cm^2 for each sample tested. For single-event upset testing, a minimum event count of 100 digital bit errors for each sample tested may be used as an alternative to the minimum ion or proton fluence. If multiple error signatures are observed, a minimum of 100 samples should be taken for each error signature.

(c) The heavy ion flux shall be between 10^2 and 10^5 ions/cm^2/s or proton flux shall be between 10^5 and 10^8 protons/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

(d) The particle range shall be adequate to detect latch-up, because the relevant junction is often buried deep below the active chip surface. Range of the ion which shall be sufficiently penetrate well beyond the deepest part of the sensitive volume of the devices to detect latch-up.

(e) The test temperature shall be the maximum specified operating temperature ±10% for destructive SEL testing and shall be 25°C ± 10°C for SEB and SEGR and nondestructive SEE testing SEU, SET and SEFI.

(f) The SEE testing bias configuration shall be as specified in C.3.3.2.2 or JESD57.

C.3.3.2.2 SEE testing bias configurations. During SEE testing the samples shall be biased in accordance with the below requirements. Due to potentially competing SEE response mechanisms, actual worst-case conditions should be ascertained separately for each device type. These requirements apply to silicon microcircuits; requirements for other structures such as discrete power MOSFET transistors are not defined in this document.

(a) For nondestructive SEE testing of microcircuits, including SEU, SET and SEFI, the samples shall be configured at minimum operating voltage and maximum clock frequency. If SEFI is encountered during testing it is recommended that failure analysis or DPA be performed to determine if latent damage is present.

(b) For SEL testing of microcircuits the samples shall be configured at maximum operating voltage and maximum operating case temperature.

(c) For SEB testing of microcircuits the samples shall be configured at maximum reverse-bias voltage and minimum operating case temperature.

(d) For SEGR testing of microcircuits the samples shall be configured at maximum operating voltage and room temperature.

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C.3.4 RHA/QML certification requirements. See 3.4.1 herein. In addition to standard flow certification the manufacturer's RHA certification testing shall be performed by a laboratory that has received suitability from the qualifying activity (QA).

C.3.4.1 Process capability demonstration. The manufacturer shall establish a Radiation Hardness Assurance Capability Level (RHACL) for the environments and levels specified in the QM plan, Standard Microcircuit Drawing (SMD). C.3.4.1.1 lists the test requirements for the natural environments consistent with space applications (total ionizing dose (TID), displacement damage (DD) and single-event effects (SEE)). C.3.4.1.2 lists the test requirements for the manmade environments consistent with weapons or nuclear applications (total ionizing dose (TID), displacement damage (DD) and transient effects (dose rate)). Changes in the RHACL may require a repeat capability demonstration as required by the TRB.

C.3.4.1.1 Natural environments. These environments are found in space, atmospheric and terrestrial applications and focus on total ionizing dose, displacement damage and single-event effects.

Devices technology	Total ionizing dose (TID) test (TM 1019 of MIL-STD-883)				Neutron/ Displacement damage test 1/ (TM1017)	Proton SEE test 2/ (JSED234)	Heavy ion SEE test 2/
	High dose rate(HDR)	Low dose rate(LDR)	HDR and LDR for ELDRS characterization 3/	TDE			SEL, SEB, SERG, SEDR, SEU, SET and SEFI (JESD57 or ASTM F1192)
Digital CMOS	Required	Optional	Optional	As Required	Optional	Recommended	Required
Linear Bipolar	Optional	Required	Required	Optional	Required	Recommended	Required
BiCMOS or Analog mixed signal device	Required	Required	Required	Optional	Required	Recommended	Required

1/ Neutron, proton and high energy electrons can cause displacement damage in microcircuits devices. The displacement damage test is to be conducted only during initial characterization or upon re-qualification of the device. However, production test can be performed when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

2/ Energetic particles in the space environment (e.g. Galactic cosmic rays (GCR), Solar enhanced particles, and energetic neutron and protons) can affect microcircuit performance. Manufacturers are required to consider space environment for characterization of microcircuit device to be used in space environment. However, heavy ion or proton SEE test shall be performed in production level when specified in the purchase order or contract.

3/ Microcircuits containing bipolar transistors e.g. Linear bipolar, or BiCMOS or Analog mixed signal devices may be susceptible to enhanced low dose rate sensitivity (ELDRS). The low dose rate sensitivity diagnostic protocol outlined in this section is specified in MIL-STD-883 TM1019 but is included herein for reference. The protocol is required for all linear bipolar, or BiCMOS or Analog mixed signal devices as defined in section C.3.3.1.1 (b). If the diagnostic protocol has not been performed, a statement shall be included in the procurement document, Standard Microcircuit Drawing (SMD) alerting the procuring activity to the potential risk of microcircuit failure in low dose rate applications.

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C.3.4.1.2 Manmade environments. These environments are found in weapons and nuclear power applications and focus on total ionizing dose, displacement damage and dose rate (transient) effects.

Devices technology	Total ionizing dose (TID) test (TM 1019 of MIL-STD-883)				Displacement damage test 1/	High dose rate latch up 2/	High dose rate upset 2/	Dose rate survivability 2/
	High dose rate(HDR)	Low dose rate(LDR)	HDR and LDR for ELDRS 3/	TDE	Neutron (TM 1017)	(TM 1020)	(TM 1021)	(TM1023)
Digital CMOS	As required	Optional	Optional	Optional	Optional	As required	As required	As required
Linear Bipolar(BJT)	As required	As required	As required	As required	As required	As required	As required	As required
BiCMOS or mixed signal devices	As required	As required	As required	As required	As required	As required	As required	As required

1/ Neutron can cause displacement damage in microcircuits devices. The displacement damage test is to be conducted only during initial characterization or upon re-qualification of the device. However, production testing shall be performed when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

2/ The weapon or Nuclear environment high dose rate irradiation has an effect on microcircuits devices. However, the high dose rate upset, latch up, and survivability test shall perform in production level testing when specified in the purchase order or contract.

3/ Microcircuits containing bipolar transistors e.g. Linear bipolar, or BiCMOS or Analog mixed signal devices may be susceptible to enhanced low dose rate sensitivity (ELDRS). The low dose rate sensitivity diagnostic protocol outlined in this section is specified in MIL-STD-883 TM1019 but is included herein for reference. The protocol is required for all linear bipolar, or BiCMOS or Analog mixed signal devices as defined in section C.3.3.1.1 (b). If the diagnostic protocol has not been performed, a statement shall be included in the procurement document or Standard Microcircuit Drawing (SMD) alerting the procuring activity to the potential risk of microcircuit failure in low dose rate applications.

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C.3.4.1.3 Design. The manufacturer shall address the design methodology for the following areas of design:

(NOTE: These are also applicable to third party design centers.)

a. Model verification. Model verification shall provide evidence that models defining device response in radiation environments accurately predict the nominal and worst-case circuit response over operating voltage limits and over the temperature range selected for the technology at the RHACL.

b. Design rule verification. The vendor shall document his design rules for radiation hardening his technology and demonstrate his procedures for verifying rule compliance in the context of Design Rules Check (DRC), Electrical Rules Check (ERC) and reliability checking procedures (see G.3.1.b, G.3.4.1.c, H.3.2.1.1.1 b). These rules cover, as a minimum:

(1) DRC: Geometric and physical.

(2) ERC: Shorts and open, connectivity.

(3) Reliability verification: Electromigration (current density), latch-up, electrostatic discharge (ESD), and fuse/anti-fuse reliability.

(4) RHA rules: The vendor shall document their design rules for radiation hardening in their technology and the procedures for verifying rule compliance.

c. Performance verification. The vendor shall demonstrate his ability to predict the response of the post-irradiation performance at the RHACL including the effects of the specified limits for temperature and voltage variations and the influence of process variations (see H.3.2.1.1.1.c). Any deviation from these requirements shall receive qualification activity approval.

C.3.4.1.4 Wafer fabrication. As part of certification, the manufacturer shall identify a specific technology or technologies for the wafer fabrication (see H.3.2.1.2).

a. Statistical process control (SPC) and in-process monitoring program for RHA. SPC is especially critical for maintaining a technology's RHACL. This occurs since relatively minor changes in a process flow can drastically effect device radiation performance. The manufacturer shall identify and document all critical process nodes associated with RHA. See H.3.2.1.3 for a general list of critical process steps, any deviation from this list shall receive qualifying activity approval.

b. Technology characterization vehicle (TCV) program. The TCV program is an integral part of a technology's RHA and shall be carefully configured to ensure the accurate characterization of a technologies radiation capability. The TCV program shall be designed to support RHA activities, parametric extraction, model development and validation, SPC and failure mode analysis. (see H.3.2.2.2.1) The TCV structures shall be used to determine a technology's RHACL and in addition determine failure modes and mechanisms by irradiation to 2x RHACL or failure, whichever comes first. Failure can be either functional or parametric.

c. TCV certification. When radiation hardness is a requirement of the technology, special structures shall be incorporated into the TCV program to characterize the technology's capability for producing devices with assured radiation hardness to the RHACL. To determine that the RHACL is appropriate for the technology, the vendor shall irradiate the TCV to 2x the RHACL or until failure to determine failure mode and mechanism(s). Also, the bounds of the radiation response shall be determined by testing the appropriate TCV test structures for worst case bias conditions, annealing conditions, and temperature.

d. Standard evaluation circuit (SEC). The SEC shall utilize all relevant radiation hardness assurance design rules and

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shall be used to demonstrate the specified level of performance at the RHACL. When radiation hardness assurance is a requirement of the technology, the SEC shall be used to certify and monitor the RHACL of a specific fabrication technology in a specific fabrication facility. The SEC shall be designed so it can be used to assess and monitor the radiation hardness of the fabrication process and design rules (see H.3.4.3). The SEC reliability data, including failure analysis results, shall be available for review by the qualifying activity. For RHA environments, the manufacturer shall irradiate SEC to 2x the requested RHACL or to failure (whichever occurs first) under worst case bias, annealing and temperature conditions as a demonstration of the technology's capability to meet the RHACL. A different SEC may be required whenever the design rules, the materials, the basic processes, or the basic functionality of the technology differ.

e. Process monitor (PM). The process monitor is an integral part of a technology's RHA SPC program for in-line process monitoring. The structures shall be carefully designed and configured to ensure the accurate characterization of a technology's radiation performance and capability. The PM shall support wafer acceptance testing and TCI (see H.3.2.1.3.2). Any deviation from this guidance shall be justified to the qualifying activity.

When RHA is a requirement of the QML line, as a minimum, process monitors for RHA qualified technologies shall include test structures to support the following:

(1) Metal oxide semiconductor (MOS) RHA parameters:

(a) Gate oxide thickness; Structures shall be included to ensure gate oxide thickness since this is a critical parameter affecting radiation performance.

(b) The following parameters shall be measured as a function of total ionizing dose:

(i) Threshold voltage (V_T); The linear V_T for each transistor in a cell.

(ii) Linear transconductance (g_m); The linear g_m for a set of transistors.

(iii) I_{on}/I_{off} (leakage current).

(iv) Propagation delay time (t_{PD}); A test structure in the form of a functional circuit such as an inverter or register chain shall be available to support this measurement.

(v) Field transistor leakage; Field transistor leakage for the minimum design/layout rules.

(2) Bipolar parameters. The bipolar parameters should be those found in H.3.2.1.3.2 c and shall be measured as a function of total ionizing dose and neutron fluence (as appropriate).

(3) Gallium arsenide (GaAs) parameters. The following parameters should be measured as a function of total ionizing dose and neutron/proton fluence (as appropriate).

(a) Sheet resistance.

(b) Isolation; An ohmic transmission line structure should be included to measure contact resistance and transfer length.

(c) FATFET; A long length gate FET suitable for the measurement of Schottky barrier height, ideality factor, carrier concentration, and channel depth should be available.

(d) GaAs FET parameters; see H.3.2.1.3.2 d.

(4) Radiation hardness assurance. When RHA is a requirement of the technology, the PM shall include test

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structures to monitor the following phenomena, as applicable:

(a) Dose-rate latch-up.

(b) Dose-rate upset.

(c) Single-event effects (SEE).

(d) Total ionizing dose.

(e) Displacement damage from neutron or proton irradiation.

(5) Other RHA considerations. In addition, test structures to monitor and characterize radiation response mechanisms and for linear circuit applications shall be included (as appropriate). These structures would include but not be limited to:

(a) Matched transistor pairs for offset current and voltage characterization.

(b) Annular and dual or multi-edged transistor sets for sub threshold I-V characterization.

(c) Four contact devices for charge pumping measurements.

C.3.4.1.5 Wafer acceptance plan. The TRB shall develop and demonstrate a wafer acceptance plan based on electrical and radiation measurement of parametric monitors (PMs). PMs shall be used to determine wafer and wafer lot uniformity and latch-up immunity (when specified). Further testing of the actual device to table C-I may be required. As an option to actual device testing, after initial establishment of device specification and device post-irradiation parameter limits (PIPL), the following procedures are presented as examples for the specified radiation environments:

a. Latch-up: The PM should utilize worst case latch-up structures to determine latch-up holding voltage at maximum temperature. The holding voltage shall be greater than the maximum rated voltage.

b. SEE: The PM should utilize SEE structures such as cross-coupling resistors to memory cells to assure critical parameters agree with worst case acceptance criteria.

c. Dose rate: The PM should utilize structures to ensure rail span collapse does not cause upset or burnout or both and that the metallization resistivity, contact resistance, via resistance, epitaxial layer (EPI), substrate resistivity, and minority carrier lifetime specifications are met.

d. Total ionizing dose: The PM should utilize structures such as capacitors and transistors to ensure that critical parameters agree with worst case PIPL values.

C.3.5 On-site validation. In addition to the requirements in 3.4.1.3 the on-site validation shall include RHA test procedures and RHA data reduction.

C.3.5.1 Technology validation. The general requirements for a technology validation are defined in 3.4.1.4. For RHA technology the following items shall be added:

a. Radiation test procedures.

b. RHA data reduction (e.g., interface state and oxide trapped charge separation).

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C.3.6 RHA packages. Packages used for RHA microcircuits shall be characterized for effects that may influence the hardness of packaged product. Characterization shall include impedance of the power and ground distribution network, impedance contributions of bond wires and die attach, and the impedance associated with any passive elements included as integral parts of the package. Qualification of the same die in different packages shall require demonstration either by test or similarity analysis.

C.3.7 Demonstration vehicles. The demonstration vehicles shall be as described in H.3.4.1.3. Each demonstration vehicle shall operate and perform in compliance with the device specification and to the RHACL for a radiation hardened process (which shall be submitted to the qualifying activity) and shall be manufactured in packages which have been tested to C.3.6 herein prior to use for qualification. For a technology that has die as its primary product, the demonstration vehicle shall be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

C.3.7.1 Qualification test plan. See H.3.4.2. Note that for RHA, the die traceability shall be to the individual wafer.

C.3.7.2 Qualification test report. For RHA testing, the pre and post irradiation, electrical parameters and the transient and SEE test conditions shall be retained by the manufacturer.

C.4 VERIFICATION

C.4.1 Traceability. Traceability to the wafer lot level (for GaAs to wafer level) shall be provided for all delivered microcircuits. Traceability shall document, as a minimum, the completion of each step required in design (when applicable), fabrication, assembly, test and any applicable qualified rework procedure.

C.4.2 Design requirements. The manufacturer shall show evidence that all QML/RHA product has been through the qualified RHA technology flow. For RHA devices, sample testing of each design to verify PIPL shall be conducted to determine total dose and neutron hardness level, dose rate upset threshold, latch-up immunity (when specified) at maximum temperature and voltage, and linear energy transfer threshold (LET_{TH}) for upset and latch-up as well as the cross section for SEE. If simulation models can be verified by test to address these concerns, they would be acceptable. It is anticipated that several designs of each ASIC family shall be tested.

C.4.3 Radiation response characterization. When specified in the acquisition document, radiation response characterization data shall be provided for QML microcircuits in those environments specified in the device specification. The characterization shall be obtained in increments of irradiation levels to failure or to a radiation level at or beyond the specification level as determined by the TRB. The characterization data shall be accompanied by the mean and standard deviation of the critical parameters. The results obtained from table C-I testing herein shall be added to the characterization data (at fluence level, dose rate, and parameter levels defined in the device procurement specification test conditions) periodically.

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C.4.4 End-of-line technology conformance inspection (TCI) testing (option 1). Group E inspection shall include radiation hardness assurance (RHA) tests on each wafer lot. The PIPL, transient and single event phenomenon (SEP) response (as applicable), and test conditions shall be as specified in the device specification. End-of-line TCI testing shall be performed as recommended in table J-I herein. Requirements as detailed in TM 5005 of MIL-STD-883 may be used, with qualifying activity approval, in place of the TCI requirements herein. All group E testing shall be performed on microcircuits to be delivered as RHA QML microcircuits.

Group E inspection is required only for parts intended to be marked as RHA. RHA quality conformance inspection sample tests shall be performed at the level(s) specified and in accordance with table C-I herein. The applicable subgroups of group E shall be performed when specified in the acquisition document. The actual devices used for group E testing shall be assembled in a qualified package and, as a minimum, shall pass table I, group A, subgroups 1, 7, and 9 at +25°C prior to irradiation. If a manufacturer elects to eliminate a quality conformance inspection step by substituting an in-process control or statistical process control procedure, the manufacturer is only relieved of the responsibility of performing the TCI operation associated with that step. The manufacturer is still responsible for providing a product which meets all of the performance, quality, and reliability requirements herein and in the device specification. Documentation supporting substitution for TCI shall be retained by the manufacturer and available to the qualifying activity upon request. For some devices, there are differences in the total dose radiation response before and after burn-in. Unless it has been shown by prior characterization or by design that burn-in has negligible effect (parameters remain within post-irradiation specified electrical limits) on the total dose radiation response, one of the following shall be done:

a. The manufacturer shall subject the radiation samples to the specified burn-in conditions prior to conducting total dose radiation testing.

b. The manufacturer shall develop a correction factor (which is acceptable to the parties to the test) taking into account the changes in total dose response resulting from subjecting product to burn-in. The correction factor shall then be used to accept product for total dose response without subjecting the test samples to burn-in.

C.4.4.1 End-point tests for group E. End-point measurements and other specified post-test measurements shall be made for each sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the detailed specifications. Any additional end-point electrical measurements may be performed at the discretion of the manufacturer.

C.4.5 In-line TCI testing (option 2). In-line control testing shall be performed through the use of the approved SEC or QML microcircuit. The following shall be addressed for RHA devices; group E testing shall be performed on the SEC or product meeting SEC complexity at intervals set by the TRB in the QM plan. Burn-in shall be addressed as per C.4.4 a or C.4.4 b above.

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APPENDIX C

TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V, class Y, class N and Class P.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 1 3/ 4/	Neutron irradiation test (Displacement Damage test) a. Initial qualification test or QCI/TCI test	a.TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot 5/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/	a.TM 1017 at 25°C 2(0) devices/wafer or 5(0) devices/wafer lot or 11(0) devices/inspection lot 5/	a.TM 1017 at 25°C 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	b. Endpoint electrical parameters test	b. As specified in accordance with device specification	b. As specified in accordance with device specification	b. As specified in accordance with device specification	b. As specified in accordance with device specification	b. As specified in accordance with device specification

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TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V, class Y, class N and Class P . –continued.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 2 3/ 7/ 9/ 10/	Total ionization dose (TID) a. Initial qualification test or QCI/TCI test b. Endpoint electrical parameters test	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/ b. As specified in accordance with device specification	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/ or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer b. As specified in accordance with device specification	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/ or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer b. As specified in accordance with device specification	a. TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/ b. As specified in accordance with device specification	a.TM 1019 at 25°C maximum supply voltage 2(0) devices/wafer or 5(0) devices/wafer lot or 22(0) devices/inspection lot 8/ or 1(0) devices/wafer + 4(0) SEC or test structures/wafer or 5(0)devices/wafer lot + 4(0) SEC or test structures/ wafer b. As specified in accordance with device specification

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TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V, class Y, class N and Class P . –continued.

Subgroups	Tests 1/ 2/	MIL-STD-883 test method and conditions Minimum sample size quantity (accept no.)				
		Hermetic classes		Non-hermetic classes		
		Class Q (class level B)	Class V (class level S)	Class Y (ceramic or organic) (class level S)	Class N (PEM) (class level B)	Class P (PEM) (class level S)
Subgroup 3 11/	a. Dose rate upset test (Transient irradiation test	a. For Digital TM 1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0)devices/inspection lot 5/	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/	a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/		a. For Digital TM1021 For Linear TM1023 (temperature at 25°C) 2(0) devices/wafer or 11(0) devices/wafer lot 6/
	b. End point electrical parameters test	b. As specified in accordance with device specification	b. As specified in accordance with device specification	b. As specified in accordance with device specification		b. As specified in accordance with device specification
Subgroup 4 12/	Radiation dose rate induced latch-up test	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification	TM 1020 As specified in the device specification		TM 1020 As specified in the device specification
Subgroup 5 13/	Single event effects (SEE) test		ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification	ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification		ASTM F-1192 or JESD57 4(0) devices or As specified in the device specification

Note: The screening and QCI/TCI tables from MIL-PRF-38535 and MIL-STD-883 Test Methods 5004 and 5005 have been combined for consistency. A future revision of MIL-STD-883 will reflect this change as well. Manufacturers shall document in their QM plan the screening and QCI/TCI requirements to either MIL-PRF-38535 or MIL-STD-883.

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TABLE C-I. Group E (RHA) TCI/QCI test for class Q, class V, class Y, class N and Class P. –continued.

1/ Group E tests may be performed prior to device screening. Parts used for one subgroup test may not be used for other subgroups but may be used for higher levels in the same subgroup. End point electrical parameters as specified in accordance with device specification.

2/ For devices with solder terminations, group E subgroups test may be performed without balls and columns.

3/ The radiation hardness assurance capability level (RHACL)/radiation assurance in the SPEC level is the ratio of the capability level to the specification level of devices fluence. Subgroups shall be invoked when the radiation hardness assurance capability level (RHACL) specification requirements of > 10 are not met. For an example, if RHACL/SPEC ratio is > 10 then this test may not be required, but if the RHACL/SPEC ratio falls within > 1 and ≤ 10 then the subgroup test is required.

4/ This test is to be conducted only when specified in the purchase order or contract. Neutron irradiation test (Displacement damage test) is not required for MOS devices unless bipolar elements are included by design.

5/ In accordance with inspection lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed.

6/ In accordance with wafer lot. If one part fails, seven additional parts may be added to the test sample with no additional failures allowed.

7/ For initial technology qualification, sample shall be randomly chosen and evenly distributed from 3 wafer lots or see H. 3.4.1 for TID test, and minimum RHA level defined based on maximum total ionizing dose level requirements (see C.3.3.1). Parts used for one subgroup test may not be used for other subgroups, but may be used for higher levels in the same subgroup. For subgroup 2, total dose exposure shall not be considered cumulative unless testing is performed within the time limits of the test method.

8/ In accordance with inspection lot. If one part fails, 16 additional parts may be added to the test sample with no additional failures allowed.

9/ Traceability to the specific wafer is required.

10/ In accordance with wafer for device types with greater than or equal to 4,000 equivalent transistors/chip selected from the wafer. The manufacturer shall define and document sampling procedures. The test structures shall be randomly selected from the wafer. An X-ray source may be used on test structures at the wafer level provided correlation has been established between the X-ray and the Cobalt-60 source and shall be documented in the QM plan.

11/ Radiation dose rate upset (Transient irradiation test) test shall be conducted during qualification on first QCI when specified in purchase order or contract.

12/ Radiation dose rate induced latch-up screen test shall be conducted when specified in purchase order or contract. Dose rate induced latch-up screen test is not required when radiation induced latch-up is verified to be not possible such as SOI, SOS and dielectrically isolated technology devices. If radiation dose rate induced latch-up screen test is required, shall be performed screening operation after seal. Test conditions, temperature, and the electrical parameters to be measured pre, post, and during the test in accordance with the specified device specification. The PDA for each inspection lot for class V, class Y, or class P (class level S) devices sublot, screened, shall be 5 percent or one device, whichever is greater.

13/ When single event effects (SEE) testing is specified in the purchase order or contract, the SEE test shall be performed during initial qualification and after any design or process change that may affect SEE response. Destructive SEE (SEB and SEGR) testing shall be performed accordance with JEDEC standard JESD57.

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APPENDIX C

C.5 NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

C.5.1 Additional reference documents. The documents in this section may be used as guidelines for the development of a hardness assurance program and are not mandatory for this specification.

MIL-PRF-38534	-	Hybrid Microcircuits, General Specification for.
MIL-HDBK-816	-	Guidelines for Developing Radiation Hardness Assurance Device Specifications.
MIL-HDBK-817	-	System Development Radiation Hardness Assurance.
MIL-HDBK-1547	-	Electronic Parts, Materials, and Processes for Space and Launch Vehicles.
SD-18	-	Defense Standardization Guide for Part Requirements and Applications.

(Copies of these documents are available online at https://quicksearch.dla.mil/.)

ASTM INTERNATIONAL (ASTM)

ASTM E666	-	Standard Practice for Calculating Absorbed Dose from Gamma or X Radiation.
ASTM E668	-	Standard Practice for Application of Thermo Luminescence-Dosimetry (TLD) Systems for Determining Absorbed Dose in Radiation-Hardness Testing of Electronic Devices.
ASTM F744	-	Standard Test Method for Measuring Dose Rate Threshold for Upset of Digital Integrated Circuits.
ASTM F773	-	Measuring Dose Rate Response of Linear Integrated Circuits (Metric).

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

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APPENDIX D

STATISTICAL SAMPLING, TEST, AND INSPECTION PROCEDURES

D.1 SCOPE

D.1.1 Scope. This appendix contains statistical sampling, life test, and qualification procedures used with microcircuits. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

D.2 APPLICABLE DOCUMENTS

(This section is not applicable to this appendix.)

D.3 REQUIREMENTS

D.3.1 Definitions. The following definitions shall apply for all statistical sampling procedures:

a. Sample size series: The sample size series is defined as the following decreasing series of values: 50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1, 0.7, 0.5, 0.3, 0.2, 0.15, and 0.1.

b. Tightened inspection: Tightened inspection is defined as inspection performed using the next sample size value in the sample size series lower than that specified.

c. Acceptance number (c): The acceptance number is defined as an integral number associated with the selected sample size which determines the maximum number of defectives permitted for that sample size.

d. Rejection number (r): Rejection number is defined as one plus the acceptance number.

D.3.2 Symbols. The following symbols shall apply for all statistical sampling procedures:

a. Acceptance number (c).

b. Rejection number (r).

D.4 STATISTICAL SAMPLING PROCEDURES AND TABLE

D.4.1 General. Statistical sampling shall be conducted using the sample size method. The sample size method as specified herein is a sampling plan which provides a high degree of assurance that a lot having a percent defective greater than or equal to the specified sample size value shall not be accepted. The procedures specified herein are suitable for all quality conformance requirements.

D.4.1.1 Selection of samples. Samples shall be randomly selected from the inspection lot or inspection sublots. For continuous production, the manufacturer, at their option, may select the sample in a regular periodic manner during manufacture provided the lot meets the formation of lots requirement.

D.4.1.2 Failures. Failure of a unit for one or more tests of a subgroup shall be charged as a single failure.

D.4.2 Single-lot sampling method. Quality conformance inspection information (sample sizes and number of observed defectives) shall be accumulated from a single inspection lot to demonstrate conformance to the individual subgroup criteria.

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D.4.2.1 Sample size. The sample size for each subgroup shall be determined from table D-I or D-II and shall meet the specified sample size series. The manufacturer may, at their option, select a sample size greater than that required; however, the number of failures permitted shall not exceed the acceptance number associated with the chosen sample size in table D-I or D-II. In table D-II, the sample size series column to be used for sample size determination shall be that given in the lot size column which is nearest in value of the actual size of the submitted lot, except that if the actual lot size is midway between two of the lot sizes given in the table, either of the bounding lot size columns may be used at the manufacturer's option. If, in table D-II, the appropriate lot size column does not contain a sample size series value equal to or less than the specified sample size series value, 100 percent inspection shall be used. In table D-II, the sample size series value in the appropriate lot size column that is numerically closest to the specified sample size series value shall be used to determine the sample size.

D.4.2.2 Acceptance procedure. For the first sampling, an acceptance number shall be chosen and the associated number of sample devices for the specified sample series selected and tested (see D.4.2.1). If the observed number of defectives from the first sample is less than or equal to the preselected acceptance number, the lot shall be accepted. If the observed number of defectives exceeds the preselected acceptance number, an additional sample may be chosen such that the total sample complies with D.4.2.3. The table (D-I or D-II), which is used for the first sampling of a given inspection lot for a given subgroup shall be used for any and all subsequent samplings for the same lot and subgroup for each lot submission.

D.4.2.3 Additional sample. The manufacturer may add an additional quantity to the initial sample, but this may be done only once for any subgroup and is limited to the initial sample (e.g., does not apply to resubmitted lots after initial failure). The added samples shall be subjected to all the tests within the subgroup. The total sample size (initial and added samples) shall be determined by the new acceptance number selected from table D-I or D-II).

D.4.2.4 Multiple criteria. When one sample is used for more than one acceptance criterion, the entire sample for a subgroup shall be used for all criteria within the subgroup. In table D-I, the acceptance number shall be that one associated with the largest sample size in the appropriate sample size series column which is less than or equal to the sample size used. In table D-II, the acceptance number shall be that one associated with the specified samples size series, in the appropriate lot size column, for the sample size used.

D.4.2.5 One hundred percent inspection. Inspection of 100 percent of the lot shall be allowed, at the option of the manufacturer, for any or all subgroups other than those which are called "destructive". If the observed percent defective for the inspection lot exceeds the specified samples size series value, the lot shall be considered to have failed the appropriate subgroup(s). Resubmission of lots tested on a 100 percent inspection basis shall also be on a 100 percent inspection basis only and in accordance with the tightened inspection sample series value and other requirements of A.4.3.3.1.

D.4.2.6 Tightened inspection. Tightened inspection shall be performed by testing to the criteria of the next sample size series value lower than that specified in the series 1, 1.5, 2, 3, 5, and 7 times 10^n, where n is an integral number.

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TABLE D-I. Sample size series (SSS) sampling plan. 1/ 2/ 3/

Percent defective allowable (PDA) / Sample size series	50	30	20	15	10	7	5	3	2	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
Acceptance number (C) (r = c + 1)	Minimum sample sizes (For device-hours required for life test, multiply by 1000)																
0	5 (1.03)	8 (0.64)	11 (0.46)	15 (0.34)	22 (0.23)	32 (0.16)	45 (0.11)	76 (0.07)	116 (0.04)	153 (0.03)	231 (0.02)	328 (0.02)	461 (0.01)	767 (0.007)	1152 (0.005)	1534 (0.003)	2303 (0.002)
1	8 (4.4)	13 (2.7)	18 (2.0)	25 (1.4)	38 (0.94)	55 (0.65)	77 (0.46)	129 (0.28)	195 (0.18)	258 (0.14)	390 (0.09)	555 (0.06)	778 (0.45)	1296 (0.027)	1946 (0.018)	2592 (0.013)	3891 (0.009)
2	11 (7.4)	18 (4.5)	25 (3.4)	34 (2.24)	52 (1.6)	75 (1.1)	105 (0.78)	176 (0.46)	266 (0.31)	354 (0.23)	533 (0.15)	759 (7.59)	1065 (0.080)	1773 (0.045)	2662 (0.031)	3547 (0.022)	5323 (0.015)
3	13 (10.5)	22 (6.2)	32 (4.4)	43 (3.2)	65 (2.1)	94 (1.5)	132 (1.0)	221 (0.62)	333 (0.41)	444 (0.31)	668 (0.20)	953 (0.14)	1337 (0.10)	2226 (0.062)	3341 (0.041)	4452 (0.031)	6681 (0.018)
4	16 (12.3)	27 (7.3)	38 (5.3)	52 (3.9)	78 (2.6)	113 (1.8)	158 (1.3)	265 (0.75)	398 (0.50)	531 (0.37)	798 (0.25)	1140 (0.17)	1599 (0.12)	2663 (0.074)	3997 (0.049)	5327 (0.037)	7994 (0.025)
5	19 (13.6)	31 (8.4)	45 (6.0)	60 (4.4)	91 (2.9)	131 (2.0)	184 (1.4)	308 (0.85)	462 (0.57)	617 (0.42)	927 (0.28)	1323 (0.20)	1855 (0.14)	3090 (0.085)	4638 (0.056)	6181 (0.042)	9275 (0.028)
6	21 (15.6)	35 (9.4)	51 (6.6)	68 (4.9)	104 (3.2)	149 (2.2)	209 (1.6)	349 (0.94)	528 (0.62)	700 (0.47)	1054 (0.31)	1503 (0.22)	2107 (0.155)	3509 (0.093)	5267 (0.062)	7019 (0.047)	10533 (0.031)
7	24 (16.6)	39 (10.2)	51 (7.2)	77 (5.3)	116 (3.5)	166 (2.4)	234 (1.7)	390 (1.0)	589 (0.67)	783 (0.51)	1178 (0.34)	1680 (0.24)	2355 (0.17)	3922 (0.101)	5886 (0.067)	7845 (0.051)	11771 (0.034)
8	26 (18.1)	43 (10.9)	63 (7.7)	85 (5.6)	128 (3.7)	184 (2.6)	258 (1.8)	431 (1.1)	648 (0.72)	864 (0.54)	1300 (0.36)	1854 (0.25)	2599 (0.18)	4329 (0.108)	6498 (0.072)	8660 (0.054)	12995 (0.036)
9	28 (19.4)	47 (11.5)	69 (8.1)	93 (6.0)	140 (3.9)	201 (2.7)	282 (1.9)	471 (1.2)	709 (0.77)	945 (0.58)	1421 (0.38)	2027 (0.27)	2842 (0.19)	4733 (0.114)	7103 (0.077)	9468 (0.057)	14206 (0.038)
10	31 (19.9)	51 (12.1)	75 (8.4)	100 (6.3)	152 (4.1)	218 (2.9)	306 (2.0)	511 (1.2)	770 (0.80)	1025 (0.60)	1541 (0.40)	2199 (0.28)	3082 (0.20)	5133 (0.120)	7704 (0.080)	10268 (0.060)	15407 (0.040)
11	33 (21.0)	54 (12.8)	83 (8.3)	111 (6.2)	166 (4.2)	238 (2.9)	332 (2.1)	555 (1.2)	832 (0.83)	1109 (0.62)	1664 (0.42)	2378 (0.29)	3323 (0.21)	5546 (0.12)	8319 (0.083)	11092 (0.062)	16638 (0.042)
12	36 (21.4)	59 (13.0)	89 (8.6)	119 (6.5)	178 (4.3)	254 (3.0)	356 (2.2)	594 (1.3)	890 (0.86)	1187 (0.65)	1781 (0.43)	2544 (0.3)	3562 (0.22)	5936 (0.13)	9804 (0.086)	11872 (0.065)	17808 (0.043)
13	38 (22.3)	63 (13.4)	95 (8.9)	126 (6.7)	190 (4.5)	271 (3.1)	379 (2.26)	632 (1.3)	948 (0.89)	1264 (0.67)	1896 (0.44)	2709 (0.31)	3793 (0.22)	6321 (0.134)	9482 (0.089)	12643 (0.067)	18964 (0.045)
14	40 (23.1)	67 (13.8)	101 (9.2)	134 (6.9)	201 (4.6)	288 (3.2)	403 (2.3)	672 (1.4)	1007 (0.92)	1343 (0.69)	2015 (0.46)	2878 (0.32)	4029 (0.23)	6716 (0.138)	10073 (0.092)	13431 (0.069)	20146 (0.046)
15	43 (23.3)	71 (14.1)	107 (9.4)	142 (7.1)	213 (4.7)	305 (3.3)	426 (2.36)	711 (1.41)	1086 (0.94)	1422 (0.71)	2133 (0.46)	3046 (0.33)	4265 (0.235)	7108 (0.141)	10662 (0.094)	14216 (0.070)	21324 (0.047)
16	45 (24.1)	74 (14.6)	112 (9.7)	150 (7.2)	225 (4.8)	321 (3.37)	450 (2.41)	750 (1.44)	1124 (0.96)	1499 (0.72)	2249 (0.48)	3212 (0.337)	4497 (0.241)	7496 (0.144)	11244 (0.096)	14992 (0.072)	22487 (0.048)
17	47 (24.7)	79 (14.7)	118 (9.86)	158 (7.36)	236 (4.93)	338 (3.44)	473 (2.46)	788 (1.48)	1182 (0.98)	1576 (0.74)	2364 (0.49)	3377 (0.344)	4728 (0.246)	7880 (0.148)	11819 (0.098)	15759 (0.074)	23639 (0.049)
18	50 (24.9)	83 (15.0)	124 (10.0)	165 (7.54)	248 (5.02)	354 (3.51)	496 (4.96)	826 (1.5)	1239 (1.0)	1652 (0.75)	2478 (0.50)	3540 (0.351)	4956 (0.251)	8260 (0.151)	12390 (0.100)	16520 (0.075)	24780 (0.050)
19	52 (25.5)	86 (15.4)	130 (10.2)	173 (7.76)	259 (5.12)	370 (3.58)	518 (2.56)	864 (1.53)	1296 (1.02)	1728 (0.77)	2591 (0.52)	3702 (0.358)	5183 (0.256)	8638 (0.153)	12957 (0.102)	17276 (0.077)	25914 (0.051)
20	54 (26.1)	90 (15.6)	135 (10.4)	180 (7.82)	271 (5.19)	386 (3.65)	541 (2.60)	902 (1.56)	1353 (1.04)	1803 (0.78)	2705 (0.52)	3864 (0.364)	5410 (0.260)	9017 (0.156)	13526 (0.104)	18034 (0.078)	27051 (0.052)
25	65 (27.0)	109 (16.1)	163 (10.8)	217 (8.08)	326 (5.38)	466 (3.76)	652 (2.69)	1086 (1.61)	1629 (1.08)	2173 (0.807)	3259 (0.538)	4656 (0.376)	6518 (0.269)	10863 (0.161)	16295 (0.108)	21726 (0.081)	32589 (0.054)

1/ Sample sizes are based upon the Poisson exponential binomial limit.
2/ The minimum quality (approximate acceptable quality level (AQL)) required to accept (on the average) 19 of 20 lots is shown in parenthesis for information only.
3/ Minimum size of sample to be tested to assure with a 90 percent confidence that a lot having percent-defective equal to the specified sample size series value will not be accepted (single sample).

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TABLE D-II. Hypergeometric sampling plans for small homogenous lot sizes of 200 or less.
(N = lot size, n = sample size, c = acceptance number).

N	10		20		30		40		50		60		80		100		120		150		160		200	
n	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS	AQL	SSS
C = 0																								
2	2.2	85	2.5	86	2.5	67	2.5	67	2.5	67	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68	2.5	68
4	1.2	36	1.2	40	1.2	42	1.2	42	1.3	42	1.3	43	1.3	43	1.3	43	1.3	43	1.3	44	1.3	44	1.3	44
5	1.0	29	1.0	34	1.0	34	1.0	35	1.0	35	1.0	35	1.0	36	1.0	36	1.0	37	1.0	37	1.0	37	1.0	37
8	0.5	15	0.6	20	0.6	22	0.6	23	0.6	23	0.6	23	0.6	24	0.7	24	0.7	24	0.7	24	0.7	24	0.7	25
10			0.4	15	0.5	17	0.5	19	0.5	19	0.5	19	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20	0.5	20
16			0.2	6.9	0.25	10	0.25	11	0.3	11	0.3	12	0.3	12	0.3	13	0.3	13	0.3	13	0.3	13	0.3	13
20					0.2	6.8	0.2	8.0	0.25	8.7	0.25	9.0	0.25	9.4	0.25	10	0.25	10	0.25	10	0.25	10	0.25	11
25					0.15	4.3	0.15	3.7	0.2	6.4	0.2	6.9	0.2	7.4	0.2	7.5	0.2	7.6	0.2	7.7	0.2	7.8	0.2	7.9
32							0.1	3.7	0.1	4.4	0.1	5.0	0.1	5.5	0.1	5.9	0.15	6.0	0.15	6.2	0.15	6.3	0.15	6.3
40									0.1	3.0	0.1	3.4	0.1	4.0	0.1	4.5	0.1	4.6	0.1	4.9	0.1	5.0	0.1	5.0
50											0.1	2.3	0.1	2.9	0.10	3.3	0.1	3.5	0.10	3.7	0.1	3.7	0.10	3.9
64													0.08	1.7	0.08	2.2	0.06	2.5	0.06	2.7	0.06	2.8	0.06	2.9
80															0.07	1.5	0.07	1.7	0.07	2.0	0.07	2.1	0.07	2.2
100																	0.05	1.1	0.05	1.5	0.05	1.5	0.05	1.7
125																			0.04	0.8	0.04	0.9	0.04	1.2
128																			0.04	0.8	0.04	0.9	0.04	1.1
160																							0.03	0.7
C = 1																								
2	27	95	24	95	24	95	23	95	23	95	23	95	23	95	23	95	23	95	22	95	22	95	22	95
4	15	62	12	66	12	66	11	67	11	67	10	67	10	67	10	67	10	67	9.8	67	9.7	67	9.7	68
5	13	51	10	55	8.8	56	8.5	57	8.4	57	8.1	58	7.9	58	7.6	58	7.5	58	7.5	58	7.5	58	7.5	58
8	11	28	7.2	35	6.2	38	5.8	38	5.4	39	5.0	39	4.7	39	4.5	39	4.3	39	4.3	40	4.2	40	4.2	40
10			6.2	30	5.0	30	4.6	31	4.2	32	4.2	22	4.2	32	3.9	32	3.5	33	3.3	33	3.3	33	3.3	33
16			5.6	15	4.2	18	3.8	18	3.4	20	3.0	20	2.9	21	2.6	21	2.5	21	2.3	21	2.3	22	2.2	22
20					4.0	13	3.2	15	2.8	16	2.5	16	2.4	16	2.3	16	2.1	17	2.0	17	2.0	17	2.0	18
25					3.8	9.2	3.1	11	2.5	12	2.2	13	2.0	13	1.8	13	1.7	13	1.6	14	1.6	14	1.6	14
32							3.1	7.4	2.4	8.2	2.1	9.0	1.8	9.9	1.6	10	1.5	10.5	1.4	11	1.3	11	1.3	11
40									2.4	5.9	2.1	6.8	1.6	7.8	1.4	7.8	1.3	8.2	1.2	8.3	1.2	8.4	1.1	8.6
50											1.7	4.6	1.4	5.6	1.2	6.1	1.2	6.4	1.0	6.5	0.9	6.7	0.9	6.7
64													1.3	3.8	1.1	4.4	1.0	4.7	0.8	5.0	0.8	5.0	0.7	5.2
80															1.1	3.0	1.0	3.4	0.8	3.7	0.7	3.8	0.6	4.0
100																	0.9	2.5	0.7	2.8	0.7	2.8	0.6	3.0
125																			0.7	1.9	0.7	2.0	0.5	2.2
128																			0.7	1.7	0.7	1.9	0.5	2.2
160																							0.5	1.5
C = 2																								
4	33	82	28	83	27	84	27	85	27	85	26	85	26	85	26	86	26	86	25	86	25	86	25	86
5	27	69	23	73	21	74	20	74	20	74	20	75	20	75	19	75	19	75	19	75	19	75	19	75
8	22	42	15	49	14	49	13	52	13	52	13	52	12	53	12	53	12	53	11	53	11	53	11	53
10			13	39	11	42	11	42	10	43	10	43	9.6	43	9.2	44	9.1	44	8.9	44	8.9	44	8.7	44
16			11	12	8.6	25	6.9	27	6.8	27	6.4	27	6.0	28	6.0	29	5.9	29	5.9	29	5.7	29	5.5	30
20					7.7	19	6.2	21	5.9	22	5.6	22	5.1	23	4.8	23	4.8	23	4.6	23	4.5	24	4.5	24
25					7.4	13	6.0	16	4.9	17	4.5	17	4.3	18	4.1	18	3.9	18	3.7	18	3.7	19	3.7	19
32							5.5	11	4.8	12	4.3	13	3.6	14	3.4	14	3.2	14	3.0	14.5	3.0	15	2.9	15
40									4.6	8.9	3.9	9.8	3.1	11	2.8	12	2.6	12	2.4	12	2.4	12	2.3	12
50											3.5	6.9	2.8	8.1	2.4	8.4	2.3	8.6	2.1	9.0	2.1	9.3	2.0	9.5
64													2.6	5.7	2.2	6.2	2.0	6.6	1.8	7.1	1.7	7.1	1.6	7.4
80															2.1	4.5	1.8	4.9	1.6	5.4	1.5	5.4	1.4	5.6
100																	1.8	3.5	1.4	3.9	1.4	4.0	1.2	4.4
125																			1.4	2.8	1.3	2.9	1.1	3.3
128																			1.4	2.6	1.3	2.9	1.1	2.2
160																							1.1	2.3

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TABLE D-II. Hypergeometric sampling plans for small homogenous lot sizes of 200 or less. - Continued.

Table D-II gives the acceptable quality level (AQL) and sample size series (SSS) values associated with certain single sampling plans (acceptance number, sample size, and lot size). The table has the following features:

a. Calculations are based upon the hypergeometric distribution (exact theory) for lot sizes 200 or less.

b. The AQL of a sampling plan is defined as the interpolated percent defective for which there is a 0.95 probability of acceptance under the plan. The AQL so defined need not be a realizable lot percent defective for the lot size involved (e.g., 12 percent is not a realizable percent defective for a lot size of 20).

c. The sample size series of a sampling plan is defined as the interpolated percent defective for which there is a 0.10 probability of lot acceptance under the plan. The sample size series value so defined need not be a realizable lot percent defective for the lot size involved.

d. The sequence of sample sizes and lot sizes are generated by taking products of preceding numbers in the respective sequences.

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APPENDIX D

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APPENDIX E

PROVISIONS GOVERNING THE CERTIFICATION AND QUALIFICATION OF OFFSHORE PROCESSES

(This appendix has been deleted in its entirety.)

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APPENDIX E

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APPENDIX F

GENERAL PROVISIONS FOR TAPE AUTOMATED BONDED MICROCIRCUITS

F.1 SCOPE

F.1.1 Scope. This appendix contains provisions for tape automated bonded (TAB) microcircuits. It provides design guidelines, in-process controls, screening and technology conformance inspection (TCI) requirements, and general manufacturing guidelines in order to produce a compliant TAB microcircuit. It is intended for use in conjunction with a manufacturer's compliancy program. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. However, for QML microcircuits the manufacturers may offer approved alternatives that demonstrate a process control system that achieves at least the same level of quality and reliability as could be achieved by this appendix.

F.2 APPLICABLE DOCUMENTS

F.2.1 General. The documents listed in this section are specified in sections F.3 or F.4 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections F.3 and F.4 of this appendix, whether or not they are listed.

F.2.2 Government documents.

F.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

F.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JESD22-A101 - Steady-State Temperature Humidity Bias Life Test.
JESD22-A112 - Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices.
J-STD-020D.01 - Joint IPC/JEDEC Standard for Moisture/Reflow Sensitivity Classification For Non-hermetic Solid State Surface Mount Devices.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

F.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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F.3 REQUIREMENTS

F.3.1 Marking. Marking shall be in accordance with the device specification and in an appropriate medium. The following should be used as guidance: Marking may be in ink, laser marked or etched in the copper of the lead frame tape. Ink-marking may be performed before or after burn-in. Ink-marked parts shall be subjected to resistance to solvents (TM 2015 of MIL-STD-883, (see F.4.7.2.1 herein)). In either the ink-marked or tape design case, the following should be included on each device:

a. On the excised portion of the tape (that portion which remains with the microcircuit):

(1) Name of manufacturer or Commercial and Government Entity (CAGE) code.

(2) Inspection lot date code (determined by the date of final assembly operation, such as date of encapsulation or date of bonding operation).

b. The following should also be marked on each device, but location may be on the non-excised portion of the tape, the individual device carrier, or the excised portion of the tape at the manufacturers option:

(1) Part or identifying number (PIN).

(2) Electrostatic discharge (ESD) identifier.

(3) Compliance indicator or certification, whichever is applicable.

(4) Serialization, if applicable.

F.3.2 Process monitors. The applicable process monitors of A.3.4.1.2 shall be performed. The quality assurance provisions described below within this appendix shall be used to address some of these process monitors.

F.3.3 Lead finish. Lead finish shall be gold, designated a "C", unless otherwise specified in the device specification.

F.3.4 Item requirements. The individual item requirements for TAB microcircuits delivered under this appendix shall be documented in the device specification prepared in accordance with 3.5 of this specification.

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F.4 VERIFICATION

F.4.1 General operation flow. The following represents the general operational flow that TAB microcircuits follow.

Reference paragraph	Operation
F.4.6.1	Internal visual (optional)
F.4.3	Bump (100 percent)
F.4.3.1	Bump visual
F.4.4.1	Bond process characterization (100 percent)
F.4.4.2	Visual inspection of bond Visual
F.4.6.2	Internal visual (100 percent)
F.4.5	Encapsulant (optional)
F.4.5.1	Encapsulant visual
F.4.6.3	Temperature cycle (100 percent)
F.3.1	Mark (100 percent)
F.4.6.4	Pre burn-in electrical (optional)
F.4.6.4	Burn-in (100 percent)
F.4.6.4	Post burn-in electrical (100 percent)
F.4.6.5	PDA
F.4.6.6	External visual (100 percent)
F.4.7	Quality conformance inspection

F.4.2 Tape. Procurement of tape shall be baselined by the manufacturer to include the following items F.4.2 a through F.4.2 f. Items e and f shall be sampled on a frequency basis necessary to demonstrate process control.

a. Design configuration.

b. Tape composition.

c. Coefficient of thermal expansion.

d. Test for delamination of layers.

e. Plating thickness and composition.

f. Dimensions (lead, terminal, external, and window).

F.4.3 Bump. The bump process shall be baselined by the manufacturer to include the following items F.4.3a through F.4.3j. Items F.4.3f through F.4.3j shall be sampled on a frequency basis necessary to demonstrate process control.

a. Minimum glassivation overlap.

b. Barrier metal system - deposition, composition.

c. Step coverage (bump to glassivation).

d. Design configuration.

e. Thickness of barrier metal.

f. Thickness of bump.

g. Hardness.

h. Bump height uniformity.

i. Bump shear.

j. Bath purity.

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F.4.3.1 Visual examination of bump. Visual examination of the bump is required prior to bond. Sample size and accept/reject limits shall be documented and determined by the manufacturer, and, at a minimum, address the following areas:

a. Alignment of bump to pad.

b. Contaminants, conductive residue.

c. Bleeding bump (metallization exposed to higher than normal temperature excursions).

d. Ineffective or improper photoresist application or removal.

e. Cracks, voids.

f. Partial or missing bumps.

g. Nodules or malformed bumps.

h. Discolored bumps.

I. Mechanically damaged bumps.

F.4.4 Bond. Bond requirements shall be as specified in F.4.4.1 through F.4.4.2 inclusive.

F.4.4.1 Bond process characterization. Process characterization of inner lead bond (ILB) is critical to the quality and reliability of a TAB device and shall be performed and documented to ascertain the minimum, maximum, and mean destructive bond pull limits to meet the requirements set forth herein. During the process characterization the following factors shall be considered and included as appropriate:

a. Tape composition.

b. Bond force.

c. Bond temperature.

d. Bond pressure.

e. Underlying layers such as:

(1) Bump configuration.

(2) Glassivation composition.

(3) Bond pad opening.

f. Any underlying metallization and passivation.

g. Cracking (the manufacturer shall evaluate the significance of any cracking throughout the device including around and below the bump area).

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F.4.4.2 Visual inspection of bond. Visual inspection of bond is required prior to encapsulation. Sample size and accept/reject limits shall be documented and determined by the manufacturer, and, at a minimum, shall include the following criteria:

a. ILB lead to bump alignment.

b. Lead contact length; bond lead contact length (L) shall be greater than the lead width (W). (See figure F-1.)

c. Lead side edge overhang shall be evaluated.

d. No open/lifted, peeling, or missing leads.

e. No visual shorts.

f. Cracks in bumps, thin film gold bump pad, glassivation, metal, or active area adjacent to the inner lead bond bumps shall not exceed the characterization requirements in F.4.4.1.

g. For single point bonds, the tool impression shall cover 100 percent of the lead to bump contact width.

h. For alloy bonds, fillet shall be visible on at least one side of the lead continuously across the bump.

F.4.5 Encapsulant. The following items a - h, as a minimum, shall be baselined by the manufacturer, and items g - h shall be sampled on a frequency basis necessary to demonstrate process control.

a. Coefficient of thermal expansion and relationship to underlying layers.

b. Presence of volatile components.

c. Gel time and temperature.

d. Cure profile (initial, ramp, and final): Time and temperature.

e. Final properties of cured polymer.

f. Storage of encapsulant.

g. Thickness.

h. Viscosity.

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F.4.5.1 Visual examination of encapsulant. Visual inspection of the applied encapsulant post-cure is required. Sample size and accept/reject limits shall be documented and determined by the manufacturer, and, at a minimum, address the following areas:

a. Cracks.

b. Voids.

c. Lack of interfacial adhesion.

d. Poor uniformity.

e. Stress on underlying layers.

f. Coverage of desired area.

F.4.6 Screening. One hundred percent screening shall be performed in accordance with TM 5004 of MIL-STD-883, with the following deletions and additions:

F.4.6.1 Optional internal visual. An optional internal visual examination may be performed prior to bump utilizing applicable criteria within TM 2010 of MIL-STD-883 or manufacturer's internal criteria in order to screen die defects. Sample size and accept/reject criteria shall be determined and documented by the manufacturer.

F.4.6.2 Internal visual screen. One hundred percent internal visual examination shall be performed prior to encapsulant utilizing applicable criteria within TM 2010 of MIL-STD-883 to screen die defects. At the manufacturer's option, bump visual and ILB visual may be combined with this internal visual examination provided 100 percent of the product is examined.

F.4.6.3 Temperature cycle. One hundred percent temperature cycle shall be performed in accordance with TM 1010 of MIL-STD-883, test condition C.

F.4.6.4 Burn-in. One hundred percent pre, interim, and post burn-in electrical test shall be performed in accordance with the device specification. One hundred percent burn-in shall be performed in accordance with TM 1015 of MIL-STD-883.

F.4.6.5 Percent defective allowable (PDA). PDA shall be calculated in accordance with TM 5004 of MIL-STD-883.

F.4.6.6 External visual. One hundred percent external visual examination shall be performed in accordance with TM 2009 of MIL-STD-883 or manufacturer's applicable external criteria.

F.4.7 Quality conformance inspection (QCI). QCI shall be performed in accordance with TM 5005 of MIL-STD-883 with the following deletions and additions:

F.4.7.1 Group A inspection. Group A inspection shall be in accordance with TM 5005 of MIL-STD-883 and the applicable device specification.

F.4.7.2 Group B inspection. Group B inspection shall be in accordance with the following:

F.4.7.2.1 Resistance to solvents. Resistance to solvents (TM 2015 of MIL-STD-883) shall be performed when ink marking is utilized. Sample size shall be in accordance with TM 5005 of MIL-STD-883.

F.4.7.2.2 Attachability. Attachability of the outer lead bond shall be assured as documented in the device specification and shall include sample size and accept/reject limits.

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F.4.7.2.3 Destructive bond strength. Destructive bond strength (TM 2011 of MIL-STD-883) shall be performed, prior to encapsulation, on inner lead bonds and may be performed during the assembly operation, prior to burn-in. Sample size shall be in accordance with TM 5005 of MIL-STD-883. The minimum value of destructive bond strength shall be documented in the device specification. Defect criteria shall include identification of the site of failure at one or more of the following areas:

a. Lead lift.

b. Lead break at bump.

c. Lead break away from bump.

d. Lead break at tape window.

e. Metal peels off tape.

f. Bump delamination from thin film metal.

g. Thin film metal delamination.

h. Crater under bump.

i. Not bonded.

j. Error (operator, machine, hook slips, etc.).

F.4.7.2.4 Constant acceleration. Constant acceleration (TM 2001 of MIL-STD-883, test condition E (min), Y1 direction only) shall only be required if documented in the device specification.

F.4.7.3 Group C inspection. Group C inspection shall be performed in accordance with TM 1005 of MIL-STD-883. Sample size shall be in accordance with table IV herein or TM 5005 of MIL-STD-883. Initial group C test shall be completed utilizing TAB packaging, while subsequent group C inspections may be performed utilizing alternate packaging technology.

F.4.7.4 Group D inspection. Group D inspection shall be in accordance with TM 5005 of MIL-STD-883 with the following deletions and additions:

a. Subgroup 1 of table IV shall be performed as specified.

b. Subgroups 2, 6, 7, and 8 of table IV of TM 5005 shall not be performed.

c. Subgroup 3 of table IV of TM 5005 shall be performed as specified with the exception of moisture resistance (TM 1004) and seal (TM 1014).

d. Subgroup 4 of table IV of TM 5005 shall be performed as specified with the exception of constant acceleration (unless specified in the device specification) (TM 2001) and seal (TM 1014).

e. Subgroup 5 of table IV of TM 5005 shall be performed as specified with the exception of seal (TM 1014).

F.4.7.4.1 Highly accelerated stress testing (HAST). HAST shall be performed in accordance with J-STD-020, and shall be performed using a sample size number (accept number) of 15(0) for 50 hours at +130°C at 85 percent relative humidity and a voltage bias applied. As an option, 85/85 testing in accordance with JESD22-A101 shall be performed using 15(0) sample size (accept number) for 1,000 hours.

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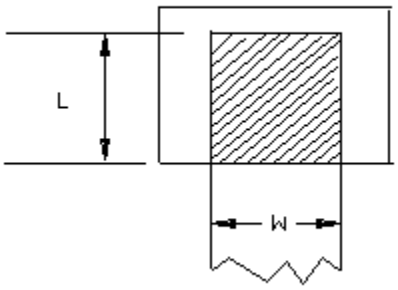
F.4.7.4.2 Post-test visual examinations. Post-test visual examinations shall be performed in accordance with F.4.6.6 of this appendix.

F.4.8 Major changes. Major changes shall be as set forth in MIL-PRF-38535 as applicable. In addition, the following shall be considered as a major change:

a. Any change to baselined items in this appendix.

b. Bond characterization parameters.



L > W

FIGURE F-1. Lead contact length.

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APPENDIX G

THE QUALIFIED MANUFACTURERS LISTING PROGRAM

G.1 SCOPE

G.1.1 Scope. The Qualified Manufacturers Listing (QML) program measures and evaluates the manufacturers' manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. Changes to the process baseline can be made by the manufacturer's Technology Review Board (TRB) after achieving QML status with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of the quality management (QM) program including the TRB, the QM plan, and change control procedures. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. However, for QML microcircuits the manufacturers may offer approved alternatives that demonstrate a process control system that achieves at least the same level of quality and reliability as could be achieved by this appendix.

G.2 APPLICABLE DOCUMENTS

G.2.1 General. The documents listed in this section are specified in section G.3 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in section G.3 of this appendix, whether or not they are listed.

G.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

G.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

SAE International

EIA557 - Statistical Process Control Systems.

(Copies of these documents are available online at https://www.sae.org/ or from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096)

G.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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G.3 REQUIREMENTS. The requirements of the microcircuits are classified in the generic qualification flow diagram (see figure G-1).

G.3.1 QM program. A quality management program shall be developed and implemented by the manufacturer and documented in the QM plan (see G.3.3 herein). Also, the manufacturer shall have a self-assessment program with an evaluation system similar to that posed by the Malcolm Baldridge National Quality Award, and the results of this assessment shall be made available for review. The manufacturer is encouraged to apply for the Malcolm Baldridge National Quality Award within 5 years of initial request for QML status.

G.3.2 Manufacturer's review system. The manufacturer's review system, known as the TRB, is responsible for development of the QM plan, maintenance of all certified and qualified processes, process change control (see 3.3.4), reliability data analysis, failure analysis, corrective actions, QML microcircuit recall procedures, and qualification status of the technology.

G.3.2.1 Organizational structure. The manufacturer's TRB should insure communication is established and maintained among representatives from device design, technology development, wafer fabrication, assembly, testing, quality assurance and third party organizations. Records of the TRB deliberations and decisions should be maintained. These records shall be made available to the qualifying activity (QA). The manufacturer shall submit the name(s) and telephone numbers of their TRB systems' contact person(s) to the QA.

G.3.2.2 TRB duties. The TRB shall keep the QA updated on the status of QML technology and products. The TRB should have a methodology in place for assessing the current status of the quality and reliability of its microcircuits by review of the Statistical Process Control (SPC) procedures and QM status of the manufacturer's process technology, reliability test data (e.g., parametric monitor (PM), Technology Characterization Vehicle (TCV), Standard Evaluation Circuit (SEC) and device), and the Failure Analysis (FA) results of burn-in/screening failures and board/assembly failures and field returns, as applicable. A method or procedure to verify correlation between test structures and actual product should be approved by the TRB. The TRB shall maintain records, available for QA review, of conditions found and the action taken. The TRB is required to report periodically to the QA on the status of the QML technology and products (see G.3.2.3 herein). The TRB should also address the impact of key managerial/TRB personnel changes and business plans in order to evaluate any impact they may have on the QML system.

When the reliability data indicates corrective action is required, the TRB should determine and implement the appropriate action in a timely manner. The SEC and TCV (see G.3.3f herein) data are to be used as a tool for monitoring the quality and reliability of the manufacturer's line and do not automatically disqualify a manufacturer when trends or limits require corrective action.

When reliability of shipped microcircuits is called into question, the TRB should provide evaluation and corrective action and prompt notification to the QA to preserve the manufacturer's qualified status and assure that defective product is not shipped.

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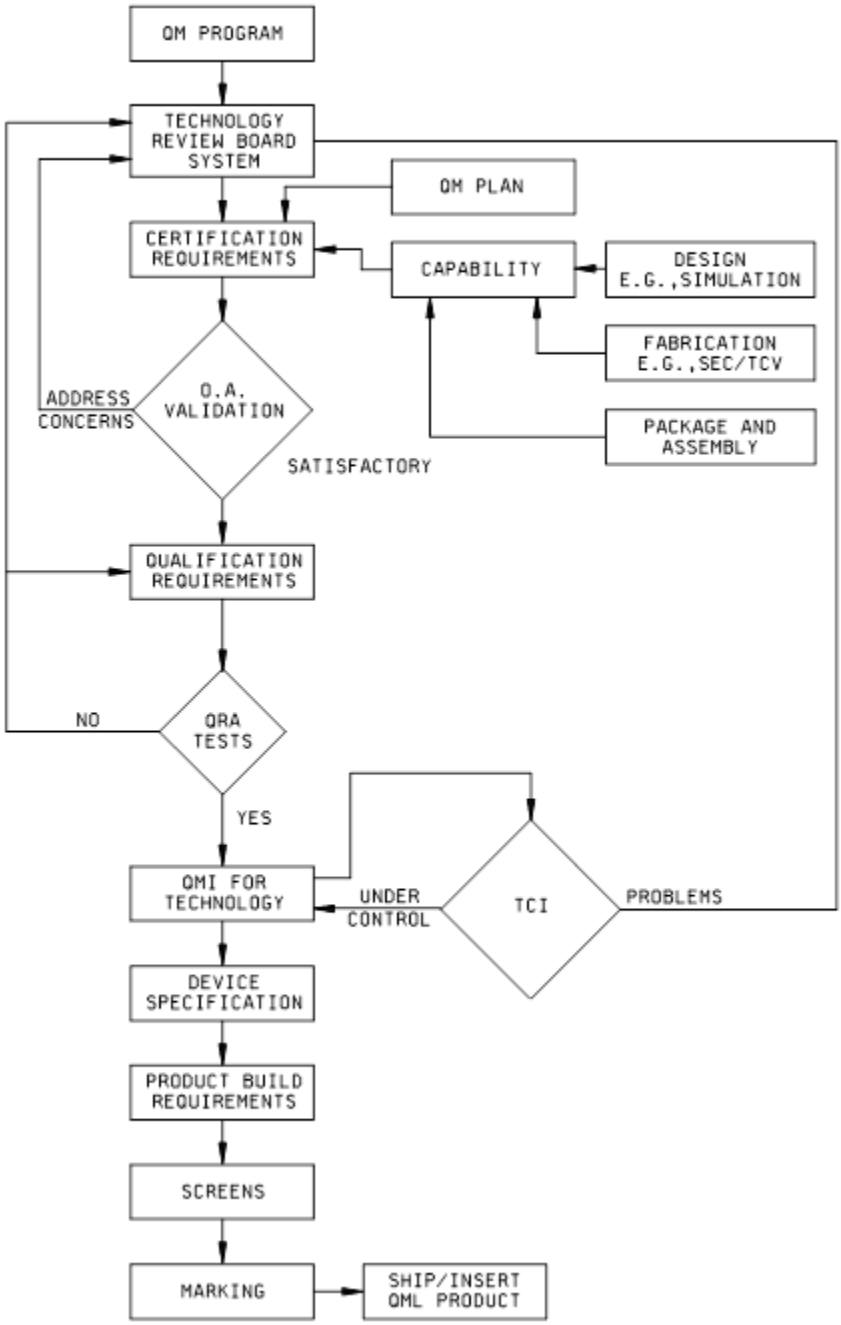

FIGURE G-1. Generic qualification flow diagram.

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G.3.2.2.1 QML certification and qualification test plan (see G.3.3g). Before a management and technology validation is scheduled, the manufacturer should submit to the QA a TRB approved test plan with milestone charts outlining the tests to be used to certify processes and the tests and devices to be used to qualify the certified processes to the requirements of 3.4.1. The TRB shall determine the tests to be accomplished on the TCV, SEC, and parametric monitor and submit to the QA a test plan with parametric limits and accept and reject criteria.

G.3.2.3 Status report. The manufacturer's TRB shall submit a status report to the QA describing the health of the QML manufacturer's line including all changes and the criticality of the changes in microcircuit quality, reliability, performance, and interchangeability. The manufacturer should retain the support test data. The QA can request to review the supporting data. The following areas should be addressed in each status report: (The information in the status report may be addressed in various ways, such as, copies of TRB meeting minutes, summary of major actions, etc.)

a. Field returns and corrective actions.

b. SPC and continuous improvement program update (e.g., defect density summary, in-process reliability monitors, Capability Index of process center (Cpk) programs, etc.).

c. SEC and TCV test data summary, including radiation data if applicable.

d. Design facility.

e. Fabrication line.

f. Assembly facility.

g. Test facility.

h. Major changes.

i. Newly qualified packages.

j. Third party activities.

k. Yield issue trends and corrective actions.

The interval of the status reports to the QA shall be determined by the TRB, but should be as a minimum, quarterly for the first year following the attainment of QML status and as a minimum, semiannually (no further than six months apart) thereafter. If major problems with the technology are encountered, more frequent reports may be required by the QA to keep informed of the status. In addition to the above report, the manufacturer shall make a presentation yearly to the QA outlining the status of the technology, products offered, future trends and other strategic business plans of the technology including foreseen changes. At the discretion of the QA, this presentation may be in lieu of a status report.

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G.3.3 QM plan. The TRB shall oversee and approve the QM plan consisting of the following activities and initiatives, as a minimum:

a. Quality improvement plan. This plan documents the specific procedures to be followed by the manufacturer to assure continuous improvement in quality, and reliability of the process and the product being produced.

b. Failure analysis program. This program establishes the procedures that a manufacturer self-imposes to test and analyze sufficient failed parts to determine each failure category from all stages of manufacturing and the field. This program should also identify corrective actions or specify the use of a corrective action plan based on the findings of the failure analysis.

c. SPC plan. A specific plan defining the manufacturer's SPC program, within the manufacturing process, to the requirements of SAE EIA557.

d. Corrective action plan. This plan should specify the specific steps followed by the manufacturer to correct any process that is out of control or found to be defective.

e. Change control program. This program addresses the process by which a manufacturer addresses changes to the technology. Further information of areas to be considered critical for change control are outlined in G.3.4 herein.

f. SEC and TCV assessment program. The frequency, testing methods, and criteria for evaluations of the SEC or the TCV or both, including correlation of test structures and actual product, are to be determined by the TRB based on the manufacturer's assessment of risk. The manufacturer's SEC and TCV evaluation plan shall be documented.

g. Certification and qualification plan. The certification and qualification plan should be defined in appendix H including self-assessment and corrective actions.

h. Retention of data. This program establishes the requirements for data retention (see A.4.8.1.2 as a guideline).

G.3.3.1 QM plan outline. The following should be addressed in the QM plan. Submittal of the QM plan is required before the validation (certification) meeting.

NOTE: Many of these items and their associated documentation may be reviewed during the validation.

a. Index of certified baseline documents. A list of the specification titles, document numbers, and revisions that make up the QML program. This is the baseline the manufacturer was certified to at a validation review.

b. Conversion of customer requirements. A system for converting all customer's requirements into in-house requirements. This includes determining if certification and QML coverage exist. The following are both part of the QM plan and the manufacturer's conversion system:

(1) Device specification requirements to Standard Microcircuit Drawing (SMD).

(2) Controlled design procedures and tools (established geometric, electrical, and reliability design rules).

(3) Mask generation procedure within the controlled design procedures of G.3.3.1b.(2).

(4) Wafer fabrication and assembly capabilities baselined.

(5) Design, mask, fabrication, assembly, and test flows.

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(6) QML listing coverage.

(7) SEC, TCV or alternate assessment procedure, and PM programs and test procedures (see G.3.3f).

(8) Incoming inspection and vendor procurement document covering design, mask, fabrication, and assembly.

(9) Screening and traveler.

(10) Technology conformance Inspection (TCI) procedures, including identification of destructive/nondestructive classification of tests.

(11) Marking.

(12) Rework.

c. Functional organization chart covering the TRB, quality assurance, and production.

d. Change control program (see G.3.4 herein). This item shall consist of a system by which changes to the QML program are classified and necessary actions taken. The following shall be addressed, as a minimum:

(1) Major changes.

(2) Required testing.

(3) TRB responsibility (e.g., notification policy).

(4) TRB of MIL-PRF-38535 program interface for DLA Land and Maritime.

e. Failure analysis (see G.3.3 b).

f. Self-audit program and audit results.

g. TRB reporting to DLA Land and Maritime, including checklist and procedure.

h. Yield improvement program (see G.3.3 a).

i. SPC program (SAE EIA557 should be used as a guideline) including, goals and plans of implementation, in-line Process Monitors , SPC measurement points (including location and procedure number on applicable flow charts; see G.3.3 c).

j. List of test methods for laboratory suitability including any outside lab.

k. Major test methods for which data may be requested to be submitted:

(1) Burn-in.

(2) Temperature cycle.

(3) Fine and gross leak.

(4) Particle impact noise detection (PIND).

(5) Temperature/humidity testing.

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(6) Preconditioning (board assembly/rework simulation.)

(7) Wafer (lot) acceptance.

(8) Internal visual.

(9) Nondestructive bond pull (NDBP).

(10) Scanning electron microscope (SEM) or nondestructive SEM.

(11) Life test.

(12) Radiographic inspection.

(13) Radiation testing.

l. Calibration.

m. Retention of qualification.

n. Training.

o. Cleanliness and atmospheric controls.

p. Electrostatic discharge (ESD) sensitivity program.

q. Certification and qualification test plan (see G.3.2.2.1).

r. Process for control of third party activities.

s. Characterization procedures for new technology validation.

G.3.4 Change control procedures. The following paragraphs outline areas of concern where a change may require action by the manufacturer. All changes to any part of a QML manufacturer's line are to be governed by the manufacturer's TRB and made available to the QA. All changes should be documented as to the reason for the change with supporting data taken to support the change, including reliability data as appropriate. The decision as to the criticality of the change shall be guided by the potential effect of the change on quality, reliability, specified radiation hardness assurance levels (when applicable), performance and interchangeability of the resulting microcircuits. For any change that merits consideration for requalification, the TRB should decide if requalification is needed. Microcircuits should be shipped following a change only upon approval of the TRB. Modifications to screens and TCI's are allowed but shall be justified, documented, and submitted to the QA. Notification of the change should be made concurrently to the QA for a period of not less than one year after initial QML listing. Thereafter, notification should be made in the TRB status reports (see G.3.2.3 herein). The manufacturer may make notification of this change of product through the Government-Industry Data Exchange Program (GIDEP) using the Product Change Notice; in any case, the manufacturer should assure that all known acquiring activities are notified. For major changes to class level “S” microcircuits, the manufacturer’s TRB shall notify the QA who will coordinate with the space community of changes prior to shipment. The manufacturer shall review all changes for applicability to previous test optimizations and alternate test methods.

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G.3.4.1 Design methodology change. Changes in the design methodology to be evaluated by the TRB shall include, but not be limited to, changes in the following areas:

a. Technology database (cell/design library).

b. Design flow.

c. Design system (computer automated design (CAD), design rules).

d. Software updates.

e. Model or modeling procedures.

f. Configuration management.

g. Radiation hardness assurance (RHA) (if applicable).

h. Electrical performance.

i. Geometry size reduction.

G.3.4.2 Fabrication process change. Changes in the fabrication process to be evaluated by the TRB shall include, but not be limited to, changes in the following areas:

a. Fabrication process sequence or process limits.

b. Fabrication process materials or material specifications, including epitaxial (EPI) layer thickness.

c. Photoresistive materials or material specifications.

d. Doping material source, concentration, or process technique (e.g., ion implantation versus diffusion).

e. Cross section diffusion profile.

f. Passivation or glassivation material, thickness or technique (including addition or deletion of passivation).

g. Metallization system (pattern, material, deposition or etching technique, line width or thickness).

h. Baseline or equivalent.

i. Conductor, resistor, or dielectric materials.

j. Wafer fabrication move from one line, or building, to another.

k. Passivation, or glassivation, process temperature and time.

l. Oxidation or diffusion process, oxide composition and thickness, oxidation temperature and time.

m. Sintering or annealing temperature and time.

n. SEC and how it is tested.

o. Method of mask making.

p. Parametric monitor and how it is tested.

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q. Wafer acceptance criteria.

r. TCV and how it is tested.

s. Sample plans (quantity and acceptance numbers).

t. Gate formation process, material, technique.

u. Backside process to include wafer thinning and backside metallization.

v. Ohmic contact formation.

w. Starting material qualification (e.g., gallium arsenide (GaAs) boule).

x. Lot formation.

G.3.4.3 Assembly process change. Changes in the assembly process to be evaluated by the TRB shall include, but not be limited to, changes in the following areas:

a. Die attach material, method, or location.

b. Wire/ribbon bond interconnect method.

c. Wire material composition and dimensions.

d. Seal technique (materials or sealing process, gas composition (e.g., for RHA)).

e. Implementation procedures for internal visual and other test methods.

f. Assembly flow.

g. Assembly operation move.

h. Scribing and die separation method.

i. TCI procedures including manufacturer imposed tests.

j. Screening tests.

k. Sample plans (quantity and acceptance numbers).

l. Die back surface preparation.

m. Bond pad geometry, spacing, or metallization.

n. Molding material, method, or location.

o. Chip encapsulation/coating material and technique.

p. Device marking process.

q. Lot formation.

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G.3.4.4 Package change. Changes in the package qualification to be evaluated by the TRB shall include, but not be limited to, changes in the following areas:

a. Vendor.
b. External dimensions.
c. Cavity dimensions.
d. Number of leads or terminals.
e. Lead or terminal dimensions (length times width or diameter).
f. Lead or terminal base material.
g. Lead or terminal plating material.
h. Lead or terminal plating thickness (range of).
i. Body material.
j. Body plating material.
k. Body plating thickness (range of).
l. Die pad material.
m. Die pad plating.
n. Die pad plating thickness (range of).
o. Lid material.
p. Lid plating materials (range of).
q. Lid plating thickness (range of).
r. Lid seal (preform) material.
s. Lid glass seal material.
t. Lead glass seal material.
u. Lead glass seal diameter (range of).
v. Leads or terminals spacing.
w. Lead configuration (e.g., J-lead, gull-wing).
x. Die size.
y. Device marking process.
z. Lead attachment.

G.3.4.5 Test facility change. Changes in the test facility to be evaluated by the TRB shall include, but not be limited to, changes in the following areas:

a. Implementation procedures for internal visual and other test methods.
b. Testing flow.
c. Test facility (with laboratory suitability) move from one facility or building to another.
d. Sample plans (quantity and acceptance numbers).
e. Test procedures (including test vector generation).
f. Lot formation.

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APPENDIX G

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APPENDIX H

CERTIFICATION, VALIDATION, AND QUALIFICATION

H.1 SCOPE

H.1.1 Scope. The qualified manufacturers listing (QML) program applies quantifiable measurement techniques that evaluate a manufacturer's ability to define and follow a baseline of its process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the methods used to evaluate and document these changes have been reviewed and approved. Once QML status is achieved, the manufacturer's Technical Review Board (TRB) may approve change(s) to the process baseline based on appropriate reliability and quality data upon concurrence with notification of the Qualifying Activity (QA). The approach outlined in this appendix contains a proven baseline that includes details of the certification, validation, and qualification programs. The necessary characterization, screening, and qualification testing applicable to new technologies is also included. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. However, for QML microcircuits the manufacturers may offer approved alternatives that demonstrate a system that achieves at least the same level of quality and reliability as could be achieved by this appendix.

H.2 APPLICABLE DOCUMENTS

H.2.1 General. The documents listed in this section are specified in section H.3. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in section H.3 whether or not they are listed.

H.2.2 Government documents.

H.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-M-38510 - Microcircuits, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

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H.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

SAE International

EIA557 - Statistical Process Control Systems.
SAE ARP6537 - Risk Mitigation for Pb-free Solders Used Internally to Parts

(Copies of these documents are available online at https://www.sae.org/ or from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP121	- Requirements for Microelectronic Screening and Test Optimization.
JEP163	- Selection of Burn-in/Life Test Conditions and Critical Parameters for QML Microcircuits.
JESD31	- General Requirements for Distributors of Commercial and Military Semiconductor Devices.
JESD78	- IC Latch-up Test.
JESD471	- Symbol & Label for Electrostatic Sensitive Devices.
JESD625	- Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices.
JESD22-B101	- External Visual.
JESD22-A102	- Accelerated Moisture Resistance - Unbiased Autoclave.
JESD22-A104	- Temperature Cycling.
JESD22-A106	- Thermal Shock.
JESD22-A110	- Highly Accelerated Temperature and Humidity Stress Test (HAST) – biased.
JESD22-B117	- Solder Ball Shear test.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

ANSI/ESDA/JEDEC JOINT STANDARD

ANSI/ESDA/JEDEC JS-001 - For Electrostatic Discharge Sensitivity Testing - Human Body Model (HBM) – Component Level.

ANSI/ESDA/JEDEC JS-002 - For Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level.

(Copies of these documents are available online at https://www.jedec.org/ or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.) or

(Copies of these documents are available online at https://www.esda.org/ or from Electrostatic Discharge Association(ESDA)
7900 Turin Road, Bldg. 3, Rome, NY 13440.)

EIA/IPC/JEDEC JOINT STANDARD

EIA/IPC/JEDEC J-STD-002 - Solderability Tests for Component Leads, Terminations, Lugs, Terminals and Wires

(Copies of these documents are available online at https://www.techstreet.com) or

(Copies of these documents are available online at https://www.ipc.org) or

(Copies of these documents are available online at https://www.jedec.org)

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APPENDIX H

ASTM INTERNATIONAL (ASTM)

ASTM D2863	- Standard Test Method for Measuring the Minimum Oxygen Concentration to Support Candle-Like Combustion of Plastics (Oxygen Index).
ASTM F1269	- Test methods for Destructive Shear Testing of Ball Bonds.
ASTM G21	- Standard Practice for Determining Resistance of Synthetic Polymeric Materials to Fungi.
ASTM E1640	- Standard Test Method for Assignment of the Glass Transition Temperature by Dynamic Mechanical Analysis.
ASTM E-1356	- Standard Test Method for Assignment of the Glass Transition Temperatures by Differential Scanning Calorimetry
ASTM D7028	- Standard for Glass Transition Temperature (DMA Tg) of Polymer Matrix Composites by Dynamic Mechanical Analysis (DMA)
ASTM E1545	- Standard Test Method for Assignment of the Glass Transition Temperature by Thermomechanical Analysis was also mentioned.

(Copies of these documents are available online at https://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA 19428-2959.)

UNDERWRITERSLABORATORIES INC. (UL)

UL 94	- Tests for Flammability of Plastic Materials for Parts in Devices and Appliances.

(Copies of this document are available online at https://www.ul.com/ or from Underwriters Laboratories Inc. (UL), 333 Pfingsten Road, Northbrook, IL 60062-2096.)

H.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein (except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

H.3 REQUIREMENTS

H.3.1 General. The qualifying activity (QA) shall evaluate the manufacturer's approach to the process baseline. The manufacturer shall have a quality management (QM) plan specifying the characterization, certification, and qualification plans of technologies and product (see appendix G). New technologies shall also be included and have a checklist defining the necessary requirements for calculation/evaluation of failure mechanism, activation energy, characterization plan, qualification plan and validation. The QM plan shall be submitted to the QA for approval (see G.3.3.1s). For class level S product, the manufacturer shall evaluate the changes listed in table A-I in conjunction with the QA to determine if a change should be classified as a new technology.

H.3.1.1 Characterization requirements. Testing performed with the intent to understand the technology part, materials, and processes used to determine an item's capability. The manufacturer should evaluate their process to determine the long term reliability of the product. For class level S product, a detailed characterization plan identifying critical parameters, test conditions, durations, required measurements, sample size, and temperatures shall be documented, including a detailed physics-of-failure analysis considering mechanical, thermal, electrical, and chemical properties that could contribute to failures. A failure modes effects analysis (FMEA) approach must be followed to ensure to the maximum extent possible that all significant failure mechanisms have been defined and appropriate mitigation techniques have been identified.

H.3.1.2 Certification. Validation, by the QA, that the manufacturer has the capability of producing product which meets or exceeds the requirements contained in this specification. The manufacturer shall document the certification plan as documented in their QM plan. The qualifying activity shall be notified if deviations or exception are taken from the approved plan.

H.3.1.3 Validation. Verification by the QA that the manufacturer has met or exceeded the requirements utilizing data,

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demonstration, other approved techniques, or a combination thereof.

H.3.1.4 Transitional certification. Temporary certification (approximately 2 years maximum) given by the QA to manufacturers working toward full QML certification (see H.3.3).

H.3.1.5 Qualification requirements. Evidence that the characterization testing and evaluations of failure mechanisms show the technology meets or exceeds documented requirements. The qualification methodology will vary depending upon the technology. The manufacturer shall document the qualification plan that is applicable to each technology. The qualification testing for new technologies shall consist of standard military test methods as outlined in MIL-PRF-38535, MIL-STD-883, or the QM plan as approved by the QA, including any tests deemed necessary by the characterization and physics-of-failure analysis.

H.3.1.6 New technology requirements. For class level B product, this is a product family, material, or process, that has never been previously characterized and qualified by the manufacturer, and is detailed in the manufacturer's new technology insertion program (see 3.4.1.1.1 and 6.4.44).

For class V, class Y, and class P (class level S), this is a product family, material, or process, that has never been previously characterized and qualified by the manufacturer for space applications, and is detailed in the manufacturer's new technology insertion program (see 3.4.1.1.1, 6.4.44 and B.3.9).

H.3.1.7 Mature technology requirements. A mature technology is one which the manufacturer has previously released to production the techniques, materials, controls, design, and has a continuous reliability monitor plan in place to identify major reliability life-limiting mechanisms and their associated acceleration factors establish activation energy, detect long-term product shifts, and generate process data or established proof of stable process and/or equipment with negligible wear out (see 6.4.45).

H.3.1.8 General QML process flows. The general QML process flows for new suppliers, and existing certified suppliers, providing class level B products is shown in figure H-1, and for new suppliers, and existing certified suppliers, providing class level S products is shown in figure H-2.

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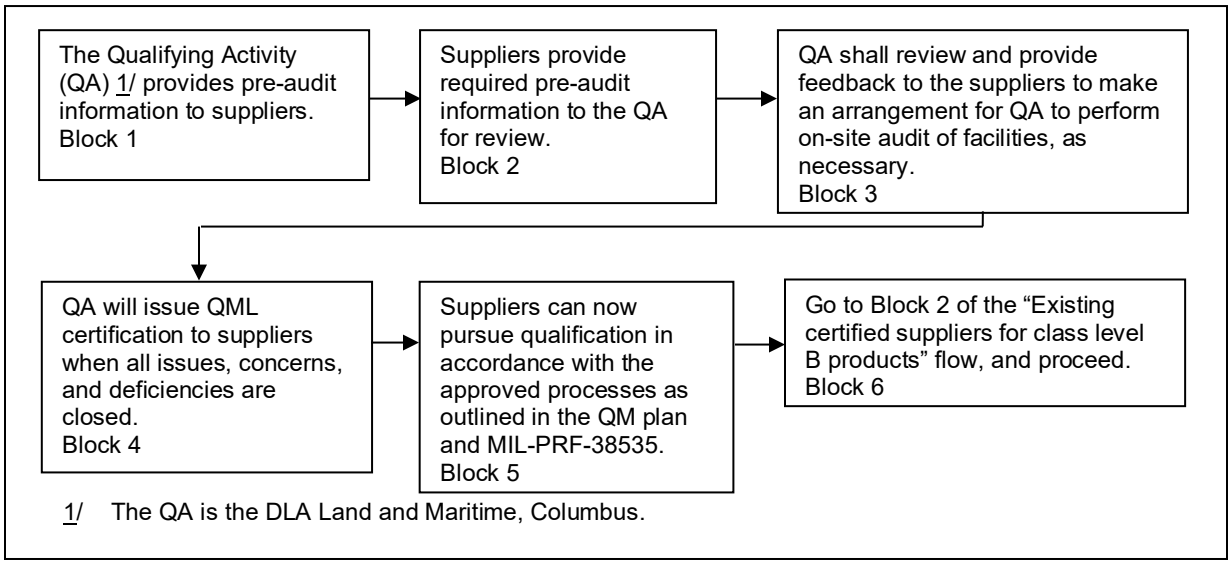
APPENDIX H

New suppliers for class level B products.



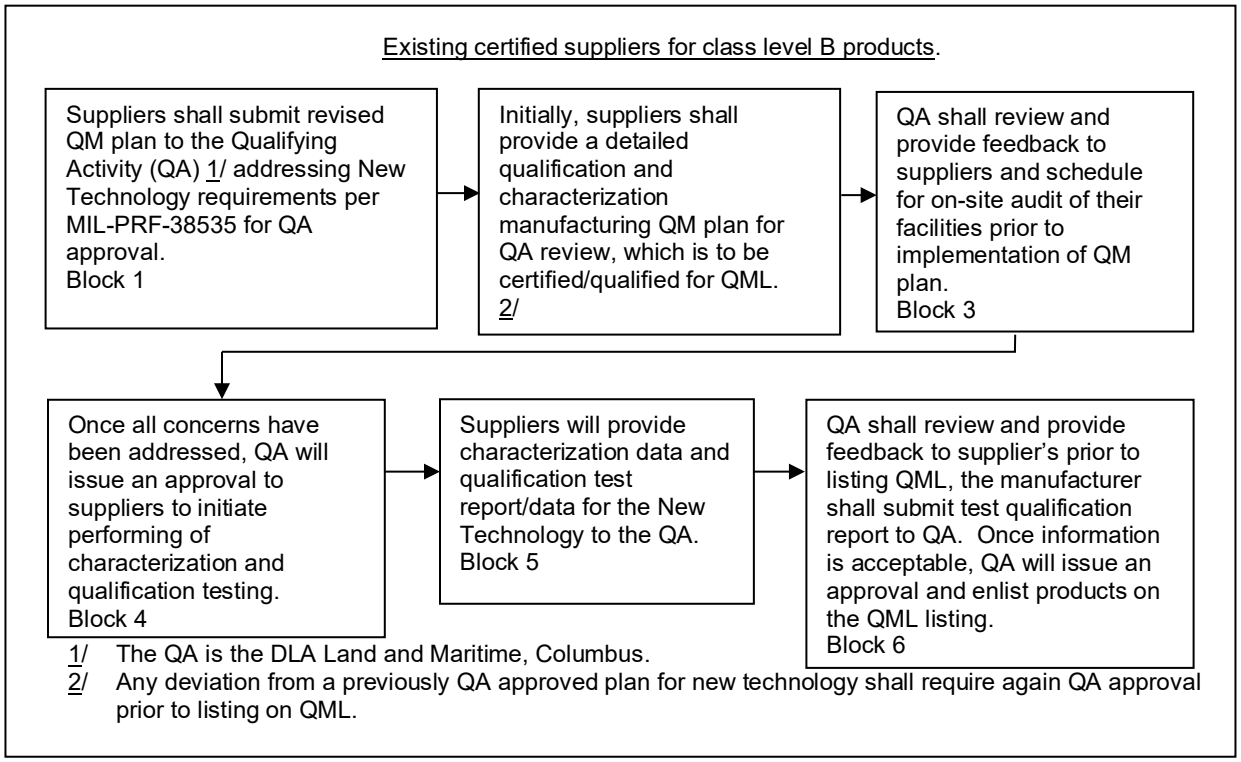


FIGURE H-1. Class level B QML process flows

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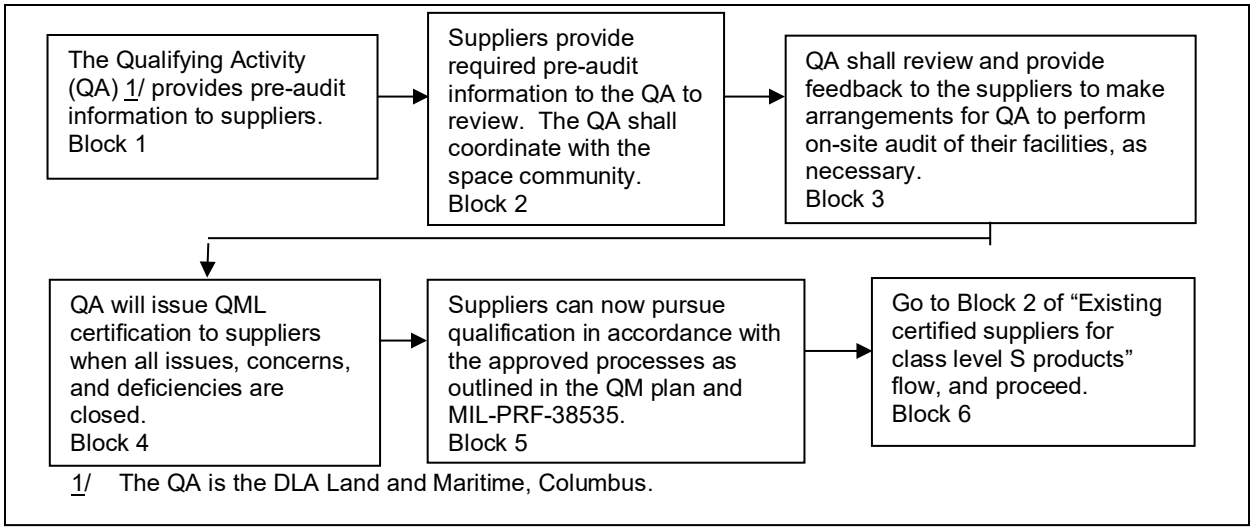
APPENDIX H

New suppliers for class level S products.



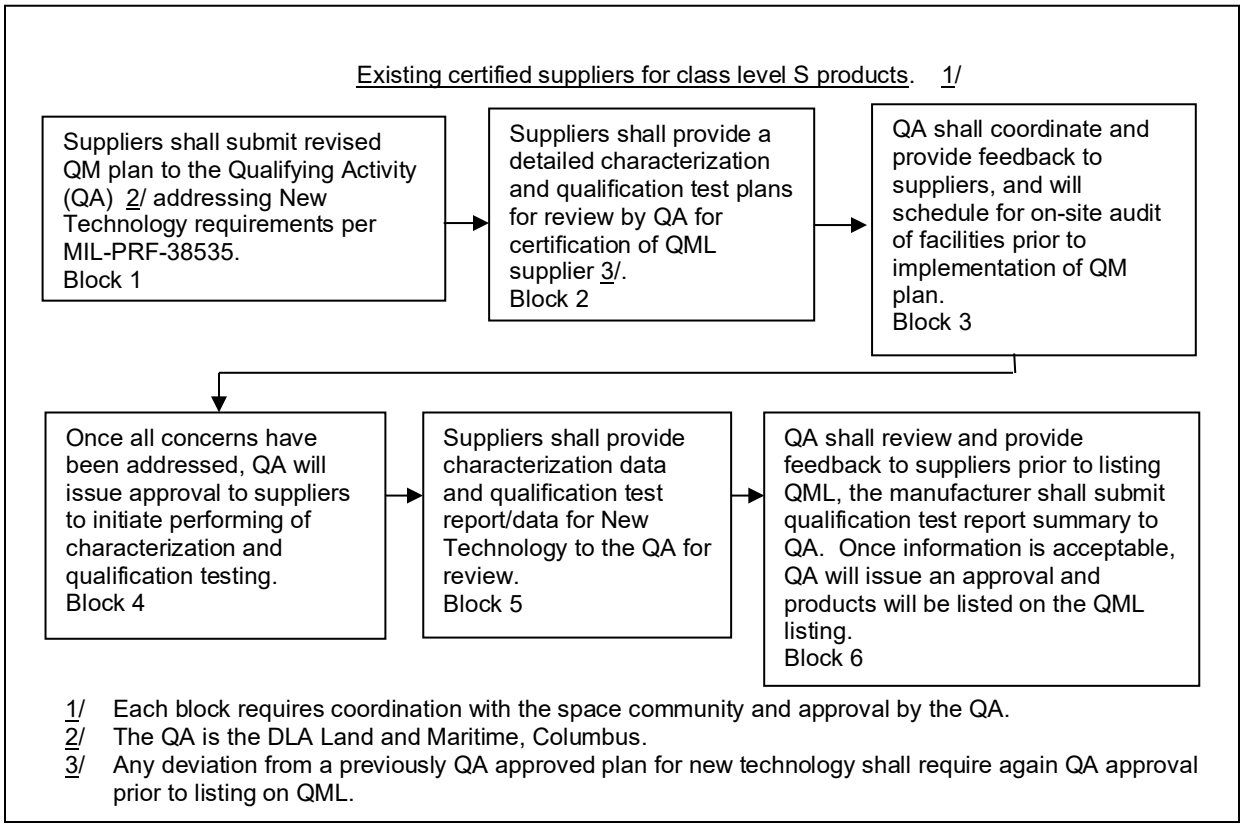


FIGURE H-2. Class level S QML process flows.

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H.3.1.9 Overview of QML Approval Process. The process for achieving QML approval is outlined below in six basic stages and is further described in detail in the subsequent sections. The stages are listed in the normal sequence to be accomplished; however, several stages may occur concurrently.

a) Design, wafer fabrication, assembly, and test certification;
   1) Design methodologies:
      i) Reliability and radiation hardness assurance (RHA) design rules.
   2) Wafer fabrication/foundry processes:
      i) SPC controls
      ii) Metallization controls
      iii) Reliability monitors
   3) Assembly processes
   4) Screening and Test Methodologies
   5) Audit/approval

b) Physics-of-failure/TCV reliability assessment;
   1) Plan approval
      i) Electromigration (EM)
      ii) Time dependent dielectric breakdown (TDDB)
      iii) Hot carrier injection (HCI)
      iv) Threshold voltage instability, including Negative Bias Temperature Instability (NBTI) for 130 nm and smaller CMOS technologies.
      v) Metallization stability over life.
      vi) Others as applicable
   2) Report approval

c) Process technology validation/SEC qualification;
   1) Plan approval
      i) Screening flow
      ii) Process performance characterizations
      iii) Process qualification tests
      iv) For class level B products, life test on a minimum of 1 wafer lot for 1000 hrs minimum at 125°C ambient, or equivalent.
      v) For class level S products, long term life test shall meet the requirements of paragraph B.3.4, appendix B, or shall meet long term life test on a minimum of 1 wafer lot for 4,000 hours minimum at 125°C ambient, or equivalent.
   2) Report approval

d) Product qualification (From existing qualified process technology)
   1) Plan approval
      i) Screening flow
      ii) Product performance characterizations
      iii) Product qualification tests
      iv) 1,000 hour life test or equivalent
   2) Report approval

e) Standard Microcircuit Drawing (SMD)
   1) Draft development
   2) User coordination
   3) SMD release

f) QML listing of approved parts.

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H.3.1.10 Manufacturer's Responsibility. It is the manufacturer's responsibility to ensure all of the defined systems and controls are fully implemented and operational as defined in this specification, appendices, and applicable standards and specifications. The manufacturer shall provide a focal point representative for the coordination and communication of QML program.

H.3.1.11 Qualifying Activity (QA) Responsibility. The QA is responsible for the coordination between the government agencies in the performance of quality audits and report approvals. The QA shall consolidate concerns and observations from the various agencies to provide a jointly agreed to position to provide to the manufacturer in addressing audit deficiencies and in meeting the specified requirements.

Any request for data, additional testing, or new manufacturing requirements, for a QML manufacturer, that were not part of the QA approved certification, qualification test plan, or DLA Land and Maritime audit results, must be provided to and approved by the QA. Supporting data for the request shall also be provided to the QA. Upon approval by the QA, the QA shall submit the request or requirement to the QML manufacturer. The QA shall arrange any necessary conference calls or site visits with the QML manufacturer.

H.3.2 Certification.

H.3.2.1 Design, Wafer Fabrication, Assembly, and Test Certification. The QA shall perform certification validation of the Design, Wafer Fabrication, Assembly, and Test capabilities of the manufacturer. The QA validation shall include analysis of data, and demonstration of the manufacturer's capability, to meet the requirements for certification in the following areas:

H.3.2.1.1 Design. The manufacturer should address the design methodology for the following areas of design.

NOTE: These are also applicable to third party design centers.

H.3.2.1.1.1 Circuit design. QML microcircuits should address the circuit design requirements and performance characteristics herein:

a. Model verification. Provide evidence that all models utilized in the design process are functional, predictable, and accurate over the worst case temperature and electrical extremes. Examples of these models are: electrical (transistor, passives, interconnect, package), behavioral, logic, fault, timing, signal integrity, power estimation and thermal conductivity.

b. Layout verification. Demonstrate the capability of the automated or manual procedures routinely used for design, electrical, and reliability rule checking to catch all known errors, singularly and in combination. These rules cover, as a minimum:
   (1) Design rules check (DRC): Geometric and physical.
   (2) Electrical rules check (ERC): Shorts and open, connectivity.
   (3) Reliability rules: Electromigration and current density, IR drops, latch-up, single event upset (SEU), hot carrier injection (HCI), electrostatic discharge (ESD), burnout backgating (for gallium arsenide (GaAs) technology).

c. Performance verification. The manufacturer should design and construct a chip or set of chips to assess the process capability to perform routing and to accurately predict post-routing performance. The manufacturer should demonstrate that the actual measured performance for each function over temperature and voltage falls between the two worst case performance limits or is covered by statistical models. All critical minimum geometric and electrical design rules should be stressed via devices or structures located on the SEC, TCV, or PMs. The electrical stress requirements for the transistors, passive devices and interconnects on these structures should be determined by worst case circuit conditions. Failure analysis (FA) should be conducted to identify the failure mechanisms occurring in any failed devices and/or structures. Corrections to the design or to the verification/screening method shall be undertaken to mitigate any future occurrences of failures. These changes shall be presented to the QA prior to implementation if part of a new technology test plan. It is allowed that the manufacturer may choose actual product for their TCV or SEC. The manufacturer shall demonstrate burn-in circuits and life test conditions through characterization efforts to ensure proper operation at the device specified frequency.

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d. Testability and fault coverage verification. The manufacturer should demonstrate a design style and a design-for-test (DFT) methodology that, in conjunction with demonstrated CAD for test tools, can provide 99 percent or greater fault coverage on a design of reasonable complexity. The manufacturer should also address their approach for a testability bus to groups such as the Joint Test Action Group (JTAG). The manufacturer should demonstrate the fault coverage measurement (fault simulation, test algorithm analysis, etc.) capability that is used to provide fault coverage statistics of the design using the demonstrated design style, DFT method and CAD for test tools. Measurement of fault coverage should be in accordance with the procedures defined in TM 5012 of MIL-STD-883. For non-digital microcircuits, the fault coverage requirement may not be applicable, but should be supplemented as measures of analog fault coverage become better defined. For microcircuits with both analog and digital functions, this requirement fully applies to the digital portions of the microcircuits.

H.3.2.1.1.2 Design checklist (Class level S) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

a. Design environment/infrastructure.

(1) Project schedule.

(2) Resource management (e.g., designers, hardware, software development).

(3) Historical factors (e.g., any pertinent information based on previous designs, design rules, lessons learned, etc.).

(4) Tools and design flow.

(5) ASIC cell library and design kit.

(6) Intellectual property (IP, e.g., any pertinent information such as use of 3rd party licensed IP, IP developed by another entity or manufacturer, etc.).

(7) Models (for those developing their own cell libraries, and ASIC design kits), for analog/signal integrity simulations, and power calculations.

b. Detailed design hardware description language (HDL) coding (first phase of design).

(1) Specification development guidelines (e.g., what design information must be included in the specification).

(2) HDL coding guidelines.

(3) Design for test (DFT) insertion and fault testing.

(4) Built-in self test (BIST).

c. Validation/verification of modules and top level design.

(1) Fault coverage percentage.

(2) Emulation/prototyping.

(3) Radiation effects mitigation.

d. Synthesis, static timing.

(1) Foundry synthesis guidelines – Handoff to design team

(2) Formulation of constraints from specification/requirements.

(3) Synthesis and statically timed net list – Correlated with original HDL.

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e. Physical design.

(1) Foundry physical design guidelines – Handoff to design team

(2) Placement based on partitioning, architecture, I/O location.

(3) Static timing analysis, with iterated placement, cell sizing and routing to achieve timing closure.

f. Release to foundry.

(1) Foundry run rule checks

(2) Critical design/final design review, utilizing foundry checklists.

H.3.2.1.1.3 Package Design. Packages used for QML microcircuits should address the design requirements and performance characteristics herein. Characterization may be performed by the microcircuit manufacturer, by an external lab, or by the package supplier. In any case, the manufacturer's assembly of QML microcircuits should address all the testing requirements herein. The manufacturer shall address package design/construction quality and reliability. The manufacturer is responsible to maintain documented validation of all characterization methods used, including all supporting data.

a. Thermal characterization. The thermal resistance should be determined for all packages used in the manufacture of QML parts. This value may be obtained by direct or indirect measurements, or by simulation tools or calculations. TM 1012 of MIL-STD-883 may be used for this calculation. If the thermal resistance is obtained by a calculation or simulation tool, this procedure should be certified. To certify such a method of theoretical estimation, the manufacturer shall demonstrate a correlation between the theoretically estimated value and the actual measured value for at least one package of the same style with equal or greater pin count.

b. Electrical characterization. The following electrical characterization parameters should be addressed:

(1) Ground and power supply impedance. Packages used in the manufacture of QML microcircuits should be minimal contributors to ground and power supply noise. The above requirement can be met either through the use of documented package design rules or through testing of the packages, either individually or by similarity, in accordance with TM 3019 of MIL-STD-883.

(2) Cross-coupling effects. Cross-coupling of wideband digital signals and noise between pins in packages used for digital QML microcircuits should be minimized. The above requirement can be met either through the use of documented package design rules or through testing the packages, either individually or by similarity, in accordance with TM 3017 and TM 3018 of MIL-STD-883.

(3) High voltage effects. The voltage applied to a QML package should not produce a surface or bulk leakage between adjacent package conductors (including leads or terminals). The above requirement can be met either through the use of documented high voltage package design rules aimed at minimizing bulk or surface leakage, or through testing of the high voltage packages, either individually or by similarity, in accordance with TM 1003 of MIL-STD-883.

c. Mechanical characterization. The manufacturer shall perform package mechanical characterization tests which includes evaluation for shock and vibration to demonstrate the capability to withstand impacts due to moisture ingression, contamination, corrosion, etc.

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H.3.2.1.2 Wafer fabrication. This includes the manufacturer's in-house fabrication or the subcontractor's fabrication. The wafer fabrication quality systems and controls include statistical process control (SPC) and in-process monitoring programs including the technology characterization vehicle (TCV) program or the Standard Evaluation Circuit (SEC) and parametric monitors (PMs) or alternate assessment procedure with the approval of qualifying activity (QA).

As part of certification, the manufacturer should identify a specific technology or technologies for the wafer fabrication. A technology consists of the fabrication sequence, design rules and electrical characteristics. Demonstration of wafer fabrication capability consists of the fabrication sequence, design rules, electrical characteristics, and process information. All supporting documentation and data shall be made available to the qualifying activity before or during the management and technology validation (see G.3.2.2.1).

A plan shall also be presented that provides for an on-going reliability monitor and failure rate calculations.

H.3.2.1.2.1 Wafer fabrication checklist (Class level S) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

a. Process development
   (1) Design of experiments (This information may not be readily available for older technologies especially when a process is transferred from another facility).
   (2) Process sensitivity (This will define what parameters within the process would identify if the process is stable or marginal. Process variation is different and shows the process can yield even when the parameters are at minimum or maximum).
   (3) Modeling and simulation.
   (4) Producibility and yield analysis.

b. Process characterization.
   (1) Voltage.
   (2) Temperature (Minimum range of -55°C to +125°C, otherwise provide justification).
   (3) Process variability.
   (4) Best and worst case or statistical simulation models considering independent variation of device types (e.g. NFET and PFET).
   (5) Frequency (Defined by the electrical requirements of the device specification).
   (6) Radiation (see appendix C), if applicable.
   (7) Performance margins (until failure).
   (8) Process optimization.
   (9) Process maturity assessment.

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c. Process qualification.
   (1) Test vehicle.
   (2) Single or 1 lot.
   (3) Environmental conditions (for fabrication, test, assembly, and storage).
   (4) Accept/reject criteria.
   (5) Perceptivity of tests (TCV and test programs shall be capable of highlighting the critical parameters and discerning the results that identify accept/reject criteria).
   (6) Process baselined for qualification (no further changes required after characterization).
   (7) Qualification by test, similarity, or space heritage (Process or device that has been produced and passed space level testing and has flown in a space environment similar to the environment expected for this process/device).

d. Fabrication.
   (1) TRB program (or equivalent) (see G.3.2.2).
   (2) SPC and in-process monitoring program (see H.3.2.1.3).

e. Radiation hardness assurance (RHA) (see appendix C), if applicable.

H.3.2.1.3 SPC and in-process monitoring program. An in-process monitoring system should be used by the manufacturer to control key processing steps to insure device yield, reliability, and RHA if applicable. The monitoring system can utilize various test structures, methods, and measurement techniques. The critical operations to be monitored should be determined by the manufacturer based on their experience and knowledge of their processes. The resulting data should be analyzed by appropriate SPC methods (in accordance with the requirements of SAE EIA557 to determine control effectiveness. The following should be addressed for the wafer fabrication process, as a minimum, by the manufacturer:

a. Incoming mask and fabrication process materials.
b. Equipment used for wafer fabrication.
c. Doping material concentration.
d. Cross section diffusion or concentration profile, and epitaxial (EPI) layer.
e. Passivation or glassivation.
f. Metallization deposition.
g. Resultant line width.
h. Passivation process temperature and time.
i. Diffusion, implant anneal process temperature, and time, or both.
j. Sintering or annealing temperature and time.
k. All reliability test data including the standard evaluation circuit (SEC).
l. Mask inspection and defect density data.
m. Parametric monitor test data.
n. Photoresistive processing (including rework procedures).

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o. Ion implant.
p. Wafer backside preparation.
q. Wafer probe acceptance criteria.
r. Rework policy.
s. Oxide process.
t. Gate formation.
u. Air bridge process.
v. Via hole process.
w. Clean room procedures.
x. Change control system/notification.
y. Lot travelers (ref. A.3.4.6, A.3.4.6.1)
z. Equipment calibration and preventive maintenance.
aa. Wafer traceability.
ab. Wafer acceptance plan.
ac. Wafer bump characteristics (height, width etc.,)

H.3.2.1.3.1 SPC and in-process monitor checklist (Class level S) . The following items shall be used as minimum requirements, as applicable for the technology, for the manufacturer and QA in evaluating the new technology for class level S product:

a. Define SPC monitor points.
b. Define control limits and absolute limits.
c. Review of data by the manufacturer and QA.
d. Out of control (OOC) action plans.
e. Radiation performance, if applicable.
f. Process capability (C_{PK}) trigger level.
g. Sample data for any prime lot reviewed by the manufacturer and QA (Prime lot is defined as a lot meeting all process monitor requirements with no MRB or out of control actions implemented).
h. SPC controls in place audited by the QA.

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H.3.2.1.3.2 Parametric monitor (PM) . The manufacturer should have PMs to be used for measuring electrical characteristics of each wafer type in a specified technology. The PM test structures can be incorporated into the grid (kerf), within a device chip, as a dedicated drop-in die or any combination thereof. Location of the PM test structures should be optimally positioned to allow for the determination of the uniformity across the wafer. A suggested location scheme is one near the wafer center and one in each of the four quadrants of the wafer, at least two-thirds of a radius away from the wafer center. The manufacturer should establish, and document, reject limits and procedures for parametric measurements including which parameters shall be monitored routinely and which shall be included in the SPC program. Documentation of the PM should also include PM test structure design, test procedure (including electrical measurement at temperature and the relationship between the measured limits and those determined in the manufacturer's circuit simulations), design rules and process rules. Alternate measurement techniques, such as in-line monitors, are acceptable if properly documented. The following parameters are to be used as a guideline by the manufacturer's TRB in formulating the PM.

a. General electrical parameters.

(1) Sheet resistance: Structures should be included to measure the sheet resistance of all conducting layers.

(2) Junction breakdown: Structures should be included to measure junction breakdown voltages for all diffusions.

(3) Contact resistance: Structures should be included to measure contact resistance of all inter-level contacts.

(3) Ionic contamination and minority carrier life time: Structures should be included to measure ionic contamination, such as sodium, in the gate, field, and inter-metal dielectrics and minority carrier lifetime.

b. MOS parameters.

(1) Gate oxide thickness: Structures should be included to measure gate oxide thickness for both “N” and “P” gate oxides as applicable.

(2) MOS transistor parameters: A minimum set of test transistors should be included for the measurement of transistor parameters. The minimum transistor set should include a large geometry transistor of sufficient size that short channel and narrow width effects are negligible, and transistors that can separately demonstrate the maximum short channel effects and narrow width effects allowed by the geometric design rules. Both "N" and "P" transistors should be included for a complementary metal oxide semiconductor (CMOS) technology. If there is more than one nominal threshold voltage for either the "N" or "P" transistor type the minimum set should be included for each threshold. The transistor parameters to be measured are given below:

(a) Threshold voltage: The linear threshold voltage (VT) for each transistor in the minimum set of transistors should be measured.

(b) Linear transconductance: The linear transconductance (g_m) for the full minimum set of transistors should be measured.

(c) Effective channel length: The effective channel length for the minimum channel length of each transistor type should be measured.

(d) I_{on}: I_{on} for representative transistors in the set.

(e) I_{off}: I_{off} for representative transistors in the set.

(f) Propagation delay: A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.

(g) Field leakage: Field transistor leakage for the minimum spaced adjacent transistors at the maximum allowed voltage should be measured.

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c. Bipolar parameters. Care should be taken in the manner and sequence in which all breakdown voltage and current measurements are taken so as to not permanently alter the device for other measurements.

(1) Sheet resistance: Structures should be included which can be used to measure sheet resistance of all doped regions (e.g., emitter, buried collector.)

(2) Schottky diode parameters: The following measurements should be made on Schottky diodes representative of the size used in the technology:

(a) Reverse leakage: The reverse leakage current (I_R) should be measured at a specified reverse voltage.

(b) Reverse breakdown: The reverse breakdown voltage (BV) should be measured at a specified current.

(c) Forward voltage: The forward turn-on voltage (V_f) should be measured at a specified current.

(3) Bipolar transistor parameters: The following measurements should be made on bipolar transistors representative of the size and type used in the technology. The types should include NPN, Schottky clamped NPN, vertical PNP, substrate PNP, and lateral PNP transistors as applicable.

(a) Transistor gain: The common emitter dc current gain (H_{fe}) should be measured on representative transistors over three decades of collector current, the highest point of which is at the maximum rated current of the device.

(b) Leakage currents: The leakage currents (I_{CEO}, I_{CBO}, and I_{EBO}) should be measured on representative transistors at a specified voltage.

(c) Breakdown voltages: The breakdown voltages (BV_{EBO}, BV_{CBO}, and BV_{CEO}) should be measured on representative transistors at specified currents.

(d) Forward voltages: The forward voltages (V_{BEO} and V_{BCO}) should be measured on representative transistors at the rated currents.

(e) Propagation delay: A test structure should be available in the form of a functional circuit from which propagation delay information can be measured at room temperature.

(4) Isolation leakage: The isolation leakage current (I_L) between minimum spaced adjacent transistor collectors should be measured at a specified voltage.

d. GaAs parameters.

(1) Sheet resistance: Structures should be included which can be used to measure sheet resistance of each of the conducting layers.

(2) Metal-insulator-metal (MIM) capacitor: Capacitor test structures should be included so that dc and rf capacitance, leakage, and breakdown can be measured.

(3) FATFET: A long gate length FET suitable for measurement of Schottky barrier height and ideality factor, carrier concentration and mobility, and channel depth should be included.

(4) Isolation: A structure for use in measuring substrate isolation breakdown should be included.

(5) Ohmic contacts: An ohmic contact transmission line structure should be included so that specific contact resistance and transfer length can be measured.

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(6) GaAs FET parameters: FET test structures should be included, suitable for RF probing, which can be used for measurement of both DC and RF FET parameters. The following parameters should be measured:

(a) I_{dss} - saturated drain current at zero gate bias.

(b) g_m - transconductance at saturation and at 50 percent I_{dss}.

(c) Pinch off voltage.

(d) Gate-drain leakage and breakdown voltage.

(e) Gate-source breakdown voltage.

(f) Source and drain resistance.

(g) S-parameters of FET over frequency range of technology.

e. Fast-test reliability structures. Fast-test reliability structures are structures meant to evaluate, within a few seconds of testing, a particular known reliability failure mechanism to insure that the processing which an individual wafer received is consistent with the reliability goals of the technology. The fast-test structures are in general new and, with the exception of hot carrier aging structures, are not sufficiently mature. Development work on them is intense however, and it is intended that these structures when mature, shall become a mandatory part of the PM. For this reason it has been decided to include information regarding fast-test reliability structures in the following paragraphs. Documentation should be available which shows the correlation between fast-tests and the results of the more traditional accelerated aging tests performed on the TCV.

(1) Hot carrier aging: A fast-test structure should be included to evaluate the susceptibility of MOS transistors to hot electron aging. This structure may be one of the PM test transistors.

(2) Electromigration: Worst-case design rule fast-test structures should be included to evaluate the susceptibility of each metal level and the associated contacts to electromigration.

(3) Time dependent dielectric breakdown (TDDB): Fast-test structures should be included that can evaluate the long-term reliability of gate oxides.

(4) Contact resistance: Fast-test structures should be included that can evaluate the long-term reliability of contacts.

(5) Gate diffusion: Fast-test structures should be included that can evaluate the long-term reliability of the gate contact.

(6) Threshold voltage instability, including Negative Bias Temperature Instability (NBTI) for 130 nm and smaller CMOS technologies.

H.3.2.1.4 Wafer acceptance plan. The TRB should develop and demonstrate a wafer acceptance plan based on electrical and radiation (if applicable) measurement of PMs. This plan should utilize the PM and should include visual criteria, if applicable.

For wafer lot acceptance tests shall be performed in accordance with TM 5007 of MIL-STD-883 or an alternative which meets the minimum requirements of TM 5007 on each wafer lot producing class V, class Y, or class P (class level S) devices. The use of TM 5013 of MIL-STD-883 is encouraged for GaAs technology devices. In addition, this plan should address the concerns detailed in TM 2018 of MIL-STD-883 (e.g., metallization, step coverage). The use of TM 2018 is encouraged, however alternate procedures utilizing PMs and in-line monitors are accepted if approved during validation. PM data should be recorded and made available for review.

This plan can be either a wafer by wafer acceptance plan or a wafer lot acceptance plan, but shall address the following concerns:

a. Small lots.

b. Large lots.

c. Specialty lots.

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H.3.2.1.5 Assembly and packaging. The manufacturer shall demonstrate the quality system and controls, including SPC and in-process monitoring programs for both in-house assembly line and any/all of their subcontractors performing assembly processing for SMD products.

H.3.2.1.5.1 Assembly and packaging technology certification. As part of the certification, the manufacturer should identify the specific assembly technologies that are expected to be listed as part of the technology flow for QML and used in QML microcircuits. Those processes shall be qualified by addressing, as a minimum, the test in tables H-IA or H-IB as appropriate. An assembly technology consists of the materials and processes used for wafer saw, die attach, wire bond, flip chip attachment, package sealing, lead attach, solder dipping, marking, and any other process involved with the construction of the product. All supporting documentation and data shall be made available to the qualifying activity before or during the management and technology validation (see G.3.2.2.1). The following items shall be used as minimum requirements by the manufacturer and the QA in evaluating assembly and packaging for class level S product:

a. Assembly processes.
   (1) Die attach.
   (2) Wire bond/bump.
   (3) Encapsulation.
   (4) Process monitors/SPC.
   (5) Inspections.
   (6) Tests – Mechanical, thermal, optical.
   (7) Lead or column attach.
   (8) Incoming tests or review of accompanying C of C on materials (e. package, die attach material, etc.).

b. Package processes and technology.
   (1) Design.
   (2) Materials selection.
   (3) Assembly under supplier control.
      (a) By supplier.
      (b) Subcontracted.
   (4) Thermal characterization.
      (a) Hot spots.
      (b) Thermal impedance.
   (5) Electrical characterization.
      (a) At specification levels including voltage, full temperature range, and other excitation conditions.
      (b) Beyond specification conditions to determine margin.
      (c) Plan to address unspecified or untested parameters (Review analysis to ensure critical untested parameters are specified or addressed)
   (6) Package qualification data.
      (a) Incoming package tests on bare package.
      (b) Incoming tests on raw materials (e. die attach, etc.)
      (c) Mechanical tests.
      (d) Thermal tests.
      (e) Electrical tests.
      (f) Thermal impedance.
   (7) Column attachment.
      (a) ESD controls.
      (b) at 25°C electrical validation pre and post column attach.
      (c) Mechanical integrity.
      (d) Co-planarity.

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H.3.2.1.6 SPC and in-process monitoring program. A process monitoring system should be used by a manufacturer to control key processing steps to insure product yield and reliability. The monitoring system can utilize various test chips, methods and measurement techniques. The critical operations to be monitored shall be determined by the manufacturer based on their experience and knowledge of their processes. The resulting data should be analyzed by appropriate SPC methods to determine control effectiveness. The following should be addressed, as a minimum, by the manufacturer:

a. Incoming assembly process materials.
b. Incoming package acceptance.
c. Equipment used for assembly.
d. Wafer acceptance criteria.
e. Die attach.
f. Chip to package interconnect (wire/ribbon bond, tab, flip chip).
g. Package seal.
h. Marking.
i. Rework.
j. Lead trim, form, and final finish.
k. Atmosphere and cleanliness control.
l. Chip encapsulation/molding.
m. Encapsulant purity.
n. Internal gas analysis (IGA).
o. Flip chip die pull off test shall be performed (before underfill dispense) in accordance with TM 2031 and bump shear test shall be performed for wafer bump technology qualification.
p. Balls/Columns attach.

H.3.2.1.7 Test capability. The manufacturer shall document test capability to their QM plan, which includes devices screening, qualification and technology conformance test conditions in accordance with the applicable Standard Microcircuits Drawing (SMD), MIL-PRF-38535, and MIL-STD-883, as applicable to the product.

H.3.2.1.8 Certification approval. Upon successful demonstration by the manufacturer of meeting the certification requirements, the QA will issue a certification of approval. This certification will include QA approved alternatives and test optimizations as presented by the manufacturer and listed in the QM plan. Documentation and data presented by the manufacturer during the certification process does not need to be provided as a part of the reliability assessment and qualification stages.

H.3.2.2 Physics-of- failure/TCV reliability assessment.

H.3.2.2.1 Reliability assessment plan. For class level S product, the manufacturer shall provide to the QA a reliability assessment plan for the technology. The plan shall account for all significant failure mechanisms as listed in the following sections.

H.3.2.2.2 TCV program . A TCV program should be implemented by the manufacturer for the technology or process being considered for certification. The program should contain, as a minimum, those test structures needed to characterize a technology's susceptibility to intrinsic reliability failure mechanisms such as electromigration, time dependent dielectric breakdown (TDDB), gate sinking, ohmic contact degradation, sidegating/backgating, hot carrier aging and threshold voltage instability, including Negative Bias Temperature Instability (NBTI). If other wear-out mechanisms are discovered as integrated circuit technology continues to mature, test structures for the new wear out mechanisms should be added to the TCV program. The TCV program shall be used for the following purposes: Certification of the technology; reliability monitoring; radiation hardness assurance and monitoring, when applicable; change control; and the characterization of fast-test intrinsic reliability structures.

NOTE: The test structures necessary to monitor intrinsic reliability failure mechanisms do not have to be a single die or

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location, but can appear on the PM, the SEC, or the device itself. The TCV program (see G.3.3.f) should, however, indicate where the structures are located and how they are tested and analyzed.

H.3.2.2.2.1 TCV certification. For initial reliability assessment, sufficient TCV test structures for each wear-out mechanism should be subjected to accelerated aging experiments. The TCV test structures should be randomly chosen from and evenly distributed from three homogeneous wafer lots in the technology to be certified in the fabrication facility to be certified. These wafers shall have passed the wafer or wafer lot acceptance requirements. The accelerated aging experiments should produce an estimate of the mean time to failure (MTTF) and a distribution of the failure times under worst case operating conditions and circuit layout consistent with the design rules for each wear-out mechanism. From the MTTF and distribution of failures a worst case operating lifetime or a worst case failure rate can be predicted. Test structures should be from completed wafers which have been passivated/ glassivated. A summary of the accelerated aging data and analysis should be available for review by the qualifying activity. The initial certification MTTF, failure distribution and acceleration factors should be used as benchmarks for the technology to which subsequent TCV results shall be compared. This includes evaluation of activation energy, acceleration factors based on voltage and temperature for the technology, long term reliability and known failure mechanism (FMEA) and mitigation strategies. The current density and temperature acceleration factors for electromigration should be determined and a MTTF and failure distribution determined for the worst case current, temperature, and layout geometry allowed in the technology. From the MTTF and failure distribution, a failure rate for electromigration in the technology should be calculated.

All of the TCV test structures shall use the same packaging materials and assembly procedures as standard circuits in the technology. The TCV structures need not use a fully qualified package since qualified packages shall tend to have lead counts far in excess of those needed for intrinsic reliability studies. The packaging requirement for the TCV may be waived by the qualifying activity if the manufacturer can supply documentation showing the equivalence of wafer level and packaged accelerated aging results.

NOTE: In those cases where this may not be possible, the TCV should use a suitable package to allow for the evaluation of the chip technology to be qualified, without adversely affecting the outcome of the test.

An example of the requirements of packages for TCV test structure concerns the hydrogen content of a ceramic package and its effect on hot carrier aging, and can differ substantially for packaged and non-packaged devices. The minimum requirements to be addressed for the TCV structures for specific mechanisms are given below.

a. Hot carrier aging. The TCV should use structures that monitor hot carrier aging applicable to the technology to be used in QML microcircuits. Device degradation is to be characterized in terms of both linear transconductance (g_m) and threshold voltage (V_{TH}) and the resistance to hot carrier aging is to be based on whichever parameter experiences the manufacturers' specified degradation limit for the minimum channel length and width allowed in the technology. A wafer level fast-test screen should be established for technologies that are susceptible to hot carrier aging. This test should be part of the wafer acceptance criteria.

   (1) Metal oxide semiconductor (MOS). The TCV should have structures to characterize the effects of hot carrier aging as a function of channel length for MOS transistors for each of the nominal threshold voltages used in the technology. Degradation should be characterized in terms of g_m and V_{TH}.

   (2) Bipolar. The TCV should contain structures for characterizing hot carrier aging of diodes in bipolar technologies.

b. Electromigration. The TCV should contain structures for the worst case characterization of metal electromigration over:

   (1) Flat surfaces.

   (2) Worst case noncontact topography.

   (3) Through contacts between conductive layers.

   (4) Contacts to the substrate.

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c. Time dependent dielectric breakdown (TDDB) (MOS). The TCV should contain structures for characterizing TDDB of gate oxides. The structures should have gate oxide area and perimeter dominated structures. Separate perimeter structures should be used for the gate ending on a source or drain boundary and where the gate terminates over the transistor-to-transistor isolation oxide. The electric field and temperature acceleration factors for TDDB should be determined and a MTTF and failure distribution determined for the worst case voltage conditions and thinnest gate oxide allowed in the technology. From the MTTF, a failure rate for TDDB in the technology should be calculated.

d. TCV fast test structure requirements. The structures to be used for the fast test reliability monitoring of hot electron aging should be included in the TCV program so that correlations of the fast-test measurements with the accelerated aging results may be made.

NOTE: It is strongly recommended that fast test intrinsic reliability structures for electromigration and TDDB be included in the TCV program so that correlations can be made with longer term aging experiments. It is likely that these structures shall be required for wafer acceptance in the future.

e. Ohmic contact degradation. The TCV should have a structure for assessing the degradation of ohmic contacts with time at temperature, especially for gallium arsenide (GaAs).

f. Sidegating/backgating. A structure should be included for evaluating sidegating/backgating of field effect transistor's (FET's) in GaAs technology.

g. Sinking gate. A FET structure should be included for evaluating the sinking gate degradation mechanism and other channel degradation mechanisms of GaAs FET's.

h. Threshold voltage instability, including Negative Bias Temperature Instability (NBTI) for 130 nm and smaller CMOS technologies. The NBTI test structure evaluates the effect due to interface traps (oxide energy states) in the gate oxide that form under DC inversion stress. Holes in the PMOS devices are known to interact with these traps more easily than electrons, and so this is a PMOS dominated mechanism. These trapped holes cause the threshold voltage (V_{TH}) of the affected transistor to shift lower (more negative) with increasing temperature, degrading device performance.

H.3.2.2.3 Assembly and packaging. The manufacturer should list the assembly and packaging processes (die-attachment, wire/ribbon bonding, seal molding and part marking) that is expected to be listed on the QML and used in QML microcircuit assembly (see H.3.2.1.5).

H.3.2.2.3.1 Assembly process technology. New assembly process technologies shall be characterized to determine the mechanical and thermal performance. The technology's susceptibility to intrinsic reliability failure mechanisms shall be characterized to determine potential failure modes. The characterizations may include performance of thermal stresses at multiple temperature levels to develop derating curves. Tables H-IA and H-IB identify the assembly process qualification testing which shall be addressed for the technology being used.

H.3.2.2.3.2 Packaging technology. The manufacturer shall address package design/construction quality and reliability. The manufacturer is responsible to maintain documented validation of all characterization methods used, including all supporting data (see H.3.2.1.1.3). Tables H-IIA and H-IIB identify the key package characteristics for which testing shall be addressed on each QML package technology.

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H.3.2.2.3.2.1 Epoxy and molding compound materials. Plastic encapsulated microcircuit (PEM) device manufacturers shall document characteristics of epoxy and molding compound materials to their QM plan for QA review and approval. Robust molding compound materials are required to meet higher operating temperature, quality, and reliability issues. For selection of epoxy and molding compound materials the following properties shall be tested in accordance with TM 5011 of MIL-STD-883 during initial qualification of PEM devices:

a. Glass transition temperature (Tg)
b. Coefficient of thermal expansion (CTE) ppm/C above or below glass transition temperature Tg.

H.3.2.2.3.2.2 Glass transition temperature. Glass transition temperature is a first order effect on package robustness specifically modulus and coefficient of thermal expansion (CTE). Knowing the glass transition temperature (Tg) of the molding compound or epoxy of plastic encapsulated microcircuit (PEM) is required for defining package operating temperature. The glass transition temperature (Tg) test method selection should be based on molding compound and may be used by the vendor/suppliers option but test method needs to remain the same for subsequent test i.e. ASTM E-1356: Differential Scanning Calorimetry is a quicker test method. Manufacturers shall document the suppliers performed test data i.e. Certificate of Compliance (CofC) includes glass transition temperature (Tg), CTE, mold compound type and shelf life for QA review and approval and shall be included in the manufacturers QM plan.

H.3.2.2.4 Reliability assessment report. For class V, class Y, or class P (class level S) product, a reliability assessment report shall be submitted to the QA for review and approval which demonstrates the successful completion and results of the assessment.

H.3.3 Transitional certification.

H.3.3.1 Transitional certification and qualification. Manufacturers may be granted transitional certification based on the following requirements:

a. The manufacturer has qualifying activity (QA) approval that all facilities covered by the transitional certification supply product built to the previously certified and qualified MIL-M-38510 product flows. Facilities not meeting this condition are eligible for transitional certification, but they may require an audit if deemed necessary by the QA.

   If the manufacturer has never received MIL-M-38510 certification and qualification, but has been approved by DLA Land and Maritime for class M products only, an audit of the facilities under QML consideration shall be required. If these facilities have been audited by DLA Land and Maritime under the class M (SMD) random audit program, the audit may not be necessary, as determined by the QA.

   Facilities that have never been audited by DLA Land and Maritime are eligible for transitional certification and an audit will be required unless the QA determines that an audit is not necessary.

b. The manufacturer should submit a plan for achieving full QML. The plan should include a self-assessment, quality improvement plan, SPC plan, and a plan to upgrade any DLA Land and Maritime drawing or SMD part to one part-one part number Q level devices.

c. The manufacturer should comply with all requirements of appendix A of this specification until the QA has approved the manufacturer for full QML certification at which time the previous MIL-M-38510 (appendix A of MIL-PRF-38535) requirements shall be superseded by the requirements of the main body of this specification and all applicable appendices. As the manufacturer moves toward full QML certification, the QA can allow variations to appendix A as part of the transition process. For class level S only, the manufacturer should notify the space community (e.g., NASA, NRO, DTRA, and AFSMC) of any proposed major variations to appendix A requirements. Further review by these organizations may be necessary before these variations can be sanctioned.

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d. Any major changes to the transitional certification lines should be approved by the QA until such time as the QA approves the manufacturers TRB system and QM plan. This includes any deletion of test requests.

e. If any re-qualifications are required they should be in accordance with the guidelines of appendix A or as approved by the QA.

The QML allowances given by this transitional certification shall be approved after the on-site verification and certification by the QA, but prior to shipment of any product under this specification. In addition, the manufacturer shall make a commitment to becoming QML certified for all portions of the process under transitional certification. If this commitment is not met, the QA reserves the right to remove the transitional certification and all benefits associated with that certification.

NOTE: The transitional certification is not permanent (approximately 2 years maximum, unless extended by the QA) but allows the manufacturer some flexibility while still working toward QML on the remainder of the processes committed to QML. No class level S product shall be shipped until a full QA on-site certification is achieved.

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H.3.4 Qualification.

H.3.4.1 Technology qualification. The process for qualification is outlined below and is further described in detail in the subsequent sections.

a. Plan approval.
   (1) Screening flow.
   (2) Process performance characterization plans and data.
   (3) Process qualification test plans and data.
   (4) For class level B products, life test on a minimum of 1 wafer lot for 1000 hrs minimum at 125°C ambient, or equivalent.
   (5) For class level S products, long term life test shall meet the requirements of paragraph B.3.4, appendix B, or shall meet long term life test on a minimum of 1 wafer lot for 4,000 hours minimum at 125°C ambient, or equivalent.
b. Report approval.

For initial technology qualification, a sufficient number of SEC devices is required, from wafers passing the wafer screen requirements and randomly chosen and evenly distributed from three wafer lots for life testing and total ionizing dose (TID) requirements (RHA products only). The testing shall be performed in accordance with MIL-PRF-38535 Groups A, B, C, D, and E (if applicable) or to the agreed to alternatives and test optimizations defined in the QM plan. The number of SEC device failures shall serve as a qualification benchmark for the technology. Failure analysis (FA) should be done on failed SEC's to determine each failure category and action taken to correct any problems found. The SEC reliability data, including FA results, should be available for review by the QA. For RHA environments, irradiate SEC to demonstrate radiation hardness assurance capabilities limit (RHACL).

For new class level S product, if the technology is mature at other levels, the manufacturer may provide a supplemental/alternative data submittal to the QA for the reliability demonstration above. The alternative data submittal may include, but is not limited to the following:

a. Historic product shipment summary - total quantity shipped of similar product/family on same process.

b. Field returns summary. (NOTE: Proprietary information such as program names and individual customer names shall not be revealed.)

c. Reliability summary data - from the reliability monitor program & Failure rate calculation.

d. Historic qualification data - from similar product(s) from the same process family.

e. Examples of process monitors and data showing performance & trends from recent lots.

f. Examples of wafer lot acceptance reports.

NOTES: For complex devices initial technology qualification, a sufficient number of SEC or actual devices are required, and selected devices must pass wafer screen test requirements. The SEC or actual devices shall be chosen randomly and evenly distributed from multiple wafers or multiple wafer lots or single wafer lot (with the approval of QA) for life testing, and for RHA devices, total ionizing dose (TID) test and samples size shall meet the requirements of table C-I group E test herein and TM 1019 of MIL-STD-883.

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H.3.4.1.1 Process technology validation. The manufacturer shall perform sufficient technology qualification testing to assure the devices supplied meet the minimum class level B or S performance requirements as described herein. The manufacturer shall maintain documentation of qualification testing for review by the preparing or acquiring activity upon request.

H.3.4.1.2 Technology qualification eligibility. Design, wafer fabrication, assembly, and qualification testing of the demonstration vehicles may begin before certification is granted. However, if deficiencies and concerns found during the validation require changes to the process flows, the design, wafer fabrication, assembly, and testing shall be redone on the new process flows. In all cases, start of the qualification testing should begin no later than 6 months after the letter of certification is received in order to retain the manufacturer's initial certification. Completion should be achieved in a timely manner or recertification may be necessary.

H.3.4.1.3 Demonstration vehicles. Demonstration vehicles shall be produced on the certified manufacturing line as defined in the QM plan submitted during the certification process. These demonstration vehicles should be of such complexity as to be representative of the microcircuits to be supplied by the manufacturer. The demonstration vehicles will be assembled in packages that are representative of manufacturer technology and shall be screened to the appropriate QML classes Q or V or Y flow, including all applicable test alternatives and test optimizations. Each demonstration vehicle shall operate and meet all performance requirements of the device specification and RHACL for a radiation hardened process.

NOTES: For a technology which has a die as its primary product, the demonstration vehicle should be suitably packaged to allow evaluation of the technology without adversely affecting the outcome of the tests.

H.3.4.2 Technology qualification test plan. The manufacturer shall submit a qualification test plan which details the test flow, test limits, test data to be measured, recorded and analyzed, test sampling techniques, and traceability records. The test plan should detail materials, manufacturing construction techniques (including design CAD tools), testing and reporting techniques and should be made available to the qualifying activity at the time of certification. The test plan should include traceability documentation, milestone charts and the proposed demonstration vehicle descriptions. All test limits should be in accordance with the requirements of the SMD. All demonstration vehicles shall be representative of the manufacturing and screening processes. For class level S product new technology items, the plan shall include any screening tests or additional qualification tests required as a result of the characterization and physics-of-failure evaluations.

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H.3.4.3 Wafer fabrication technology validation. A manufacturer should have the standard evaluation circuits (SEC) or technology characterization vehicles (TCV) for the technology or process being considered for certification. A manufacturer's SEC should be used to demonstrate fabrication process reliability for the technology. The SEC design documentation should address: The design methodology, the software tools used in the design, the functions it is to perform, its size in terms of utilized transistor or gate count, and simulations of its performance. Documentation procedures for the SEC and standard production devices should be the same so that correlation can be made. The SEC may be designed solely for its role as a quality and reliability monitoring vehicle or it may be a standard product. (For RHA environment, see appendix C.) The SEC should address the following requirements for initial technology characterization/qualifications:

a. Complexity. The complexity of the SEC for digital microcircuits shall contain, as a minimum, one-half the number of transistors expected to be used in the largest microcircuit to be built on the QML line.

   All microcircuits device types shall include one or more test vehicles or SEC that represent all the cell types, including memory and exercise the functionality of the process technology.

   For classes V, Y or P (class level S) microcircuit devices, the SEC or multiple devices shall represent all the cell types including memory and shall operate during burn-in at a minimum of 75% of the product frequency, and keeping in mind maximum junction temperature and power dissipation constraints, and shall have electrical tests performed to demonstrate expected product operating capability at the maximum rated frequency without parametric or catastrophic failure. Alternative approaches must be approved by the Qualifying Activity.

b. Functionality. The SEC shall contain fully functional circuits capable of being tested and screened in a manner identical to the QML microcircuits.

c. Design. The SEC shall be designed to stress the design capabilities of the process (see H.3.2.1.1.1c). The architecture of the SEC should be designed so that failures can be easily diagnosed.

d. Fabrication. The SEC shall be processed on a wafer fabrication line that is intended to be, or already is, a certified QML line.

e. Packaging. The SEC shall be packaged in a package qualified in accordance with requirements in 3.4.1.4.1 herein.

NOTES: A different SEC may be required whenever the design rules, the materials, the basic processes, or the basic functionality of the technology differ.

H.3.4.4 Assembly/Packaging technology validation. The manufacturer shall demonstrate the capability of the assembly and package processes by qualifying the SEC package or actual product to the package certification and qualification procedures. The manufacturer shall document how packages used in the manufacture of QML products are grouped together as a package family for qualification and change control purposes. The technology qualification demonstration shall be conducted on samples pulled from minimum of 3 different assembly lots for assembly/process technology validation. The qualification testing shall be conducted in accordance with MIL-PRF-38535 Groups A, B, and D or to the agreed to alternatives and test optimizations defined in the QM plan.

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H.3.4.4.1 Package integrity demonstration test plan (PIDTP) . Manufacturability, test, quality and reliability issues unique to specific assembly/package technologies intended for space applications shall be addressed in a Package Integrity Demonstration Test Plan at the start of the package design cycle. The PIDTP shall be approved by QA after consultation with the space community. The technologies requiring such a plan include: a) non-hermetic packages (e.g., class Y), b) flip-chip assembly, c) solder terminations and d) passive components. Microcircuits employing more than one of these technologies shall include elements for each in the PIDTP.

H.3.4.4.1.1 Non-Hermetic packages. For class Y microcircuits, the PIDTP must address issues unique to non-hermetic construction and materials, such as potential materials degradation, moisture absorption, and resistance of active devices, passive devices and interconnects to environmental effects and processing stresses. Moisture sensitivity level characterization (ref: IPC/JEDEC J-STD-020D) shall be performed for exposed flip-chip underfill or thermal grease/epoxy.

H.3.4.4.1.2 Flip-chip assembly. For space microcircuits employing flip-chip assembly technologies either class V or class Y (class level S), the PIDTP must address the materials and processes unique to solder bump interconnect attach, underfill and lid-to-die attach. The plan shall demonstrate as a minimum, how the following are evaluated and monitored including a corresponding package level reliability demonstration:

1) Substrate materials. The substrate materials shall be documented in the PIDTP, and shall include the following properties and characterizations:

i) Substrate core and build-up layer materials

ii) Conductor material and composition

iii) Landing pad construction and composition

iv) Solder mask material and thickness

v) Coefficient of thermal expansion (CTE)

vi) Glass transition temperature (Tg) if appropriate

vii) Moisture absorption and outgassing characterization (MSL level characterization)

viii) Radiation exposure effects on materials (part of product qualification)

2) Bump geometry and quality. The solder bump geometry and wafer level inspections shall be documented in the PIDTP, and shall include the following items:

i) Bump height

ii) Bump diameter

iii) Minimum bump pitch

iv) Under bump metallurgy (UBM) construct

v) UBM shape and size

vi) Bump yield

vii) Bump shear

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3) Solder bump construction process and materials. The solder bump construction process shall be documented in the PIDTP (e.g., plated, evaporation, solder paste, ball drop), along with the bump material composition (e.g., alloy). In addition, the Under Bump Metallization (UBM) deposition process (e.g., plated, evaporation, sputtered) and composition shall be documented in the PIDTP.

4) Flux materials. If flux is used during flip chip assembly, the flux type (e.g., no-clean, water soluble) and materials employed for solder bump interconnect reflow shall be documented in the PIDTP.

5) Underfill materials. Underfill materials shall be documented in the package integrity demonstration test plan (PIDTP) and shall include the following properties and characterizations, as well as those in accordance with MIL-STD-883 Test Method 5011:

i) Coefficient of thermal expansion (CTE)

ii) Glass transition temperature (Tg)

iii) Thermal conductivity

iv) Underfill Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. Underfill outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.

5.1) Underfill Quality: Manufacturer shall perform stress tests to evaluate the underfill material and process for complete fill and strength.

i) Die shear or die pull-off strength performed during PIDTP for one-time evaluation.

ii) Voiding

iii) Incomplete fill

iv) Excess underfill material control

5.2) Underfill long term reliability test: Manufacture's shall perform the following long term underfill reliability test.

i) Temperature cycling test: Cured underfill with solder bump temperature cycling test shall be performed for 1,000 cycles in accordance with TM1010 condition C (-65 to 150°C) or condition B depending on package capability. For cases with glass transition temperature(Tg) below 125°C the upper temperature may be set at underfill glass transition temperature.

a) Post temp cycle Acoustic Microscopy test shall be performed to verify underfill void and delamination. The sample size 10(0) shall be considered as minimum during underfill package initial qualification.

b) Additional destructive evaluation may be required depending on acoustic microscopy results.

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6) Thermal interface materials (TIM) for Lid attach/adhesive materials.

Devices with lid or heat spreader attached to the back side of a microcircuit die, the lid attach/adhesive thermal interface materials shall be documented in the PIDTP and include the following properties and characterizations, as those in accordance with MIL-STD-883 Test Method 5011:

a) Glass transition temperature (Tg)

b) Coefficient of thermal expansion (CTE)

c) Thermal conductivity

d) Outgassing test: For non-hermetic flip chip devices(e.g. class Y) outgassing test shall be performed in accordance with ASTM E595. TIM outgassed limits shall be <1% for total mass loss and <0.1% for CVCM.

7) Flip chip bump shear test. For flip chip, a bump shear test shall be performed on bumped wafers in accordance with JEDEC JESD22-B117 or equivalent (e.g. method 2019, 2031) to determine the shear strength of the individual solder bumps for initial qualification. The test method does not define the pass/fail criteria for small bumps used in flip-chip. Data analysis should be done to evaluate the process variability. The evaluation process shall be documented in the PIDTP. Die shear tests 2011, 2019, or 2031 are not useful as the mechanical strength of the flip-chip assembly will either exceed the tool capability or the die will be destroyed and not provide meaningful information.

8) Lot date code for non-hermetic flip chip device. For non-hermetic flip chip devices lot date code shall be assigned upon completion of underfill cure or at lid attach (method to be defined and documented by the manufacturer) to identify the device assembly processing and assembly location. Devices will be traceable through the lot date code to the assembly year, sealing week and assembly location.

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H.3.4.4.1.2.1 Pb free bump qualification for flip-chip devices : For microcircuit devices containing Pb-free solder bumps with Underfill/Encapsulation, the materials and processes unique to Pb-free solder bump alloy and underfill composition shall be documented in the PIDTP for QA approval. Manufacturer processes and materials shall be qualified by addressing, as a minimum, the test in table H-I for Pb free bump initial qualification and risk mitigation:

TABLE H-I. Assembly process technology testing for flip chip packages containing Pb free bump 1/

Test	Test Method	Condition	Sample Size
Temperature Cycling	MIL-STD-883, TM1010	Cond C, 1000 Cycles 2/	15 pieces
HAST 3/	JESD22-A110 (Biased HAST)	130°C/85% relative humidity for 96 hours Or 110°C/85% relative humidity for 264 hours	16 pieces
Thermal Shock	MIL-STD-883, TM1011	Cond B, 15 cycles	15 pieces
Shock and Vibe	MIL-STD-883, TM2002, 2007, and 2001 similar to MIL-PRF-38535 Group D, Subgroup 4 (without hermeticity)	TM2002: Cond B TM2007: Cond A TM2001: Cond D	15 pieces
Bump Shear Test	JESD22-B117 or JESD22-B109 or equivalent (e.g. method 2019 or 2031)		Minimum of 30 bumps on each of 3 different die
Die Attach Bond Strength	MIL-STD-883, TM2011	Cond F	3 pieces
Die Shear Strength	MIL-STD-883, TM2019		3 pieces
Die Pull Off	MIL-STD-883, TM2031		3 pieces
Destructive Part Analysis(DPA) bump sample post-thermal cycle and thermal shock test	For DPA see SAE ARP 6537 section 4.1.1.		1 piece

1/ SAE ARP 6537 may be used as a guideline.
2/ Parts with organic substrates containing Pb-free solder bumps with underfill use MIL-STD-883, TM 1010 condition B.
3/ Baised HAST test shall apply to non-hermetic packages only. For ceramic hermetically sealed packages baised HAST test shall be replaced with HTOL (Steady State Life Test, MIL-STD-883, TM 1005) test for bump integrity under high temperature (either 110°C/85% RH for 96 hours or 130°C/85% RH for 264 hours).

H.3.4.4.1.3 Solder terminations. For space use microcircuits employing solder terminations (e.g ball grid array or column grid array), the PIDTP shall address the materials and processes unique to solder terminations, such as ball/column integrity, attachment integrity, damage due to test, protection for shipment and shelf life. The manufacturer shall perform post column attachment electrical characterization over temperature and compare data with pre-column attachment process to assess any changes due to the column attachment process.

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TABLE H-IA. Assembly process technology testing for hermetic (classes Q, V) and non-hermetic packages (class Y).

Group number	Process	MIL-STD-883 test method and condition or JEDEC test method 1/	
		Hermetic packages (classes Q, V)	Non-hermetic packages (class Y)
1	Die-attach and interconnect	Where applicable a. Thermal shock TM1011 condition C, 100 cycles b. End-point electricals test - In accordance with device specification c. Radiography (X-ray) TM 2012 or Acoustic Microscopy - TM 2030 d. Bond strength TM 2011 (die-mount and wire bond) plus Die cracks TM 2010 2/ 3/ e. Die shear or stud pull TM 2019 or TM 2027 3/ f. Underfill/epoxy (see H.3.4.4.1.2)	Where applicable a. Thermal shock TM1011 condition C, 100 cycles (Ceramic class Y only) b. End-point electricals test - In accordance with device specification c. Radiography (X-ray) TM 2012 or Acoustic Microscopy - TM 2030 d. Bond strength TM 2011 (die-mount and wire bond) plus For die cracks TM 2010 2/ 3/ e. Die shear or stud pull TM 2019 or TM2027 3/ f. Underfill/epoxy (see H.3.4.4.1.2) and ASTM E595 for outgassing.
2	Die-attach, interconnect and seal test	Where applicable a. Mechanical shock TM 2002, condition B b. Variable frequency vibration TM 2007, condition A c. Constant acceleration TM 2001 4/ d. Fine and gross leak TM 1014 e. Visual inspection TM 1010, (visual criteria 20X of magnification) f. End-point electricals test - In accordance with device specification	Where applicable a. Mechanical shock TM 2002, condition B b. Variable frequency vibration TM 2007, condition A c. Constant acceleration TM 2001 4/ d. Not applicable e. Visual inspection TM 1010, visual criteria 20X of magnification f. End-point electricals test - In accordance with device specification
3	Lid seal	Internal gas analysis (IGA) test TM 1018 (5,000 ppm maximum at +100°C)	Not applicable
4	Lid seal	Where applicable Lid torque (glass seal) TM 2024	Where applicable Lid torque (glass seal) TM 2024
5	Code marking	Where applicable Resistance to solvents TM 2015	Where applicable Resistance to solvents TM 2015
6	Final package testing	High temperature Storage TM 1008 (1,000 hours at +150°C)	High temperature Storage TM 1008 (1,000 hours at +150°C)
7	Post burn-in lead finish	Where applicable Solderability TM 2003 solder temperature (+245°C ± 5°C)	Where applicable Solderability TM 2003 5/ solder temperature (+245°C ± 5°C)

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TABLE H-IA. Assembly process technology testing for hermetic (classes Q, V) and non-hermetic packages (class Y). - Continued.

1/ The test methods are listed herein to give the manufacturer an available method to use. Alternate procedures or test methods may be used.
2/ Flip chip does not have wire bonds. Wire pull testing does not apply.
3/ Flip chip die pull-off or shear testing does not provide useful information. The required force either exceeds the tool capability or results in extreme damage to the die. Bump adhesion quality can be inferred using the electrical test, radiography, and/or acoustic microscopy.
4/ Constant Acceleration (Centrifuge) is not applicable for flip chip. No wires in the package that can move and create shorts.
5/ Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002.

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TABLE H-IB. Assembly process technology testing for plastic packages (classes N, P). 1/

Group number	Process	Test	MIL-STD-883 test method or industry standard
1	Die-attach and interconnect	a. In-line visual inspection b. In-line bond strength 2/ c. In-line ball bond shear 2/ d. In-line die shear/stud pull 3/ e. Post molding X-ray	a. TM 2010 (die-mount and wire bond) b. TM 2011 c. ASTM F1269 d. TM 2019 or TM 2027 e. TM 2012
2	Die-attach, interconnect, and molding	a. Radiography (X-ray) b. Acoustic Microscopy (ultrasonic inspection) etc.	a. TM 2012 (die-mount and wire bond) b. TM 2030
3	Die-attach, interconnect, and molding	a. Temperature cycling (1,000 cycles) b. End-point electricals	a. TM 1010 condition C or JESD22-A104 4/ b. In accordance with device specification
4	Marking	Resistance to solvents	TM 2015
5	Storage conditions	High temperature storage	TM 1008, 1,000 hours at +150°C 4/
6	Post burn-in lead finish	Solderability	TM 2003 solder temperature (+245°C ± 5°C) 5/

1/ The test methods are listed herein to give the manufacturer an available method to use. Alternate procedures or test methods may be used.
2/ Flip chip does not have wire bonds. Wire pull testing does not apply.
3/ Flip chip die pull-off or shear testing does not provide useful information. The required force either exceeds the tool capability or results in extreme damage to the die. Bump adhesion quality can be inferred using the electrical test, radiography, and/or acoustic microscopy.
4/ Package materials with limited high and low temperature range may apply an alternate test condition and shall be specified in the manufacturer's QM plan.
5/ Alternative solderability may be performed in accordance with IPC EIA/IPC/JEDEC J-STD-002.

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TABLE H-IIA. Technology characterization testing for hermetic (classes Q, V) and non-hermetic packages (class Y) .

Group number	Process	MIL-STD-883 test method and condition or JEDEC test method	
		Hermetic packages (classes Q, V)	Non-hermetic packages (class Y)
1	Dimension 1/	Physical dimension TM 2016	Physical dimension TM 2016
2	Resistance to moisture	Where applicable a. Thermal shocks TM 1011, condition C, 15 cycles b. Temperature cycles TM 1010, condition C, 100 cycles c. Moisture resistance TM 1004, unbiased condition d. Visual inspection TM 1010 and TM 1004 visual criteria e. Fine and gross leak TM 1014	Where applicable a. Thermal shocks TM 1011, condition C, 15 cycles b. Temperature cycles TM 1010, condition C, 100 cycles c. HAST(Biased) JESD22-A110 d. Visual inspection TM 1010 and TM 1004 visual criteria e. Not applicable
3	Susceptibility to corrosion	Where applicable Salt atmosphere TM 1009, condition A	Where applicable Salt atmosphere TM 1009, condition A
4	Leads	Where applicable Lead integrity TM 2004, condition A, B2 or D For pin grid array TM 2028 For BGA (ball shear) - JESD22-B117 For CGA (Column pull test) TM 2038	Where applicable Lead integrity TM 2004, condition A, B2 or D For pin grid array TM 2028 For BGA (ball shear) - JESD22-B117 For CGA (Column pull test) TM 2038
5	Susceptibility to electrostatic discharge (ESD) sensitivity 2/	ESD TM 3015 or ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002	ESD TM 3015 or ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002
6	Susceptibility to latch-up	Where applicable Latch-up test JESD78 or Manufacturers internal procedures	Where applicable Latch-up test JESD78 or Manufacturers internal procedures
7	Thermal resistance	Thermal characteristics TM 1012	Thermal characteristics TM 1012
8	Underfill/epoxy materials	(see H.3.4.4.1.2)	(see H.3.4.4.1.2) and For outgassing ASTM E595
9	BGA/CGA packages: Ball/Column attachment	Per approved PIDTP	Per approved PIDTP

1/ Performed as either characterization or as part of qualification.
2/ ESD classification level is as defined within test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) as applicable.

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TABLE H-IIB. Technology characterization testing for plastic packages (classes N, P) .

Group number	Process	Test	MIL-STD-883 test method or industry standard
1	Dimensions	Physical dimension	TM 2016 1/
2	Moisture sensitivity Level	Moisture sensitivity Level	Per manufacturer's specification
3	Resistance to moisture	a. Preconditioning Electrical test b. Biased HAST (500 hours, +130°C , 85% RH) c. End-point electricals test	a. In accordance with device specification. 2/ b. JESD22-A110 3/ c. In accordance with device specification.
4	Susceptibility to corrosion	Salt atmosphere	TM 1009
5	Susceptibility to leakage and corrosion	Autoclave (no bias) (pressure pot) 2 atm., +121°C	JESD22-A102 4/ (data to be provided for 96 hours and 168 hours)
6	Leads	Lead integrity	TM 2004, condition A, B2 or D
7	Susceptibility to moisture induced cracking at reflow soldering for surface mount and applicable through hole packages	a. Moisture intake b. Reflow simulation c. Inspection for Delamination and cracks	a. 168 hours at +85°C/85% RH or bake + minimum guaranteed time at +30°C /60% RH b. Vapor phase (+219°C , no preheat) or Infrared (+240°C maximum) c. Cross-section at 1000X, ultrasonic (Acoustic Microscopy) etc. TM 2030
8	Safety	Flammability	UL 94, ASTM D2863
9	Fungus resistance	ASTM G21	Required only if fungus is a concern
10	Susceptibility to electrostatic discharge (ESD) sensitivity	ESD	ESD TM 3015 or ANSI/ESDA/JEDEC JS-001 and ANSI/ESDA/JEDEC JS-002 5/
11	Susceptibility to latch-up	Latch-up test	JESD78 or manufacturers internal Procedures
12	Thermal resistance	Thermal characteristics	TM 1012

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TABLE H-IIB. Technology characterization testing for plastic packages (classes N, P) . - Continued

1/ Performed as either characterization or as part of qualification.
2/ The manufacturer shall define a "preconditioning" procedure that simulates board assembly of plastic surface mount devices. This procedure should include moisture intake and reflow simulation. Exposure to soldering fluxes (possible source of corrosiveness) and to board cleaning agents is also recommended for preconditioning the devices.
3/ Five hundred hours of highly accelerated stress testing (HAST) is preferred but the qualifying activity shall consider the manufacturers overall processing and testing to evaluate this requirement. The actual HAST hours or alternate testing shall be included in the QM plan.
4/ Alternative to Autoclave, unbiased HAST may be performed in accordance with JESD22-A118.
5/ ESD classification level is as defined within test method 3015 of MIL-STD-883 or ANSI/ESDA/JEDEC JS-001 for Human Body Model (HBM) and ANSI/ESDA/JEDEC JS-002 for Charge Device Model (CDM) as applicable.

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H.3.4.5 Technology qualification report approval . The technology qualification report that demonstrates successful compliance to the qualification test plan, and shall be submitted to the QA for their review and approval.

H.3.4.6 Qualification test report. The manufacturer should present to the qualifying activity (QA) an analysis of the qualification data. The aim of this analysis is to show that all process variables are under control and repeatable within the certified technology and that parametric monitor, TCV, and SEC data monitoring are adequate and correlatable to the process. The QA should be notified of any improvements/changes to the certified QML technology flow as a result of evaluating the qualification testing data. The following data, if applicable, should be addressed and retained by the manufacturer to support the results:

a. Simulation results from the design process (can be reviewed during the validation).

b. Parametric monitor test data.

c. Results of each subgroup test conducted, both initial and any resubmissions.

d. Number of devices tested and rejected.

e. Failure mode and mechanism for each rejected device.

f. Read and record variable data on all specified electrical parameter measurements.

NOTE: Specified electrical tests from a serialized, random sample (minimum of 22 devices) may be used to satisfy this requirement. The manufacturer may submit variables data in histogram format giving mean and standard deviation or equivalent for passing microcircuits.

g. Where delta limits are specified, variable data, identified to the microcircuit serial number, should be provided for initial and final measurements.

h. For physical dimensions, the actual dimension measurements on three randomly selected microcircuits, except where verification of dimensions by calibrated gauges, overlays, or other comparative dimensions verification devices is allowed.

i. For bond strength testing, the forces at the time of failure and the failure category, or the minimum and maximum readings of the microcircuits if no failures occur.

j. For die shear or stud pull strength testing, the forces at the time of the failure and the failure category, or the die shear or stud pull reading if no separation occurs.

k. A copy of the test data on nondestructive bond pull testing as required by TM 2023 of MIL-STD-883.

l. For RHA testing, pre-test and post-test end-point electrical parameters, transient and single event phenomenon (SEP) response and test conditions (if applicable).

m. For lid torque strength testing, the forces at the time of failure or the actual torque, if no separation occurs.

n. For internal gas analysis (IGA) readings, report all gases found.

o. Copy of burn-in circuits.

H.3.4.7 Qualification test failures. If any particular testing results are not successful, the manufacturer should perform failure analysis and take necessary corrective action. The manufacturer should notify the qualifying activity of any decision not to pursue qualification of any material or manufacturing construction technique previously certified. After corrective actions have been implemented, qualification testing should restart.

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H.3.4.8 Product qualification (extension from existing qualified technology) . If the manufacturer wants to qualify additional product types from previously QA approved process technologies, the qualification plan shall reference the process technology information (physics-of-failure, description, etc.) and define the specific characterization, screening, and qualification tests required for the new product including the life test duration, conditions, and rationale.

a. Product Qualification (Extension from existing qualified process technology)

1) Plan approval

i) Screening flow

ii) Product performance characterization plans and data

iii) Product qualification test plans and data

iv) 1,000 hour life test or equivalent

2) Report approval

b. Product qualification for multi-product wafer (MPW):

1) When qualifying product from a multi-product wafer (MPW), the manufacturer's shall determine whether each product design shall receive all qualification testing separately, or whether commonality of designs shall allow extension to the other designs on the MPW. Each microcircuit design to be used as an SEC or product shall receive the full applicable QML approved screening flow.

2) If any MPW microcircuit design is to be considered for qualification by extension then a technical analysis of the designs shall be documented and approved by the TRB to determine which design is worst case and representative of the other microcircuit designs on the same wafer. Microcircuit designs with different levels of circuit spacing (e.g., digital logic vs. memory cell) or different functionality (e.g., analog to digital converter vs. transceiver) must be qualified separately.

3) The following areas shall be evaluated as a minimum to determine if a worst case design is representative of the MPW for the identified qualification test methods of MIL-STD-883.

i) SEM inspection shall be performed in accordance with TM 2018, (class level S only): Worst case representative design only.

ii) Life test shall be performed in accordance with TM 1005; Full qualification sample on worst case representative design only and 5 (five) pieces sample on all other designs also be tested.

iii) Total Ionizing Dose (TID) test shall be performed in accordance with TM 1019; Dose rate Latch-up test shall be performed in accordance with TM 1020, and Dose rate Upset shall be performed in accordance with TM 1021 (If applicable): Full qualification sample on worst case representative design and 5 (five) pieces sample on all other designs.

iv) Electrostatic Discharge (ESD) sensitivity test shall be performed in accordance with TM 3015; Capacitance in accordance with TM 3012; and Electrical Latch-up: Each buffer type shall be tested for initial qualification or buffer design changes.

v) Single Event Effects (SEE) test shall be performed in accordance with JESD57 (If applicable): Manufacturer's shall test each cell type potentially susceptible for initial qualification or cell design changes.

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H.3.5 Standard microcircuit drawings (SMDs) . SMD depicts the Government's requirements for an existing commercial item, tested for a military application, disclosing applicable configuration, envelope dimensions, mounting and mating dimensions, interface dimensional characteristics, specified performance requirements, and inspection and acceptance test requirements as appropriate for a military environment. The general steps of SMD preparation by the preparing activity (PA) are as follows:

a. Draft Development

b. User Coordination

c. SMD Release

H.3.6 Listing of microcircuits on the Qualified Manufacturer's List (QML) . To be listed on the QML for this specification, the manufacturer shall demonstrate compliance to the QML certification requirements (see 3.4.1), demonstrate compliance to the QML qualification requirements (see 3.4.2), and work with the PA, the DLA Land and Maritime, to develop a SMD describing the candidate QML device(s) (see 3.5).

Upon approval of the final draft of the SMD, the manufacturer shall submit a completed certificate of compliance (C of C) to DLA Land and Maritime. Acceptance of the C of C by the qualifying activity results in the device being listed on the QML and provides authority for the manufacturer to ship the QML devices in accordance with the SMD.

Manufacturers are officially QML qualified to a given SMD when the SMD is dated and the C of C and qualification report is approved by the QA. Manufacturers are able to ship SMD devices upon being QML qualified to the given SMD. Manufacturers will receive notification of approval from the QA.

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APPENDIX H

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APPENDIX J

TECHNOLOGY CONFORMANCE INSPECTION AND SCREENING INFORMATION

J.1 SCOPE

J.1.1 Scope. The qualified manufacturer listing (QML) program measures and evaluates the manufacturers' manufacturing process against a baseline for that process. This baseline can include innovative and improved processes that result in an equivalent or higher quality product, provided that the process used to evaluate and document these changes has been reviewed and approved. Changes to the process baseline can be made by the manufacturer's Technology Review Board (TRB) after achieving QML status with documented reliability and quality data. The approach outlined in this appendix is a proven baseline which contains details of the screening and technology conformance inspection (TCI) procedures. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. However, for QML microcircuits the manufacturers may offer approved alternatives that demonstrate a process control system that achieves at least the same level of quality and reliability as could be achieved by this appendix.

J.2 APPLICABLE DOCUMENTS

J.2.1 General. The documents listed in this section are specified in section J.3 of this appendix. This section does not include documents cited in other sections of this appendix or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in section J.3 of this appendix, whether or not they are listed.

J.2.2 Government documents.

J.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil/)

J.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

SAE INTERNATIONAL

EIA557 - Statistical Process Control Systems.

(Copies of these documents are available online at https://www.sae.org/ or from SAE International, 400 Commonwealth Drive, Warrendale, PA 15096)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP121 - Requirements for Microelectronic Screening and Test Optimization.

JEP163 - Selection of Burn-in/Life Test Conditions and Critical Parameters for QML Microcircuits.

(Copies of these documents are available online at https://www.jedec.org/or from JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240–S, Arlington, VA 22201-2107.)

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J.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein(except for related specification sheets), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

J.3 TCI AND SCREENING INFORMATION

J.3.1 Mask requirements (when applicable). If the mask shop is internal to the manufacturing organization, all designs shall be checked for errors utilizing appropriate design rule checkers before start of the mask making. Before use, the mask shall be inspected for flaws and errors. The final photolithographic mask to be used for QML microcircuit wafer fabrication shall be compliant with the critical dimensions. Measurements shall show that the pattern sizes and positions are consistent with the design rules. All masks shall be maintained under an inventory control program which outlines the inspection and the release of masks to fabrication, recording of usage, cleaning cycles, and maintenance repair. All conditions for removal of masks from inventory shall be documented.

J.3.1.1 Wafer fabrication process. The wafer fabrication process shall be monitored and controlled using a standard evaluation circuit (SEC), technology characterization vehicle (TCV) or alternate assessment procedure, and parametric monitors (PMs) in accordance with 3.4.1. The wafer fabrication sequence to produce finished wafers shall be established with processing limits for each wafer fabrication step. Specific items to be addressed are detailed below:

Procedure	Paragraph
Traceability	3.11
Lot travelers	As required (TRB determined)
Glassivation/passivation	A.3.5.5, A.3.5.8
Parametric monitors	H.3.2.1.3.2
Wafer acceptance	C.3.4.1.3, H.3.2.1.2, H.3.2.1.4
Standard evaluation circuits	C.3.4.1.2, H.3.4.3
Technology characterization vehicles	H.3.2.2.2.1
Rework	In accordance with QM plan
Internal conductors and metallization thickness	In accordance with applicable design rules

J.3.2 Assembly process procedures. The following assembly process procedures shall be used, as applicable, to assemble QML microcircuits. The manufacturer shall control all phases of the assembly line to ensure that contamination from any source or equipment operation and human intervention does not degrade the reliability of the assembly process or QML microcircuit. Specific items to be addressed are shown below:

Assembly and package procedure	Paragraph
Incoming inspection	H.3.2.1.5.b.6
Eutectic die attach	TM 2010 of MIL-STD-883, H.3.2.1.5.1
Non-eutectic die attach	TM 2010, TM 5011 of MIL-STD-883, H.3.2.1.5.1 (as applicable)
Internal visual	TM 2010 of MIL-STD-883, 3.4.1.4 w
Hermeticity	TM 1014 of MIL-STD-883, TM 1018 of MIL-STD-883
Handling (electrostatic discharge (ESD))	G.3.3.1 p or 3.4.1.4 v herein
Human contamination	3.4.1.4 x
Rework	J.3.2.1
Internal gas analysis (IGA)	TM 1018 of MIL-STD-883
Wire bonding	3.4.1.4 q herein

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J.3.2.1 Assembly rework requirements. All QML microcircuit rework procedures shall be certified and documented in the quality management (QM) plan.

J.3.3 Internal visual inspection. Internal visual inspection shall be performed to the appropriate level of TM 2010 of MIL-STD-883 Microcircuits awaiting pre-seal inspection, or other accepted, unsealed microcircuits awaiting further processing shall be stored in a dry, inert, controlled environment until sealed. Alternate procedures, such as those provided in TM 5004 of MIL-STD-883 or some other TRB approved alternate, may be used. For gallium arsenide (GaAs) devices only, TM 5013 of MIL-STD-883 should be used.

J.3.4 Constant acceleration. All microcircuits shall be subjected to constant acceleration, except as modified in accordance with 4.2 in the Y1 axis only, in accordance with TM 2001 of MIL-STD-883, condition E (minimum). Microcircuits which are contained in packages that have an inner seal or cavity perimeter of two inches or more in total length, or have a package mass of five grams or more, may be tested by replacing condition E with condition D in TM 2001 of MIL-STD-883. For packages that cannot tolerate the stress level of condition D, the manufacturer shall have data to justify a reduction in the stress level. The reduced stress level shall be specified in the manufacturers QM plan. The minimum stress level allowed in this case is condition A.

J.3.5 Burn-in. The manufacturer's Technology Review Board (TRB) shall establish appropriate burn-in and life test methodology for new product families or technology by using JEDEC publication JEP163 in order to meet the quality and reliability performance requirements of MIL-PRF-38535. The burn-in and life test methodology shall be documented to the manufacturer's Quality Management (QM) plan and devices specification e.g. standard microcircuit drawing (SMD). However, JEP163 requirement shall not be applicable for legacy/heritage products and technologies. Burn-in shall be performed on all QML microcircuits, except as modified in accordance with section 4.2, at or above their maximum rated operating temperature (for devices to be delivered as wafer or die, burn-in of packaged samples from the lot shall be performed to a quantity accept level of 10(0)). For microcircuits whose maximum operating temperature is stated in terms of ambient temperature (T_A), table I of TM 1015 of MIL-STD-883 applies. For microcircuits whose maximum operating temperature is stated in terms of case temperature (T_C), and where the ambient temperature would cause T_J to exceed +175°C, the ambient operating temperature may be reduced during burn-in from +125°C to a value that will demonstrate a T_J between +175°C and +200°C and T_C equal to or greater than +125°C without changing the test duration. Data supporting this reduction shall be available to the acquiring and qualifying activities upon request.

J.3.6 Final electrical measurements. Final electrical testing of microcircuits shall assure that the microcircuits tested meet the electrical requirements of the device specification and shall include the tests of table III, group A, subgroups 1, 2, 3, 4 or 7, 5 and 6 or 8, and 9, 10, and 11, unless otherwise specified in the device specification.

J.3.7 Seal (fine and gross leak) testing. Fine and gross leak seal tests shall be performed, as specified in 4.2, between temperature cycling and final electrical testing after all shearing and forming operations on the terminals in accordance with TM 1014 of MIL-STD-883.

J.3.8 Pattern failures. Pattern failure criteria may be used as an option for any screen provided that pre burn-in testing is done. When acceptance is based on pattern failures (multiple device failures - two or more caused by the same basic failure mechanism) shall apply as specified in the acquisition document. If not otherwise specified, the maximum allowable failures shall be five devices for each failure pattern established. Accountability shall include burn-in through final electrical test.

J.3.8.1 Pattern failure rejects. When the number of pattern failures exceeds the specified limits, the burn-in lot shall be rejected. At the manufacturer's TRB option, the rejected lot may be resubmitted to burn-in one time provided:

a. The cause of the failure has been determined and evaluated.

b. Appropriate and effective corrective action has been completed to reject all microcircuits affected by the failure cause.

c. Appropriate preventive action has been initiated.

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J.3.9 TCI. TCI testing shall be accomplished by the manufacturer on a periodic basis to assure that the manufacturer's quality, reliability, and performance capabilities meet the requirements of the QM plan. The manufacturer of QML microcircuits shall be certified by the qualifying activity to use one or a combination of both of the TCI procedures described below. The two TCI procedures are end-of-line TCI (option 1, see J.3.10) and in-line TCI testing (option 2, see J.3.11).

NOTE: All tests may not be appropriate for the technology (e.g., for wafer or die product, group B, subgroups 1 and 3 and group D do not apply). The manufacturer's TRB shall determine that the appropriate tests are completed to assure conformance of the product to be delivered.

J.3.9.1 General. Any QML or SEC integrated circuit used for either TCI option (see J.3.10 or J.3.11) shall be screened in accordance with 4.2.

J.3.9.2 TCI reporting. Summary of TCI tests analysis shall be submitted to the qualifying activity in accordance with 3.9.1 requirements. If TCI requirements are not met, the TRB shall notify the qualifying activity immediately and all products manufactured and delivered between the last TCI and the failed TCI shall be placed in suspect status. The manufacturer shall analyze the failure, determine the reason for failure and submit a corrective action plan. An assessment of whether to recall all suspect products shall be made by the TRB and the qualifying activity shall be notified of the decision. Recertification and requalification of the QML line may be required based on the nature of the problem and action taken by the manufacturer. Procedures for end-of-line TCI and in-line TCI testing for a QML line are described in the following paragraphs.

J.3.9.3 Technology conformance inspection of multi-product wafer lots . If a Multi-Product Wafer (MPW) has been qualified then TCI testing sampling plan must be documented based on the same criteria used to establish the qualification criteria specified in section H.3.4.8.

a. SEM inspection shall be performed per TM 2018, (class level S only); Worst case representative design only.

b. Life test shall be performed per TM 1005; Worst case representative design only and 5 pieces sample on all other designs for class level S.

c. Total Ionizing Dose (TID) shall be performed per TM 1019; Worst case representative design only and 5 pieces sample on all other designs for class level S.

Note: If a test failure is encountered then all designs shall be reviewed to determine whether the test failure is related to all designs or the specific design that failed the test. This analysis shall be applicable to burn-in PDA, qualification, and TCI failures.

J.3.10 End-of-line TCI (option 1). End-of-line TCI testing shall be performed every TCI interval, as recommended in table J-1 herein. Quality conformance inspection (QCI) requirements as detailed in TM 5005 of MIL-STD-883 may be used, with qualifying activity (QA) approval, in place of the TCI requirements herein. Each end-of-line TCI vehicle shall pass the end-of-line quality conformance. All groups A, B, and E (as applicable) testing shall be performed on microcircuits to be delivered as QML microcircuits. Groups C and D testing shall be done on either the SEC or QML microcircuits. Groups A, B, C, D, and E requirements are found in tables II through V and table C-I herein.

Group E inspection is required only for parts intended to be marked as radiation hardness assurance (RHA) (see 3.4.3). RHA TCI sample tests shall be performed at the level(s) specified and in accordance with appendix C. The applicable subgroups of group E, (see appendix C) shall be performed when specified in the acquisition document. The actual devices used for group E testing shall be assembled in a qualified package and, as a minimum, shall pass table III, group A, subgroups 1, 7, and 9 at +25°C prior to irradiation.
NOTE: If a manufacturer elects to eliminate a TCI step by substituting an in-process control or statistical process control procedure, the manufacturer is only relieved of the responsibility of performing the TCI operation associated with that step. The manufacturer is still responsible for providing a product that meets all of the performance,

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quality, and reliability requirements herein and in the device specification. Documentation supporting substitution for TCI shall be retained by the manufacturer and available to the QA upon request.

Each group may contain individual subgroups for the purposes of identifying individual tests or groups of tests. Subgroups within a group of tests may be performed in any sequence but individual tests within a subgroup (except table II, group B, subgroup 2) shall be performed in the sequence indicated for groups B, C, D, and E tests herein. Electrical reject devices from the same inspection lot may be used for all subgroups when electrical end-point measurements are not required.

J.3.10.1 Group A inspection. Group A inspection shall be performed on each inspection lot and shall consist of electrical parameter tests specified for the specified device. Group A inspection may be performed in any order.

J.3.10.2 Group B inspection. Group B inspection shall be performed on each inspection lot, for each qualified package type and lead finish. Group B shall consist of mechanical and environmental tests for the specified device class. Resubmission procedures shall be documented in the QM plan. For solderability, a statistical sound sample size (sample sizes indicated in TM 5005 of MIL-STD-883 are acceptable, as a minimum) consisting of leads from several packages shall be tested with zero failures. The actual number shall be determined by the TRB and detailed in the TCI procedures in the QM plan.

J.3.10.3 Group C inspection. Group C inspection shall include die related tests specified which are performed periodically. Resubmission procedures shall be documented in the QM plan. Where group C end-points are done on actual devices, group C end-points shall be specified in the device specification.

J.3.10.4 Group D inspection. Group D inspection shall include package related tests which are performed periodically. Resubmission procedures shall be documented in the QM plan. Where group D end-points are done on actual devices, group D end-points shall be specified in the device specification.

J.3.10.5 Group E inspection. When applicable, group E inspection shall include RHA tests on each wafer lot. The post-irradiation parameter limits (PIPL), transient, and single event phenomenon (SEP) response (as applicable), and test conditions shall be as specified in the device specification.

J.3.10.6 End-point tests for groups C, D, (E if applicable). End-point measurements and other specified post-test measurements shall be made for each sample after completion of all other specified tests in the subgroup. The test limits for the end-point measurements shall be the same as the test limits for the respective group A subgroup inspections. Different end-points may be specified for group E tests in the detail specifications. Any additional end-point electrical measurements may be performed at the discretion of the manufacturer.

J.3.10.7 End-of-line TCI testing (option 1). All microcircuits used in end-of-line TCI testing that meet the requirements of this specification and the device specification and are subjected to destructive tests or which fail any test shall not be shipped on the contract or order as acceptable QML product. They may, however, be delivered at the request of the acquiring activity, if they are isolated from, and clearly identified so as to prevent their being mistaken for acceptable product. Sample microcircuits, from lots which have passed quality assurance inspections or tests and which have been subjected to mechanical or environmental tests specified in groups B, C, and D inspection and not classified as destructive, may be shipped on the contract or order provided the test has been proven to be nondestructive (see A.4.3.2.3) and each of the microcircuits subsequently passes final electrical tests in accordance with the applicable device specification.

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J.3.11 In-line TCI testing (option 2). In-line control testing shall be performed through the use of the approved SEC or QML microcircuit. The in-line control test plan shall show how all the groups A, B, C, D, and E test conditions are incorporated under statistical process control or process control to allow in-line control monitoring. The following shall also be addressed. Groups A, B, C, D, and E requirements are found in tables II through V and table C-I.

TABLE J-I. End-of-line TCI testing procedure (option 1). 1/

Table	TCI requirements	TCI vehicle	Interval
Table III	Group A electrical testing	Actual device	Each inspection lot
Table II	Group B testing	Actual device	Each inspection lot
Table IV	Group C testing	SEC or actual device	Every 3 months
Table V	Group D testing	SEC or actual device	Every 6 months
Table C-I	Group E testing	Actual device	Each wafer lot

1/ Each group may contain individual subgroups for the purposes of identifying individual tests or groups of tests.

J.3.11.1 Group A electrical testing. Group A electrical testing shall be satisfied by in-line inspections performed in accordance with the applicable procedure of MIL-STD-883 on actual devices.

J.3.11.2 Group C life tests. Life tests shall be performed on the SEC at intervals set by the TRB in the quality management plan.

J.3.12 Test optimization requirements. The process used by the manufacturer to optimize testing utilizing the best commercial practices available while still assuring all performance, quality and reliability requirements herein. All of the applicable JEP121 process elements shall be addressed for test optimization. To obtain test optimization validation on a particular microcircuit device technology family(see table A-VI to A-IX), manufacturers TRB shall analyze 10 wafer or module inspection lots or 2 years period of test data of a candidate test for screening and TCI/QCI test, wherein test data shows steady results of the devices performance characteristics limit. Any screen or TCI test prescribed herein may be reduced, modified, moved, or eliminated by the QML manufacturer provided the following considerations are addressed as a minimum.

a. Nodes critical to test outcome, called test critical nodes, have been identified and are in control in accordance with SAE EIA557.

b. Test critical nodes have exhibited sufficient capability to assure low product defect rates.

c. An understanding and control of assignable causes at test critical nodes.

d. The long term reliability of devices remains unaffected or is improved.

e. Low defect rates in the process and delivered product are maintained.

f. Measurements taken for out of control conditions along with corrective actions are recorded and this data is maintained for a time period consistent with data retention requirements herein.

g. For screening test, method and frequency for revalidation of optimized tests shall be conducted on every 20^{th} inspection lots or every 2 years or as defined by the manufacturer's documentation.

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h. For periodic TCI/QCI test, method and frequency for revalidation of optimized tests shall be conducted on every 20th inspection lots or every 2 years or as defined by the manufacturer's documentation.

The manufacturer shall maintain the established process control and evaluate the effect on quality and reliability of any out of control conditions that may exist at critical nodes. The manufacturer shall also evaluate if a relationship exists between any optimized test and any field failure returns, take appropriate corrective actions, and report this information as part of the TRB status reports. Regardless of testing modifications, the manufacturer shall supply product capable of passing any screening or TCI/QCI test prescribed herein. As a part of the QML philosophy and the conversion of customer requirements the manufacturer shall communicate variations in screening, end-of-line testing with customers as appropriate. This information shall be available from the manufacturer and to the QA. Any major change listed in table A-I occurred, the affected test optimization for screening/TCI/QCI test shall be revoked immediately, to re-establish validation of test optimization test manufactures shall follow all test optimization requirements, and required TRB's review and QA approval.

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APPENDIX J

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DLA - CC

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DLA - CC

Review activities:
Army - MI, SM
Navy - AS, CG, MC, OS, SH
Air Force - 19

Civil agency:
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