INCH-POUND

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PERFORMANCE SPECIFICATION

HYBRID MICROCIRCUITS, GENERAL SPECIFICATION FOR

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This specification is approved for use by all Departments and Agencies of the Department of Defense.

This document is a performance specification. It is intended to provide the device manufacturers an acceptable established baseline in order to support Government microcircuit applications and logistic programs. The basic document has been structured as a performance specification that is supplemented with detailed appendices. These appendices provide guidance to manufacturers on demonstrated successful approaches to meeting defense performance requirements. These appendices are included as a performance benchmark and are intended to impose mandatory requirements.

1. SCOPE

1.1 Scope. This specification establishes the general performance requirements for hybrid microcircuits, multi-chip modules (MCM) and similar devices, and the verification requirements for ensuring that these devices meet the applicable performance requirements. Verification is accomplished through the use of one of two quality programs (Appendix A). The main body of this specification describes the performance requirements and the requirements for obtaining a Qualified Manufacturers List (QML) listing. The appendices of this specification are intended for guidance to aid a manufacturer in developing their verification program. Detail requirements, specific characteristics, and other provisions that are sensitive to the particular intended use should be specified in the applicable device acquisition specification.

1.2 Description of this specification. The intent of this specification is to allow the device manufacturer the flexibility to implement best commercial practices to the maximum extent possible while still providing a product which meets the military performance needs. Devices that are compliant to this specification are those that are capable of meeting the verification requirements outlined herein; and are built on a manufacturing line which is controlled by the manufacturer's quality management program and has been certified and qualified in accordance with the requirements herein. The certification and qualification requirements outlined herein are the requirements to be met by a manufacturer to be listed on the (QML). The manufacturer may modify, substitute, or delete the tests and inspections defined herein. This is accomplished by baselining a flow of tests and inspections that will assure that the devices are capable of meeting the generic verifications provided in this specification. This does not necessarily mean that compliant devices have been subjected to the generic performance verifications provided in this specification, just that compliant devices are capable of meeting them. It is the manufacturer's responsibility to ensure that their devices are capable of meeting the generic performance verifications applicable to each specified product assurance level.

Appendix A defines the quality management program that may be implemented by the manufacturer. Appendix A includes an option to use a quality review board concept, hereafter referred to as the Technology Review Board (TRB) in this document, which may be used to modify the generic verification, design, and construction criteria provided in this specification. Appendix B is not currently being used. Appendix C defines generic performance verifications. These verifications consist of a series of tests and inspections which may be used to verify the performance of devices. They may be used as is or modified as allowed by this specification. Appendix D defines generic performance verifications for non-hermetic device technologies. Appendix E defines generic design and construction criteria relative to this technology, including rework limitations and major change testing guidance. Appendix F provides statistical sampling procedures. Appendix G provides the requirements for Radiation Hardness Assurance (RHA).

1.3 Classification. Seven quality assurance levels are provided for in this specification. Four of these classes, in highest to lowest order, are K, H, G and D, as defined below. The fifth class is Class E, the quality level associated with a Class E device is defined by the acquisition document. The sixth and seventh classes are L and F for non-hermetic devices, with Class L being the higher quality assurance level.

1.3.1 Class K. Class K is the highest reliability level provided for in this specification. It is intended for space applications.

1.3.2 Class H. Class H is the standard military quality level.

1.3.3 Class G. Class G is a lowered confidence version of the standard military quality level (H) with QML listing in accordance with 4.5.2.2, a possibly lower temperature range (-40°C to +85°C), a manufacturer guaranteed capability to meet the Class H conformance inspection and periodic inspection testing, and a vendor specified incoming test flow. The device will meet the Class H requirements for in-process inspections and screening.

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1.3.4 Class D. Class D is a vendor specified quality level available to this specification. This is a possibly lower temperature range (0°C to +70°C) part with a vendor specified test flow available from a QML listed manufacturer.

1.3.5 Class E. Class E designates devices which are based upon one of the other classes (L, K, H, G, or F) with exceptions taken to the requirements of that class. These exceptions are specified in the device specification, therefore the device specification should be carefully reviewed by the user to ensure that the exceptions taken will not adversely affect the performance of the system.

1.3.6 Class L. Class L is the highest quality class for non-hermetic devices.

1.3.7 Class F. Class F is the standard quality class for non-hermetic devices.

2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

2.2 Government documents.

* 2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-I-46058 - Insulating Compound, Electrical (For Coating Printed Circuit Assemblies).
MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-750 - Test Methods for Semiconductor Devices.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-1331 - Handbook for parameters to be controlled for the specification of microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil).

* 2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

QML-38534 - Qualified Manufacturer's List of Products Qualified Under Performance Specification MIL-PRF-38534, Hybrid Microcircuits General Specification For.

(Copies of these documents are available online at https://quicksearch.dla.mil).

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2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEDEC Publication JEP133 - Guide for the Production and Acquisition of Radiation-Hardness-Assured Multichip Modules and Hybrid Microcircuits.

(Copies of this document are available online at https://www.jedec.org/)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Performance requirements for Class K devices. Class K devices shall be capable of meeting the Class K tests and inspections of Appendices C and E (see table I). This shall include the incoming inspection flow, the in-process inspection flow, the screening flow, and the conformance inspection and periodic inspection flow. These devices shall be specified over the temperature range of -55ºC to +125ºC or as specified in the device specification. Manufacturers of these devices shall be fully certified and qualified in accordance with this specification. Verification of these performance requirements shall be performed as described in 4 herein.

3.2 Performance requirements for Class H devices. Class H devices shall be capable of meeting the Class H tests and inspections of Appendices C and E (see table I). This shall include the incoming inspection flow, the in-process inspection flow, the screening flow, and the conformance inspection and periodic inspection flow. These devices shall be specified over the temperature range of -55ºC to +125ºC or as specified in the device specification. Manufacturers of these devices shall be fully certified and qualified in accordance with this specification. Verification of these performance requirements shall be performed as described in 4 herein.

3.3 Performance requirements for Class G devices. Class G devices shall be capable of meeting the Class H tests and inspections of Appendices C and E, except incoming inspection (see table I). This shall include the in-process inspection flow, the screening flow, and the conformance inspection and periodic Inspection flow. Compliance with the conformance inspection and periodic inspection flow shall be guaranteed by the manufacturer. Actual completion of conformance inspection and periodic inspection tests and inspections are optional and at the manufacturer's discretion. DLA Land and Maritime approval or notification is not required to eliminate conformance inspection and periodic inspection tests and inspections for this class of device; however, it is the manufacturer's responsibility to ensure that their devices are capable of passing these tests and inspections. These devices shall be specified over the temperature range of -40ºC to +85ºC or a wider range. Manufacturers of these devices shall be fully certified and QML listed in accordance with this specification. Verification of these performance requirements shall be performed as described in 4 herein.

3.4 Performance requirements for Class E devices. Class E devices are devices which meet all of the requirements of one of the other classes (K, H, or G) with some exceptions taken. The device specification shall clearly state which class the device is based upon (K, H, or G) and what exceptions are being taken. The users of these devices should carefully examine the device specification to verify that the exceptions being taken will not adversely affect the system performance. Manufacturers of these devices shall be fully certified in accordance with this specification. Verification of the performance requirements shall be performed as described in herein.

3.5 Performance requirements for Class D devices. Class D devices are built and tested in accordance with the manufacturer's specified production and testing flow (see table I). These devices shall be capable of meeting the specified electrical tests. However, these devices are not required to meet any of the tests and inspections of this specification. These devices shall be specified over the temperature range of 0ºC to +70ºC or a wider range. Manufacturers of these devices shall be fully certified and QML listed in accordance with this specification. Verification of these performance requirements shall be performed as described in 4 herein.

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3.6 Performance requirements for radiation hardness assurance (RHA) devices. Compliant RHA devices shall meet the additional performance requirements of Appendix G. Detailed information for producing and acquiring RHA devices can be found in JEDEC publication JEP133 “Guide for the Production and Acquisition of Radiation-Hardness-Assured Multichip Modules and Hybrid Microcircuits”.

3.7 Performance requirements for Class F non-hermetic devices. Class F devices shall be capable of meeting the Class F tests and inspections of Appendices D and E (see table I). This class shall include the element evaluation flow, in-process inspection flow, screening flow, conformance inspection (CI), and the periodic inspection (PI) / qualification manufacturer list (QML) flow. These devices shall be specified over the temperature range of -40°C to +85°C or a wider range. Manufacturers of these devices shall be fully certified and qualified in accordance with Appendix D. Verification of the applicable performance requirements shall be performed as described in D6, D7, and D8 herein.

3.8 Performance requirements for Class L non-hermetic devices. Class L devices shall be capable of meeting the Class L tests and inspections of Appendices D and E (see table I). This class shall include the element evaluation flow, in-process inspection flow, screening flow, conformance inspection (CI), and the periodic inspection (PI) / qualification manufacturers list (QML) flow. These devices shall be specified over the temperature range of -55°C to +125°C or as specified in the device specification. Manufacturers of these devices shall be fully certified and qualified in accordance with Appendix D. Verification of the applicable performance requirements shall be performed as described in D6, D7, and D8 herein.

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* TABLE I. Performance requirements summary.

Test flow or requirement 1/	Class						
	D	E 2/	G 2/	H 2/	K 2/	F	L
Certification	Required	Required	Required	Required (Class H)	Required (Class K)	Required	Required
QML listing	Required IAW 4.5.2.2	Required in accordance with the applicable device class and the device specification	Required IAW 4.5.2.2	Required IAW 4.5.2.1	Required IAW 4.5.2.1	Required IAW 4.5.2.2	Required IAW 4.5.2.2
Incoming inspection (appendix C or D as applicable)	Manufacturer specified 3/		Manufacturer specified 3/	Applicable (Class H) 1/	Applicable (Class K) 1/	Applicable (Class F) 1/	Applicable (Class L) 1/
In-process inspections (appendix C or D as applicable)	Manufacturer specified 3/		Applicable (Class H) 1/	Applicable 1/	Applicable 1/	Applicable 1/	Applicable 1/
Screening (appendix C or D as applicable)	Manufacturer specified 3/		Applicable (Class H) 1/	Applicable (Class H) 1/	Applicable (Class K) 1/	Applicable (Class F) 1/	Applicable (Class L) 1/
Conformance inspection and periodic inspection (appendix. C or D as applicable)	Manufacturer specified 3/		Guaranteed (Class H) 4/	Applicable (Class H) 1/	Applicable (Class K) 1/	Applicable (Class F) 1/	Applicable (Class L) 1/
Temperature range 5/	0ºC to +70ºC		-40ºC to +85ºC	-55ºC to +125ºC	-55ºC to +125ºC	-40ºC to +85ºC	-55ºC to +125ºC

1/ For test flow implementation and available flexibility see 3.9.1.
2/ Design and construction and rework criteria are as specified in Appendix E and shall be utilized in accordance with 3.9.1.
3/ Manufacturer specified states that the manufacturer does not have to take the generic criteria of this specification into consideration during the establishment of its manufacturing and test flows. The manufacturer's flow may or may not meet the same requirements as the flow of this specification. In addition, the manufacturer may specify that they do not perform the particular test or inspection flow.
4/ Guaranteed (Class H) means that the manufacturer is assuring that their devices shall meet the conformance inspection and periodic inspection test flow contained in tables C-Xa, C-Xb, C-Xc, and C-Xd, but may or may not actually perform the tests and inspections specified. Elimination of these tests and inspections does not necessitate DLA Land and Maritime approval or notification.
5/ Classes D and G may be specified at wider temperature ranges. Classes H and K shall be -55ºC to +125ºC unless otherwise specified in the device specification.

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3.9 General. The manufacturer of devices, in compliance with this specification, shall have and use production and test facilities and a verification program adequate to assure successful compliance with the provisions of this specification and the associated device specification. Adequacy of a device manufacturer to meet the requirements of this specification shall be determined by the Government qualifying activity. The individual item requirements shall be as specified in the associated device specification and as specified herein. Only devices which meet all the performance requirements of this specification and the associated device specification, and have been adequately verified, shall be marked as compliant and delivered.

Monolithic microcircuits may be built to Class K, H, G, E, D, L, or F performance requirements of MIL-PRF-38534 only when all of the following conditions are met:

a. The monolithic microcircuit is already listed on MIL-PRF-38535 SMD and has no current source of supply.

b. The military service or space agencies have a need for the non-sourced MIL-PRF-38535 SMD device.

c. No MIL-PRF-38535 monolithic microcircuit manufacturer is found by the preparing activity to supply the device on the existing MIL-PRF-38535 SMD.

Only when these conditions are met may a new MIL-PRF-38534 hybrid SMD then be developed to supply the military services or space agencies with a similar monolithic microcircuit device qualified to MIL-PRF-38534. Monolithic microcircuits offered in compliance with this specification shall be specified on a Standard Microcircuit Drawing (SMD).

Facilities and programs listed on the Qualified Manufacturer's List (QML) may be used for the manufacture of other than compliant devices; however, any use of reference to compliant device marking, Class K, H, G, E, D, L, or F certification status, or this specification in such a way as to state or imply equivalency (and thereby Governments endorsement) in connection with noncompliant devices is prohibited and may be cause for revocation of certification or QML status (or both). Terms definitions, methods, and symbols are in accordance with 6.4. Any defense specification or standard referred to in this specification may be replaced by and equivalent commercial standard as determined by the preparing activity.

3.9.1 Implementation of this specification. All devices offered and shipped in compliance with this specification shall meet the performance requirements specified for the applicable device class. The manufacturer shall verify that devices meet the performance requirements of the applicable device class. The manufacturer is responsible for developing a verification program which shall meet this requirement. The appendices of this specification give standard methods for verifying that the devices meet the performance requirements (except for Class D). The manufacturer may address the requirements of this specification as written, adapt them to their products, or develop a new methodology. Prior to the manufacturer being certified, the actual verification program to be used shall be reviewed and approved by DLA Land and Maritime. Any deletions or changes to the test flow shall also be reviewed and approved by DLA Land and Maritime or the manufacturer's DLA Land and Maritime approved Technology Review Board (TRB) prior to implementation. In this manner, a manufacturer may use an alternative method to the method specified in this specification to evaluate their parts if the alternate method verifies the same performance requirement. Furthermore, the manufacturer may eliminate a test or inspection (or decrease the occurrence or sample size of the test or inspection) if it is shown that the test or inspection is not necessary or can be performed less frequently. It is the manufacturer's responsibility to show how their verification program (and any changes to it) meets the requirements of this specification. The manufacturer shall analyze the impact of major changes and their effect on previously approved modifications of tests (test optimization). See table II for clarification.

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TABLE II. Implementation summary.

<table>
<tr><th>Option</th><th>Definition</th><th>Typical examples</th><th>Implementation procedures</th></tr>
<tr><td>Meet requirement as written</td><td>The manufacturer performs the test or requirement as specified.</td><td>Self explanatory</td><td>The manufacturer implements the test or requirement into internal documentation, verified during certification.</td></tr>
<tr><td rowspan="2">Alternate method to the requirement</td><td rowspan="2">The manufacturer assures that the intent of the requirement is met, but does not perform the test/requirement exactly as written.</td><td rowspan="2">- Replacement of a test with statistical process control (SPC) or alternate method.
- Historical data analysis shows that the requirement is met.
- Design verification/validation shows that the process is capable of meeting the requirement.
- Requirement does not address new materials, technologies, or designs.</td><td>For TRB companies, alternate method and appropriate justification are approved by the manufacturer's TRB.</td></tr>
<tr><td>For traditional companies, manufacturer proposes the alternate method and justification to the qualifying activity for approval.</td></tr>
<tr><td rowspan="4">Elimination of the requirement</td><td rowspan="2">The manufacturer proves that the test or requirement is either:

Non-value added</td><td colspan="2"></td></tr>
<tr><td>- Test does not stress the process adequately (e.g., PIND for encapsulated parts).
- Historical data analysis shows that the test does not induce failures.</td><td>Elimination is achieved in the same manner as alternate methods described above.</td></tr>
<tr><td>The product will not comply with the test or requirement due to technology limitations.</td><td>- Configuration of the product (i.e., size, mass, package) is incompatible with the test method.</td><td>The exception shall be documented in the applicable acquisition document. Product is classified as Class E.</td></tr>
<tr><td>Application has no need of the requirement.</td><td>The device will not experience the particular stress in the application.</td><td>The exception shall be documented in the applicable acquisition document. Product is classified as Class E.</td></tr>
</table>

3.9.2 Device specification. The preferred device specification for devices built in full compliance with this specification is a SMD. Monolithic microcircuits built in compliance with this document shall be documented on an approved SMD.

3.9.3 Design and construction. The design and construction of compliant devices shall address the limitations and guidelines of Appendix E.

3.9.3.1 Lead finish. Appendix E provides the general interface requirements for lead finishes.

3.9.4 QML qualification requirements. Hybrid microcircuits furnished under this specification shall be products which are authorized by the qualifying activity for listing on the QML. Qualification testing shall be performed in accordance with the agreed upon qualification plan. (See appendix C for guidance on qualification testing.)

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3.9.5 Marking of devices. Marking shall be in accordance with the requirements of this specification and the device specification. The marking shall be legible and complete, and shall meet the resistance to solvents requirements of method 2015 of MIL-STD-883. When mechanical or laser marking is performed, it shall be clearly visible through those conformal coatings approved for use in MIL-I-46058 (see method 2015 of MIL-STD-883 if contrasting material or ink is used to highlight the trace). Mechanical or laser marked metal surfaces shall meet all applicable microcircuit finishes and shall not degrade the performance requirements of the device. Mechanical or laser marking shall be approved by the qualifying activity. If any special marking is used, it shall in no way interfere with the marking required herein, and shall be visibly separated therefrom. The following marking shall be included on each microcircuit unless otherwise specified.

a. Part or Identifying Number (PIN) (see 3.9.5.1).

b. Index point (see 3.9.5.2).

c. Lot identification code or date code (see 3.9.5.3).

d. Device manufacturer's identification (see 3.9.5.4).

e. Device manufacturer's CAGE CODE. The CAGE CODE online database is available at https://cage.dla.mil/ (see 3.9.5.5).

f. Country of manufacture (see 3.9.5.6).

g. Serialization, when applicable (see 3.9.5.7).

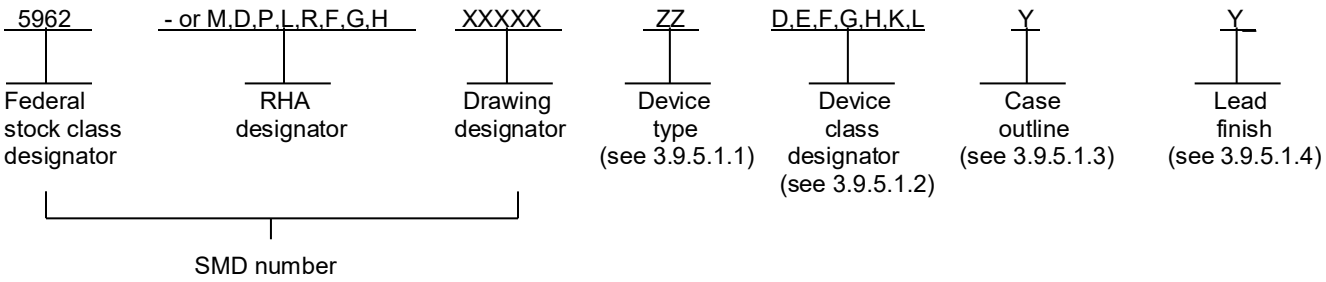
h. Special marking (see 3.9.5.8).

i. Electrostatic discharge (ESD) sensitivity identifier (see 3.9.5.8.2).

j. Certification mark (see 3.9.5.8.3).

Unless otherwise specified, the certification mark, the PIN, the inspection lot identification code, and the ESD identifier shall be located on the top surface of flat packages or dual-in-line configurations and on either the top or the side of cylindrical packages (TO configurations and similar configurations).

3.9.5.1 Part or Identifying Number (PIN). Each Standard Microcircuit Drawing (SMD) microcircuit shall be marked with the complete PIN, as specified in the SMD. The number sequence for MIL-PRF-38534 is 5962-XXXXXZZHYY, where:



3.9.5.1.1 Device type. The device type shall identify the circuit function as indicated in the SMD.

3.9.5.1.2 Device class designator. This device class designator shall be a single letter identifying the quality level in accordance with the SMD.

3.9.5.1.3 Case outline. The case outline shall be designated by a single letter assigned to each outline within each SMD.

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3.9.5.1.4 Lead finish. Lead frame or terminal material and finish shall be as specified (see Appendix E). The lead finish shall be designated by a single letter as follows:

Finish letter	Lead finish (see note)
A	Hot solder dip
B	Tin-lead plate
C	Gold plate
X	Finishes A, B, or C (see note)

NOTE: Finish letter "X" shall not be marked on the microcircuit or its packaging. This designation is provided for use in drawings, part lists, acquisition orders, or other documentation where lead finishes A, B, and C are all considered acceptable and interchangeable without preference. For Government logistic support, the A lead finish will be acquired and supplied to the end user when the X is included in the PIN for lead finish. If the PIN is not available with the A lead finish, the same PIN will be acquired except with the C or B lead finish designator as determined by availability. Type C terminal material is a fired on metallization used with leadless chip carriers.

3.9.5.2 Index point. The index point, tab, or other marking indicating the starting point for numbering of leads or for mechanical orientation shall be as specified and shall be applied so that it is visible from above when the microcircuit is installed in its normal mounting configuration. The outline of an equilateral triangle (i.e., Δ), which may be used as an electrostatic identifier (see 3.9.5.8.2), may also be used as the pin 1 identifier.

3.9.5.3 Lot identification code (date code). Devices shall be marked by a unique code to identify the week of final seal. The first two numbers in the code shall be the last two digits of the number of the year, the third and fourth numbers shall be two digits indicating the calendar week of the year. When the number of the week is a single digit, it shall be preceded by a zero. Reading from left to right or from top to bottom, the code number shall designate the year and week, in that order (e.g., 8806 equals week 6 of 1988).

3.9.5.4 Manufacturer's identification. Devices shall be marked with the name or trade mark of the manufacturer. The identification of the equipment manufacturer may appear on the device only if the equipment manufacturer is also the device manufacturer.

3.9.5.5 Manufacturer's designating symbol. When space permits, the manufacturer may mark the CAGE code on devices. CAGE codes can be found using the online database references in 3.9.5.e. The designating symbol shall be used only by the manufacturer to whom it has been assigned and only on those devices manufactured at the manufacturer's plant. In the case of small devices, the manufacturer's designating symbol may be abbreviated by omitting the first "C" in the series of letters.

3.9.5.6 Country of manufacture. The manufacturer shall indicate the country where the device was manufactured (i.e., substrate and element attach, interconnect, seal). At the option of the manufacturer, the country of manufacture marking may be omitted from the body of the device but shall be retained on the initial container.

3.9.5.7 Serialization. Serialization allows traceability of electrical tests results (variables data) to an individual device.

3.9.5.7.1 Class K and L serialization. Prior to the first recorded electrical measurement in screening, each Class K and L device shall be marked with a unique serial number assigned consecutively. Lot records shall be maintained to provide traceability from the serial number to the specific incoming inspection lots from which the elements originated.

3.9.5.7.2 Class H, G, D and F serialization. Serialization of Class H, G, D and F devices shall only be required when specified in the device specification.

3.9.5.8 Special marking. When the size of a package is insufficient to allow marking of special process identifiers on the top surface, the back side of the package may be used for these markings except the ESD identifier shall be marked on the top. Button cap flat packs with less than, or equal to, 16 leads may have the identifier marked on the ceramic. Back side marking with conductive or resistive ink shall be prohibited on nonconductive surfaces.

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* 3.9.5.8.1 Beryllium oxide package identifier. If a device package contains beryllium oxide, the device shall be marked with this designation: BeO.

NOTE: Packages containing beryllium oxide will not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllium oxide or beryllium dust. Furthermore, beryllium oxide packages will not be placed in acids that will produce fumes containing beryllium.

3.9.5.8.2 Electrostatic discharge (ESD) sensitivity identifier. ESD classification levels are defined as follows when tested in accordance with method 3015, of MIL-STD-883.

NOTE: The appropriate class is specified by the device passing at any voltage in a given classification level range; passing the highest voltage level in the classification level range is not required (e.g. If a device passes at 900 V and fails at 999 V, it will be classified as Class 1B).

ESD classification designator level shall be as defined as follows and in accordance with C.6.3.3.4 and D.8.5.

ESD class designator	Prior designation category	Optional individual part marking 1/	Required shipping container marking 1/	Electrostatic voltage
0		∆0	∆0	<250 V
1A 2/		∆A	∆A	250 V – 499 V
1B		∆B	∆B	500 V - 999 V
1C		∆C	∆C	1,000 V – 1,999 V
1 3/ 4/ 5/		∆ 3/ 4/	∆ 3/ 4/	0 - 1,999 V
2 5/		∆∆	∆∆	2,000 - 3,999 V
3 3/ 4/		∆∆∆ 4/	∆∆∆ 4/	≥ 4,000 V
3A		∆∆∆A	∆∆∆A	4,000 V – 7,999 V
3B		∆∆∆B	∆∆∆B	≥ 8,000 V

1/ The manufacturer may mark the part as indicated under “Optional Individual Part Marking” as class 1 (single triangle ∆) or the “Optional Individual Part Marking” may be used as the pin 1 identifier. After 1 November 2006, the required packaging or documentation marking shall be used.

2/ If ESD testing is performed at one test level only IAW C.6.3.3.4 and the device fails at 250 V, it is classified as Class 0 and if the device passes 250 V, it is classified as Class 1A.

3/ ESD class designator 1 has been replaced with designators 0, 1A,1B, and 1C and ESD class 3 designator has been replaced with 3A and 3B ESD class designators as of 24 March 2006

4/ Devices not yet ESD re-classified may continue to be marked as class 1 (single triangle) or class 3 until testing determines the appropriate class. The class 1 single (∆) may be used as a pin 1 identifier. The manufacturer may mark the part as indicated under “Optional Individual Part Marking” (see C.6.3.3.4 for testing requirements.) After 24 March 2006, (for newly qualified product-PI), the 0, 1A, 1B, 1C, 3A, and 3B designators shall be used with the appropriate marking.

5/ Devices previously classified by test as category A may be designated as class 1 and devices classified as category B may be designated as class 2.

3.9.5.8.3 Certification mark. All devices acquired to and meeting the requirements of this specification, and the applicable associated device specification, shall bear a certification mark as shown in table III.

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TABLE III. Certification mark.

Device Specification	Class	Certification mark
SMD	All	QML or Q for small devices
Non-SMD dated after this document	K	CK
	H	CH
	G	CG
	E	CE
	D	CD
Non-SMD dated prior to this document	All	CH or C for small devices
Non-SMD RHA devices	All	See G.3.4

These certification marks, or the abbreviations "Q" or "C", shall not be used for any device acquired under contracts or orders which permit or require any changes to this specification except as allowed in 3.9.1. In the event that a lot fails to pass inspection, the manufacturer shall remove or obliterate the certification mark from the sample tested and also from the devices represented by the sample.

3.9.5.9 Marking option for controlled storage of Class H and G. Where devices are subjected to testing and screening in accordance with some portion of the quality assurance requirements and stored in controlled storage areas pending receipt of orders requiring conformance to the same or a different level, the inspection lot identification code shall be placed on the device package along with the other markings specified in 3.9.5 sufficient to assure identification of the material. As an alternative, if the microcircuits are stored together with sufficient data to assure traceability to processing and inspection records, all markings may be applied after completion of all inspection to the specified level.

3.10 Item requirements. The individual item requirements, including temperature range, for devices delivered under this specification shall be documented in the device specification.

3.10.1 Certification of conformance. Manufacturers, or distributors, who offer compliant devices described by this specification shall provide written certification, signed by the corporate officer who has management responsibility for the production of the devices, that the devices are built, tested, and handled in accordance with this specification and that they meet or exceed the performance requirements for the applicable class. The responsible corporate official may, by documented authorization, designate other responsible individuals to sign the certificate of conformance, but, the responsibility for conformity to the facts shall rest with the responsible corporate officer. The certificate shall include the following information:

a. Manufacturer documentation:

(1) Manufacturer’s name and address.

(2) Customer’s or distributor’s name and address.

(3) Acquisition order number.

(4) Device type and Class level (SMD part numbers include both).

(5) Date code.

(6) Assembly plant location, if applicable.

(7) Quantity of devices in shipment from manufacturer.

(8) Statement certifying QML microcircuit conformance and traceability.

(9) Signature and date.

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b. Distributor documentation for each distributor:

(1) Distributor's name and address.

(2) Name and address of customer.

(3) Quantity of devices in shipment.

(4) Latest re-inspection date, if applicable.

(5) Certification that this shipment is a part of the shipment covered by the manufacturer's documentation.

(6) Signature and date.

(7) Contract number.

(8) Part number.

(9) Company or distributor from which parts were received.

(10) Include all documentation from 3.10.1.a.

3.11 Recycled, recovered, environmentally preferable, or biobased materials. Recycled, recovered, environmentally preferable, or biobased materials should be used to the maximum extent possible, provided that the material meets or exceeds the operational and maintenance requirements, and promotes economically advantageous life cycle costs.

3.12 Workmanship. Devices shall be manufactured, processed, and verified to meet the performance requirements of this specification; and with the production practices, workmanship instructions, inspection and test procedures, and training aids prepared by the manufacturer in fulfillment of the baseline process flow.

3.12.1 Rework and repair provisions. All rework and repair operations shall address the limitations and guidelines of Appendix E.

4. VERIFICATION

4.1 General verification. All items shall meet all requirements of section 3. The manufacturer is responsible for verifying that product delivered to this specification meets the performance requirements as stated in section 3. The absence of any inspection requirements in the specification shall not relieve the contractor of the responsibility of ensuring that all products or supplies submitted to the Government for acceptance comply with all requirements of the contract. Sampling inspection, as part of manufacturing operations, is an acceptable practice to ascertain conformance to requirements, however, this does not authorize submission of known defective material, either indicated or actual, nor does it commit the Government to accept defective material.

4.2 Quality Management (QM) Program. Manufacturers of compliant devices to this specification shall have in place, or shall implement a quality management program, (see Appendix A). This system will be used to verify that devices meet the applicable performance requirements of section 3. This system will be verified by the qualifying activity, see 4.5 herein.

4.3 Baseline process flows. Manufacturers of compliant devices to this specification shall implement a baseline process flow detailing the processes, tests, inspections/monitors, material entry points, and the order in which operations are performed. Appendices C, D and E provide generic verifications, design, and construction criteria for use in developing these flows. The criteria and verifications identified in Appendices C, D and E may be modified as specified in 3.9.1 herein. The baseline flow will be verified by the qualifying activity, see 4.5 herein. The baseline process flow used to list a QML manufacturer as Class G or D may be one or more of its product manufacturing flows (e.g., travelers) that are representative of the manufacturer's processes and materials.

4.4 Quality management (QM) plan. The manufacturer's QM plan reflects the major elements of the quality management program. The QM plan shall be available at, and continually effective in, the manufacturer's plant.

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4.4.1 Self-audit program. As part of the QM plan, the manufacturer shall establish an independent self-audit program under the direction of the quality organization to assess the effectiveness of the manufacturer's quality assurance system, and ability to meet specification requirements. The results of these audits shall be available.

4.4.2 Change control procedures. As part of the QM plan, the manufacturer shall have a system which shall include procedures for notification of change that affects form, fit, and function, to all applicable acquiring activities.

4.5 Verifications for QML listing. Manufacturers of devices furnished as compliant to this specification shall obtain a (QML) listing from the qualifying activity (DLA Land and Maritime). The qualifying activity is as defined in 6.4.39. QA approval of the manufacturers quality management program, baseline process flows, and technology capability will result in the manufacturers receiving a QML certification and QML listing. The manufacturing processes and materials portion of the baseline flow (see 4.3) are listed on the QML. The qualifying activity shall provide procedures to obtain a QML certification and QML listing. This verification will require an on-site visit to the manufacturer's facility.

4.5.1 Verification audit. During the audit, the qualifying activity shall verify the adequacy of the manufacturer's quality management program to achieve at least the same level of quality as could be achieved by complying with Appendix A. The qualifying activity shall also verify the adequacy of the manufacturer's baselined process flow, assessing the flow's capability to produce products that can meet the generic performance verifications defined in Appendix C. The qualifying activity shall also evaluate the manufacturer's capability for holding critical processes within established limits at specified points and continuously maintaining this capability during production. Qualifying activity approval of the manufacturer's quality management system and baseline process flow results in certification, and is a mandatory precondition to QML listing. The interval between on-site reaudits shall normally be two years. However, the qualifying activity will adjust this interval based on the manufacturer's TRB reports or retention reports (as applicable), customer feedback, self-audit, and other indications of the manufacturer's maintenance of the QML system.

4.5.1.1 On-site verification. The manufacturer shall make available to the qualifying activity all data needed to support the quality management program and procedures. Qualifying activity access to manufacturing and testing facilities and operators will be required. For first time qualification, on-site verifications will include all of the following areas: The manufacturer's quality management program, design program, substrate fabrication, assembly and test processes, and facility control. Deficiencies and concerns shall be noted by the audit team and provided during the exit critique.

4.5.1.2 Certification. After verification, and upon correction of all deficiencies and concerns, the qualifying activity shall issue a certificate and letter of certification to the manufacturer.

4.5.1.3 Classes E, G, H, K, F, and L process flow audits. The qualifying activity shall also verify the adequacy of the manufacturer's baselined process flow, assessing those flows' capability to produce a product that can meet the generic performance verifications and criteria as defined in Appendices C, D, and E as applicable.

4.5.1.4 Class D process flow audit. The qualifying activity shall verify that the manufacturer plans the manufacturing of products and ensures that process control is practiced in accordance with the manufacturer's defined quality management program. The manufacturer's processes and materials will also be compared to the manufacturer's selected baseline process flow (see 4.3) for verification.

4.5.2 Technology capability verification (qualification). In order to receive a QML listing, manufacturers shall demonstrate the capability of their processes and materials to produce products that meet the appropriate performance requirements. Manufacturers of emerging technologies or advanced technologies shall also perform technology characterization as part of their technology capability verification.

4.5.2.1 Class H and K QML listing. The manufacturer shall demonstrate the capability of products built using their baseline process flow to meet the specified performance requirements with an established reliability safety margin. An established reliability safety margin is shown by testing performed to more stringent stress levels than those specified for screening and conformance inspection and periodic inspection testing. The safety margin is specified in Appendix C as a qualification test flow. This demonstration shall be performed using data, either historical data or data specifically generated by testing, performed to meet the qualification test flow of Appendix C. In order to qualify advanced or emerging technologies, the manufacturer may need to modify the qualification test flow of Appendix C.

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4.5.2.2 Class G, D, F and L QML listing. The manufacturer shall demonstrate the ability of their baseline to produce devices which will meet the performance requirements of the respective class. This demonstration shall consist of data, either historical or specifically generated to demonstrate this capability. This data shall be presented to the qualifying activity. It is the manufacturer's responsibility to provide enough information to demonstrate that their devices are capable of meeting the performance requirements.

4.5.2.3 Class E listing. Class E listing is granted upon qualification to one of the above levels. As Class E is based upon one of the above flows, users should carefully evaluate and approve exceptions taken to the Class H, K, or G baselined flow.

5. PACKAGING

5.1 Packaging For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activity within the Military Service or Defense Agency, or within the Military Service's system command. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

6. NOTES.

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. Microcircuits conforming to this specification are intended for use for Government microcircuit applications and logistic purposes. For maximum cost effectiveness while maintaining essential quality and reliability requirements, it is recommended that, for initial acquisitions for original equipment complements, the device class appropriate to the need of the application be acquired. For acquisition of spare parts for logistic support, it is recommended that, unless otherwise specified, all devices be acquired to Class H requirements.

6.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of the specification.

b. Packaging requirements (see 5.1).

c. PIN.

d. Title, number, and date of applicable device specification and identification of the originating design activity.

e. Device finishes.

f. Product assurance level (see 1.3).

g. Change notification (i.e, point of contact).

6.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the acquisition documents.

a. Requirements for failure analysis.

b. Special requirements.

c. Disposition of samples.

d. Requirement for qualification or conformance inspection (CI) and periodic inspection (PI) plan.

e. Requirements for resistance of soldering heat.

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6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturer's List, QML-38534, whether or not such manufacturers have actually been listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime-VQ, P.O. Box 3990, Columbus, Ohio 43218-3990.

6.4 Terms, definitions, methods, symbols, and abbreviations. For the purposes of this specification, the terms, definitions, methods, and symbols of MIL-STD-883, MIL-STD-750, MIL-HDBK-1331, and those contained herein apply and may be used in applicable device specifications wherever they are pertinent. The preparing activity will interpret these definitions for use wherever pertinent. To further describe a particular type of device, additional modifiers may be prefixed to the type name.

6.4.1 Acquiring activity. The organizational element of the Government which contracts for articles, supplies, or services may authorize a contractor or subcontractor to be it's agent. When this organizational element of the Government has given specific written authorization to a contractor or subcontractor to serve as agent, the agent will not have the authority to grant waivers, deviations, or exceptions to this specification unless specific written authorization to do so has also been given by the Government organization which is the preparing activity, or qualifying activity. In the absence of a specific acquiring activity, the acquiring activity will be an organization within the supplier's company that is independent of the group responsible for device design, process development or screening, or may be an independent organization outside the supplier's company.

6.4.2 Acquisition documents. Acquisition documents consist of the acquisition order or contract, device specification (e.g.SMD's, SCD's) or specifications as applicable. The preferred device document for compliant devices is the SMD.

6.4.3 Audit checklist. A form listing specific items which are to be audited.

6.4.4 Baseline index of documents. The documents which establish the baseline for a given device manufacturer in satisfying the requirements of certification in accordance with this specification.

6.4.5 Baseline process flow. The manufacturer's baseline process flow is that flow of manufacturing processes, inspection and test processes, and material entry points into the flow that defines the manufacturer's specific technology flow. This flow begins with incoming material, goes through all manufacturing processes including in-processes monitors, completed device screening, and final acceptance verification of the product. The manufacturing processes and materials portion of the baseline process flow are the portions of the baseline that are listed on the QML. The total baseline flow is certified under QML certification.

6.4.6 Burn-in lot. The burn-in lot is used for purposes of percent defective allowable (PDA) or pattern failure accountability (or both).

6.4.7 Compliant devices. Compliant devices are those that meet, without exception, the performance requirements of this specification, as well as the requirements of the device specification (e.g., SMD).

6.4.8 Compound bond. A bond placed on top of another bond, wire, ribbon, or other conductor not integral to the substrate.

6.4.9 Cpk. Cpk is a capability index that reflects process centering and variability with respect to specification requirements. The higher the Cpk number, the more capable the process.

6.4.10 Critical control parameters. Critical control parameters are parameters whose variability most affect a design, process, or material.

6.4.11 Customer compliance matrix (CCM). The CCM documents the relationship between each customer requirement for a specific product, and the method used to assure that customer requirements will be achieved. The CCM will document the correlation between alternative methods used by the manufacturer and the verification methods of Appendix C including any changes, and justification for any changes, made to the design requirements.

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6.4.12 Delta (Δ) limits. Delta limits, maximum changes in specified parameter readings which permit device acceptance on specified tests, will be based on comparison of present measurements with specified previous measurements.

NOTE: When expressed as a percentage value, they will be calculated as a proportion of previously measured values.

6.4.13 Design activity. The organization that specifies the device design parameters (e.g. layout, materials of construction, elements, and sources.)

6.4.14 Design analysis. Design analysis is an evaluation of critical performance parameters or design data to determine a design/process/material combination that guarantees compliance to a specific requirement without testing.

6.4.15 Design of experiments (DOE). DOE is a formal plan for conducting experiments which may be used to make achievement of a specific requirement less sensitive to process/material variability. Typical examples include: Taguchi, Central Composite Design, and factorial designs.

6.4.16 Design robustness. Design robustness is the insensitivity of a design to uncontrollable variation so that it does not significantly affect the product or process once it is in routine operation.

6.4.17 Electrostatic discharge sensitivity (ESDS). The level of susceptibility of devices to damage by static electricity, found by classification testing, is used as the basis for assigning an ESDS class.

6.4.18 Element. A constituent of a device that contributes directly to its operation (e.g., chip resistor, capacitor, diode, transistor, integrated circuit, surface acoustic wave (SAW), substrate, or package incorporated into a device), is an element of the device.

6.4.19 Film microcircuit. A microcircuit consisting exclusively of elements which are films formed in-situ upon or within an insulating substrate.

6.4.20 Final seal. After manufacturing operations which complete the enclosure of a device following all allowable rework so that further internal processing cannot be performed, and for the purpose of seal date code identification and (CI) and (PI) testing, the final seal date code is used.

6.4.21 Flip chip bonding. Direct attachment of a bare die face down with the surface of the die being placed in direct contact with the substrate.

6.4.22 Hybrid microcircuit. A microcircuit that contains two or more of a single type, or a combination of the following types of elements with at least one of the elements being active.

a. Film microcircuit (6.4.19).

b. Monolithic microcircuit (6.4.30).

c. Semiconductor element (6.4.42).

d. Passive chip or printed or deposited substrate elements (6.4.35).

6.4.23 Hybrid microcircuit type (device type). The term "hybrid microcircuit type" (device type) refers to a single specific device configuration. All samples of a hybrid microcircuit type are electrically and functionally interchangeable with each other; have the same electrical and environmental test limits; and use the same package, materials, piece parts, and assembly process.

6.4.24 Inspection lots. Inspection lots consist of a quantity of devices of a single device type (required for group A) or several different circuit types (allowed for groups B, C3, and D tests only) in a single package type and lead finish submitted at one time for final acceptance. All devices within each inspection lot will be finally sealed in the same period not exceeding 13 weeks.

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* 6.4.25 Inspection lot formation. Inspection lot formation is required if the inspection lot is to be formally accepted by the lot related CI and PI testing of this specification (option 2 end-of-line inspection) or method 5005 of MIL-STD-883. If in-line process verification testing (option 1 in-line inspection) is used, inspection lot formation is not required.

6.4.26 Integral substrate/package. An integral substrate/package (ISP) element is a unit where the base substrate becomes an integral part of the finished package.

6.4.27 Known good die (KGD). A bare die of the same quality and reliability level as an equivalent packaged die.

6.4.28 Microelectronics. That area of electronic technology associated with, or applied to, the realization of electronic systems from extremely small electronic parts or elements.

6.4.29 Microcircuit. A small active circuit having a high equivalent circuit element density, which is considered as a single part composed of interconnected elements on one or more substrates to perform an electronic circuit function. (This excludes printed wiring boards, circuit cards assemblies, and modules composed exclusively of discrete electronic parts mounted on a non-ceramic substrate or board.)

6.4.30 Monolithic microcircuit. A microcircuit (active) consisting exclusively of elements formed in-situ or within a single semiconductor substrate with at least one of the elements formed within the substrate.

6.4.31 Multichip module (MCM). A hybrid microcircuit that contains two or more microcircuits, each having greater than 100,000 junctions.

6.4.32 Non-continuous production. Non-continuous production occurs when devices are held by the manufacturer, with no additional assembly work performed, for more than 30 days.

6.4.33 Off-line reliability assessment. Off-line reliability assessment is the use of statistically based methods to monitor reliability data. This data may be used to control future adjustments to the design/process/material.

6.4.34 Package type. Packages which have the same case outline, configuration, materials (including bonding wire and die attach), piece parts (excluding preforms which differ only in size), and assembly processes.

6.4.35 Passive element. Planar resistors, capacitors, inductors and patterned substrates (single and multilayer), and nonplanar chip resistors, capacitors, inductors, and transformers.

6.4.36 Percent defective allowable (PDA). PDA is the maximum observed percent defective which will permit the lot to be accepted after the specified 100 percent test.

6.4.37 Periodic capability certification. Periodic capability certification is the calibration and certification of equipment or process steps for an individual parameter(s) such that it can be used as an alternative method to detection testing.

6.4.38 Production lot. A production lot consists of a device type manufactured from the same basic raw materials on the same production line, processed under the same manufacturing techniques and controls using the same type of equipment. The production lot is formed at, or prior to, device kit preparation (i.e., release to manufacturing). In addition for Class K devices, all materials will be from the same manufacturing lot or incoming inspection lot for each element. If necessary, rework requirements may be satisfied with materials from a different manufacturing lot or incoming inspection lot.

6.4.39 Qualifying activity. The qualifying activity is the organizational element of the Government that grants certification and QML status. For the purpose of this document the qualifying activity will be DLA Land and Maritime.

6.4.40 Quality function deployment (QFD). QFD is a technique for analysis of the interrelationships between different requirements. These interrelationships are evaluated in a decision making matrix developed through concurrent engineering.

6.4.41 Self-audit. The performance of periodic surveys and reviews by the device manufacturer's designated personnel to evaluate compliance to defense specifications, customer and internal requirements, and to evaluate the company's overall quality programs.

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6.4.42 Semiconductor element. Active semiconductor elements other than microcircuits (e.g. transistors, diodes, or silicon controlled rectifiers (SCRs).)

6.4.43 Similar devices. For the purpose of PI, one device type is similar to another when it meets all the following conditions:

a. Designed and manufactured identically using the same or fewer fabrication and assembly processes and materials.

b. Assembled with the same, or fewer, active and passive elements.

c. Subjected to the same screening except electrical testing.

d. Designed to generate the same, or fewer, functions (magnitude of functional attributes such as voltage, current, duty cycle, frequency, etc. may vary) using the same, or less functional, circuitry and element type (e.g., a 4-bit A/D converter is similar to a 10-bit A/D converter, but not vice versa).

6.4.44 Standard evaluation circuit (SEC). An SEC is a test coupon/device that is representative of actual product. The SEC may be actual product or may be specifically designed to evaluate a particular process. The SEC should be processed using the same processes, equipment, and type of material as the product it represents.

6.4.45 Statistical process control (SPC). SPC utilizes statistical methods to monitor parameters (i.e., process or product) in order to provide early warning of a process fluctuation or shift. Appropriate actions should be taken to maintain a state of statistical control. SPC may be used as a tool to facilitate process improvement.

6.4.46 Sub-assembly. A standalone functional device with more than one element mounted on a substrate or in a package and not already defined in element evaluation table C-I.

6.4.47 Tape automated bonding (TAB). The attachment of a bare die to a very fine pitch lead frame.

6.4.48 Technology capability. Technology reliability and performance limits, normally determined through tests known to reveal failure modes/mechanisms; and through testing of critical characteristics of the technology that are known to impact performance and reliability. Testing performed to more severe test conditions than those used for screening and final acceptance testing of the device, or test-to-failure testing, are examples of testing performed specifically to determine a technology's capability. The data may also be produced through other means for mature technologies, (e.g., production test data taken over time, design or product qualification test data accumulated for a specific program or customer.)

6.4.49 Wafer lots. Wafer lots consist of microcircuit and semiconductor wafers formed into lots at the start of wafer fabrication for homogeneous processing as a group. Each lot is assigned a unique identifier or code to provide traceability and maintain lot integrity throughout the fabrication process. Wafer lot processing as a homogeneous group is accomplished by any of the following procedures, providing process schedules and controls are sufficiently maintained, to assure identical processing in accordance with process instructions of all wafers in the lot:

a. Batch processing of all wafers in the wafer lot through the same machine process steps simultaneously.

b. Continuous or sequential processing (wafer by wafer or batch portions of wafer lot) of all wafers through the same machine or process steps.

c. Parallel processing of portions of the wafer lot through multiple machines or process stations on the same certified line, provided statistical quality control (SQC) assures and demonstrates correlation between stations and separately processed portions of the wafer lot.

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6.5 Destructive tests. All mechanical or environmental tests (other than those listed in 6.6), will be considered destructive initially, but may subsequently be considered nondestructive upon accumulation of sufficient data to indicate that the test is nondestructive. The accumulation of data from five repetitions of the specified tests on the same sample of product, without evidence of cumulative degradation or failure to pass the specified test requirements in any device in the sample, is considered sufficient evidence that the test is nondestructive. Any test specified as a 100 percent screen will be considered nondestructive for the stress level and duration or number of cycles applied as a screen. Unless otherwise specified, or subsequently determined to be otherwise, the following MIL-STD-883 test methods will be initially classified as destructive:

Internal visual and mechanical (method 2014). 1/
Bond strength (method 2011).
Solderability (except for lead finish A).
Moisture resistance.
Lead integrity (method 2004).
Salt atmosphere.
SEM inspection for metallization.
Steady state life test (accelerated).
Single Event Upset (SEE).
Neutron testing.
Autoclave
Steady-state temperature humidity bias life test (85/85)
Highly accelerated temperature and humidity stress test (HAST)
Die shear strength test.
Total dose radiation hardness test.
ESDS test.
Lid torque test.
Adhesion of lead finish.
Vibration, variable frequency.
Internal gas analysis (IGA). 2/
Pin grid package lead pull (method 2028).
Dose rate upset.
Moisture/reflow sensitivity classification
Random vibration

6.6 Nondestructive tests. Unless otherwise specified, the following tests are classified as nondestructive:

Barometric pressure.
Steady-state life (see note).
Intermittent life (see note).
Hermeticity.
External visual.
Internal visual (preseal).
Burn-in screen (see note).
Radiography.
Particle impact noise detection (PIND).
Physical dimensions.
Nondestructive bond pull test (method 2023).
Resistance to solvents.
Solderability (for lead finish A only).

NOTE: When the test temperature exceeds the maximum specified junction temperature for the device (including maximum specified for operation or test), these tests are considered destructive unless otherwise specified.

6.7 Subject term (key word) listing.

Class E
Class G
Class H
Class K
Multichip module (MCM)
Qualified Manufacturers List (QML)
Qualification
Statistical Process Control (SPC)
Technology Review Board (TRB)

1/ This inspection is nondestructive when performed at preseal visual.
2/ Test samples may be delidded/relidded in accordance with Appendix E making these devices eligible for shipment. The manufacturer will ensure that proper precautions for handling, testing, and shipping have been taken by the IGA test laboratory.

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6.8 List of acronyms.

ATT	- Authorization to test
CCM	- Customer compliance matrix
CI	- Conformance inspection
DOE	- Design of experiments
DRC	- Design rules check
ERC	- Electrical rules check
ESD	- Electrostatic discharge
ESDS	- Electrostatic discharge sensitivity
IC	- Integrated circuit
IGA	- Internal gas analysis
IR	- Insulation resistance
ISP	- Integral substrate package
KGD	- Known good die
LTPD	- Lot tolerance percent defective
MCM	- Multichip module
MIS	- Metal insulation semiconductor
PDA	- Percent defective allowable
PI	- Periodic inspection
PIND	- Particle impact noise detection
PPM	- Parts per million
QA	- Qualifying activity
QFD	- Quality function deployment
QM	- Quality management
QML	- Qualified manufacturers list
QPL	- Qualified product list
RF	- Radio frequency
RHA	- Radiation hardness assurance
SAW	- Surface acoustic wave
SCR	- Silicon controlled rectifier
SEC	- Standard evaluation circuit
SEM	- Scanning electron microscope
SEU	- Single event upset
SMD	- Standard microcircuit drawing
SPC	- Statistical process control
SQC	- Statistical quality control
TAB	- Tape automated bonding
TCR	- Temperature coefficient of resistance
TRB	- Technology review board

6.9 Change from previous issue. The margins of this specification are marked with asterisks to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations and relationship to the last previous issue.

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APPENDIX A

QUALITY MANAGEMENT PROGRAM

A.1 SCOPE

A.1.1 Scope. This appendix is intended to be used by manufacturers in developing their Quality Management (QM) Program for implementation of verification and preventative techniques to assure product quality and reliability. The QM program should demonstrate the methods used to assure conformance to the applicable performance requirements, including design, manufacturing, and verification. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. Manufacturers may demonstrate a QM system that achieves at least the same level of quality as could be achieved by complying with this appendix.

A.1.2 Technology Review Board (TRB) option. Manufacturers using this option will develop a TRB system and have it approved by the qualifying activity (QA). This option allows a manufacturer to migrate from the conventional design and construction requirements and detection tests (e.g., screening, conformance inspection and periodic inspection, and qualification) of this document to alternative prevention methods with sufficient documentation. Alternative prevention methods include statistical process control (SPC), periodic process capability certification, design analysis, design robustness, and off-line reliability assessment. The documentation will show that the alternative methods ensure product compliance to the minimum quality and reliability requirements of this specification without performing the detection tests or adhering to the specific design and construction requirements. Using this specification as a baseline, the manufacturer develops a QM program, which encompasses the entire manufacturing line being validated. This line is controlled by the TRB, which can modify, substitute, or delete detection tests as appropriate for the technology or process. Techniques such as statistical process control (SPC) and design of experiments may be employed to ascertain process capabilities. Once alternative techniques are developed, periodic assessment is required to ensure that the processes continue to meet the required capabilities. The QM program also requires a program of continuous improvement to reduce overall product cost and improve quality and reliability. A customer compliance matrix (CCM) is generated for each product as part of the conversion of customer requirements process, and documents the means by which the end-item performance requirements will be met.

A.1.3 Description of appendix A. This appendix describes a QM program to demonstrate and assure that design, manufacture, inspection, and testing of devices are adequate to ensure compliance with the applicable performance requirements and quality standards for each device manufactured. This appendix also describes an optional TRB system. When used, the TRB system will be certified by the QA.

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A.2 APPLICABLE DOCUMENTS

A.2.1 General. The documents listed in this section are specified in section A.3 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in section A.3 of this specification, whether or not they are listed.

A.2.2 Government documents.

* A.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

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APPENDIX A

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits

(Copies of this document are available online at https://quicksearch.dla.mil).

A.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN NATIONAL STANDARDS INSTITUTE (ANSI)

ANSI/NCSL Z540.3 - Calibration Laboratories and Measuring and Test Equipment - General Requirements.

(Copies of these documents are available online at https://www.ansi.org/).

INTERNATIONAL ORGANIZATION FOR STANDARDIZATION (ISO) STANDARDS

ISO 14644-1 - Cleanrooms and Associated Controlled Environments - Part 1: Classification of Air Cleanliness - First Edition.
ISO 14644-2 - Cleanrooms and Associated Controlled Environments – Part 2: Specifications for Testing and Monitoring to Prove Continued Compliance with ISO 14644-1 – First Edition.

(Copies of these documents are also available online at https://www.iso.org/iso/home.htm).

A.2.4 Order of precedence. Unless otherwise noted herein or in the contract in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 QUALITY SYSTEM REQUIREMENTS

A.3.1 Management responsibility. Management is responsible to ensure that the quality system is implemented and successful in fulfilling its goals.

A.3.2 Quality system.

A.3.2.1 QM plan. The QM plan should consist of a volume or portfolio, or series of documents, which is adequate to assure the quality of the device. This section is a guide in developing these documents. A summary of the manufacturer's approach that makes specific reference to the manufacturer's actual procedures is also a method of documenting the product assurance program plan. The documents authorizing and implementing changes should be maintained. Any difference in treatment of different product lines within a plant should be stated and explained in the QM plan, or separate QM plan's prepared for such different lines. The QM plan should contain, as a minimum, documentation covering the items detailed herein, including all TRB information when applicable.

A.3.2.1.1 Functional block organization chart. This chart should show, in functional block-diagram form, the lines of authority and responsibility (both line and staff) for origination, approval, and implementation of all aspects of the product assurance program. Names of the incumbents are not necessary in this chart.

A.3.2.1.2 Baseline process flowchart. The flow (see 4.3 herein) should identify all major documents pertaining to the inspection of materials, the production processes, the production environments, and production controls which were used. The documents will be identified by name and number. Changes approved thereafter will be treated in accordance with the approved document change control procedures in A.3.5 herein.

A.3.2.1.3 Design guidelines. Design guidelines used to design or verify the design of microcircuits intended to be submitted for acceptance inspection (see A.3.4 herein).

A.3.2.1.4 Travelers. Travelers are used to track materials and products during production and testing.

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A.3.2.1.5 Baseline index of documents. A list of the specification titles, document numbers, and revisions which make up the QML program. This is the baseline the manufacturer is certified to at the certification audit.

A.3.2.1.6 Manufacturer's self-audit. The manufacturer's self-audit program should identify key review areas, their frequency of audit, and the corrective action system to be employed when variations from approved procedures or specification requirements are identified.

A.3.2.2 Design, processing, manufacturing, and testing instructions. The manufacturer should maintain documentation and instructions covering, as a minimum, the areas identified below. Procedures should exist which will control the processes and materials which affect the quality of the devices. The following is a guideline for developing these procedures; it is the manufacturer's responsibility to develop necessary procedures to adequately control the quality of their devices. These areas will normally be addressed by the manufacturer's standard drawings, specifications, process instructions, and other established manufacturing practices.

a. Quality control operations (A.3.2).

b. Material handling (A.3.2.3).

c. Design, processing, rework, tool and materials standards, and instructions (A.3.2.3).

d. Conversion of customer requirements into manufacturer's internal instructions (A.3.3).

e. Change control of design, process, and documentation (A.3.5).

f. Inspection of incoming materials, applicable utilities, and work in-process (A.3.6).

g. Incoming, in-process, and outgoing inventory control (A.3.6.2).

h. Performance verification operations (including test methods) (A.3.10.3).

i. Tool, gauge, and test equipment maintenance and calibration (A.3.11).

j. Failure and defect analysis and data feedback (A.3.13).

k. Failure corrective action and evaluation (A.3.14.1).

l. Control of non-conforming materials (A.3.14).

m. ESD handling control program (A.3.15.1).

n. Cleanliness and atmosphere control in work areas (A.3.15.2)

o. Personnel training and testing (A.3.18)

p. Packaging

A.3.2.3 Design, processing, manufacturing equipment, and materials instructions. Procedures should address device design, processing, manufacturing equipment, and materials described in drawings, standards, specifications, or other appropriate media covering the requirements and tolerances for all aspects of design and manufacturing including equipment test and prove-in, materials acquisition and handling, design verification testing and processing steps. As a minimum, detailed instructions should exist for the following items, and be adequate to assure that quantitative controls are exercised, that tolerances or limits of control are sufficiently tight to assure a reproducible high quality product, and that process and inspection records reflect the results actually achieved:

a. Incoming materials control (e.g. substrates, packages, active and passive chips or elements, wire, and water purification).

b. Substrate fabrication operations.

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c. Die, element, or substrate attachment.

d. Interconnect (e.g., wire bonding).

e. Rework.

f. Sealing.

A.3.2.4 Quality improvement program. The manufacturer should develop and implement a program for continuous quality and reliability improvement of processes, including corrective and preventative action.

A.3.2.5 QM program (TRB option).

A.3.2.5.1 General. A QM program should be developed and implemented by the manufacturer, documented in the QM plan, and controlled by the TRB. The QM program should ensure and demonstrate compliance to the minimum performance requirements of this specification and outline a program for continuous improvement. A device manufactured under this option should, as a minimum, be equivalent in form, fit, function, quality, and reliability to a device manufactured in accordance with Appendix C.

A.3.2.5.2 Implementation. Appendix A should be used as a baseline for the QM program. From that baseline, this option may be implemented incrementally by process, or by product line. After satisfying the minimum requirements for validation, a manufacturer may implement alternative methods for addressing the requirements contained in the baselined (Appendix C) flow while performing detection testing in accordance with Appendix C on the remainder of the processes. The minimum requirements for the QM program which should be reviewed during validation are as follows:

a. A TRB.

b. A QM plan.

c. Process/material confirmation and capability achievement procedures including technology qualification test flows.

A.3.2.5.3 TRB. The manufacturer should establish a TRB and develop the necessary procedures to govern its' operation. The manufacturer will be responsible for ensuring that the actions of the TRB result in products that meet all customer and performance requirements. As a minimum, these operating procedures should address the following:

a. Record retention.

b. Minimum organizational membership.

c. TRB charter.

d. Responsibilities.

e. System for recovery of data used in TRB decisions.

f. TRB meeting structure.

g. Decision making/approval procedures.

h. Distribution of TRB minutes.

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A.3.2.5.3.1 TRB organizational structure. The following functions, as a minimum, should be represented on the manufacturer's TRB: Design, material procurement, assembly, test, reliability, and quality assurance. Other personnel with decision making responsibilities affecting the product, its processes, or its production facility should participate as required. The manufacturer should identify those organizations that shall be represented on the TRB. A responsible technical representative within each of these organizations should be identified to the qualifying activity.

A.3.2.5.3.2 TRB responsibilities. The TRB should oversee the manufacturer's qualified line, including the processes and materials that continue to be controlled under Appendix C. The TRB should be responsible for the following:

a. Developing, monitoring, maintaining and controlling the QM program and QM plan, and all supporting documents and data.

b. Managing QM plan implementation.

c. Monitoring and controlling the self audit program.

d. Managing and maintaining the quality improvement programs.

e. Overseeing the process/material confirmation and change control activities.

f. Overseeing the initial process/materials certification/qualification and subsequent maintenance thereof.

g. Reviewing and analyzing data (e.g., Cpk data, defect data, rate of assembly failures, rate of failure returns, and failure analysis results) and taking appropriate action to improve processes. When performance or reliability of shipped microcircuits is called into question, the TRB should provide quick evaluation, appropriate corrective action, and prompt notification of the problem to the qualifying activity.

h. Maintaining records of conditions found and actions taken.

i. Reporting status of the QM program to the qualifying activity.

j. Approving alternative methods that modify, substitute, or delete existing methods (e.g., inspection, testing, screening, CI and PI, or design/construction procedures of this specification).

A.3.2.5.4 Alternative method correlation, confirmation, and implementation procedures. This is the approach by which inspection/testing/screening/CI and PI or design/construction requirements within this specification should be modified, substituted, or deleted. The manufacturer should develop methods for confirmation and maintenance of process and material capability and for verification of design capability under this option. Test methods and design/construction requirements of this specification are intended to address worst case application environments for military product. Any alternate method used in lieu of testing, screening, or design/construction requirements should be approved by the manufacturer's TRB and should document the specific areas of correlation between the alternative method and the specification requirement it replaces (i.e., how it meets the specific application environments of this specification) or if the requirement does not apply to a particular technology (see 3.9.1). Alternative methods may be used by non-TRB companies with qualifying activity approval.

A.3.2.5.4.1 Correlation, confirmation, and implementation. The following is a typical flow.

a. Identify candidate requirements of this specification for alternative method.

b. Using data, identify any correlations between the candidate requirement and potential alternative method(s).

c. Where correlations exist, develop and document alternative method(s).

d. Accumulate data off-line to confirm the capability of the alternative method(s) to assure meeting the requirement.

e. Submit alternative method(s) for TRB approval.

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f. Implement the alternative method(s) as directed by the TRB.

NOTE: If an alternative method is determined to no longer assure meeting the requirements of this specification, the product should be inspected/screened/tested in accordance with the previous TRB approved baseline, until the required capability is achieved.

A.3.2.5.4.2 Alternative methods. For each candidate process under this option, the manufacturer should specify and implement alternative methods that should be used to maintain each process/material capability such that it continues to meet the minimum performance requirements of this specification. Examples of alternative methods are design analysis, design of experiment (DOE), off-line reliability assessment, periodic capability certification, SPC, embedded machine controls, manufacturer derived test methods, and automated methods with feedback controls.

A.3.2.5.4.2.1 Standard evaluation circuits (SEC). A manufacturer may utilize SEC's to evaluate the capability of alternative methods and monitor product performance. The SEC design should be approved by the TRB and controlled through the manufacturer's documentation system. SEC documentation should include construction, dimensions, intended application (i.e., the processes it evaluates), and minimum acceptable limits (e.g., mechanical or electrical values).

A.3.2.5.4.2.2 Periodic assessment of alternative methods. Alternative methods should be periodically assessed, as necessary (determined and documented by the TRB), to assure their continued effectiveness. This periodic assessment is a tool for the TRB to aid in monitoring and maintaining product quality. Methods for periodic assessment may include stress-to-failure tests, failure mode analysis, or analytic prediction modeling. If an alternative method is determined to no longer meet the initial requirement (i.e., Appendix C), the manufacturer should implement the appropriate previous TRB approved baselined inspection/screening/testing/step.

A.3.2.5.5 TRB records. Records of the TRB's membership, deliberations, and decisions should be maintained; dissenting opinions should be recorded. As a minimum, TRB minutes and associated data should be maintained for 5 years.

A.3.3 Conversion of customer requirements. The manufacturer should develop a system by which customer requirements and all requirements of this specification, are converted into working instructions. The results of this review, including alternate methods, shall be documented and made available to the customer upon request. As part of the conversion of customer requirements process for TRB companies, the manufacturer should generate a Customer compliance matrix (CCM) for each product that documents the means by which the end-item quality, reliability, and customer/specification requirements should be met and the next level assembly environment should be considered. Required process capabilities and specific internal documents used by the manufacturer to control, monitor, or assess processes and materials should be specified in the CCM. The CCM should be approved by the TRB or procuring activity when specified by contract. The CCM should be kept current.

A.3.4 Design requirements. The manufacturer should develop an approach for device design when applicable. The design approach should include the following:

a. Design guidelines/handbook. The design guidelines/handbook should define the manufacturer's qualified processes and materials as they relate to the design including the interactions between the application environment and affected materials/processes. Any design requirement not in accordance with this specification should be recorded. These guidelines should form the basis for all designs to be manufactured under the QM program.

b. Design models/procedures for worst case temperature and electrical extremes.

c. Rules check procedures, covering the following areas, as applicable:

(1) Design rules check (DRC) - geometric and physical.

(2) Electrical rules check (ERC) - shorts and connectivity.

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(3) Reliability rules - Electromigration and current density, IR drops, latchup, single event upset (SEU), hot electrons, ESD, burn-out, or backgating, as applicable.

(4) RHA rules - applicable radiation environments.

d. Thermal design verification procedures.

e. Reliability design verification procedures. Worst case circuit design.

f. Package design performance verification procedures.

g. Feedback loop from design/material/process development activities into design guidelines.

h. Next level assembly environment (e.g. hand solder device or wave solder device to the next level assembly).

A.3.4.1 Changes in design, materials, or processing. Records should document the change, the date the change is made, traceability of the first change through processing and testing, and justification for the change.

A.3.5 Change control. Procedures should address the methods and procedures for implementation and control of changes in device design, processing, and documentation; and for making change information available when applicable. This includes changes made for cost reduction and continuous improvement. The manufacturer should assure that the correct revisions of all documents are available to the appropriate people.

A.3.5.1 Configuration control. Changes are categorized into three classifications.

Class	Description
I	Major changes
II	Minor changes
III	Editorial changes

All changes in design, substitution of materials or processes, or modifications to baselined documentation (i.e., all class I, II, and III changes) for any hybrid microcircuit should be processed in accordance with established change control procedures.

a. Class I: Class I changes are those changes that may affect the performance, quality, reliability, radiation (when specified), or interchangeability of the product (see Table E-I of Appendix E for representative examples of major changes). Acquiring activity approval shall be required if specified by contract.

b. Class II: Class II changes are all changes except class I and class III changes (e.g., conformance to the performance specification revision, vendor metallization mask change, or package height change within the envelope tolerances of the detail drawing.). Control procedures, records, and rationale for the changes should be kept available for review.

c. Class III: Class III, editorial changes, are those changes to documentation necessary to ensure the understanding and execution of the affected document (e.g., format changes, spelling, or word identity). Change documentation history for class III type changes should be kept available for on-site review.

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A.3.6 Control and acceptance of incoming materials.

A.3.6.1 Supplier control program. The capability of supplied material may be validated through a supplier certification system. This system selects and monitors suppliers in order to guarantee that the supplied material should meet and maintain required capability levels (e.g., Cpk, ppm). Supplier certification is granted based on consistent proof that their product conforms to the specification requirements, through implementation of SPC and quality control systems analogous to those herein. Conventional element evaluation is not required when the elements are purchased from certified suppliers. Material may be procured from vendors who are not certified; such material should be evaluated in accordance with Appendix C of this specification or alternative methods approved by the TRB or the QA. The following are the minimum documentation requirements for each supplier controlled under this program:

a. A description of the vendor quality assurance plan with status update reports as required by the TRB or QA.

b. A description of the procedure used by the vendor for notification of changes in materials or processes.

c. A quality assurance procedure that can be performed by either the vendor or the manufacturer, or a combination of the two.

A.3.6.2 Incoming, in-process, and outgoing inventory control. Procedures should address methods and procedures which are used to control storage and handling of incoming materials, work in-process, and warehoused and outgoing product in order to achieve such factors as age control of limited-life materials; and prevent inadvertent mixing of conforming and nonconforming materials, work, or finished product. Each area should maintain identity of work in process.

A.3.7 Customer supplied material. A system should be in place to track and control all customer supplied material.

A.3.8 Traceability.

A.3.8.1 Material and element traceability. Traceability for each device, all adhesives and coatings shall be traceable to a material production lot, inspection lot, or other specified grouping. All elements and materials used for Classes G, H, K, F, and L will be traceable to the element manufacturer's production lot. Traceability for die for Class G, H, K, F, L and parts identified as radiation hardened, is to the wafer lot. For Class K and L traceability shall be from the device serial number to specific wafer lot.

A.3.8.2 Process/test traceability. Each device, or each group of devices, which have been fabricated as a common batch, will be identifiable through means of production travelers or similar documentation such that the complete manufacturing history, including rework, will be recorded. The records should include, as a minimum, the performance date of all identified production process steps, the specification, number of production process steps, and the identification of the operator performing the process steps. The records will be retained in accordance with A.3.16.

A.3.8.3 Production lot traceability. The manufacturer will maintain production lot traceability. In addition for Class K devices, all materials will be from the same manufacturing lot or incoming inspection lot for each element. If necessary, rework requirements may be satisfied with materials from a different manufacturing lot or incoming inspection lot, and shall be traceable to the device serial number.

A.3.8.4 Country of manufacture. The manufacturer shall maintain traceability to the location(s) where the baselined assembly processes were performed.

A.3.8.5 Production lot identification. Records should identify when each production or inspection lot was processed through each area. These records should identify, for each production or performance verification lot (as applicable) of finished product, test/inspections performed and results, device serial numbers, date of completion, lot identification, device specification, lot disposition, and the number of devices at seal, shipped, and stocked.

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A.3.9 Process control. The manufacturer should define all processes and methods used to assure the capability and consistency of the processes. As a minimum, all critical process parameters should be defined. The manufacturer should define process monitors as appropriate.

A.3.9.1 Process and materials controls. Records should cover the implementation of tools such as control charts (e.g., X and R charts) or other means of indication of the degree of control achieved at the points in the material, utility, and assembly process flow documented in the manufacturing instructions. Records should also indicate the action taken when each out-of-control condition is observed, and the disposition of product processed during the period of out-of-control operation.

A.3.10. Inspection and testing

A.3.10.1 Inspection operations. Procedures should address inspection operations specifying type of inspection, sampling and test procedures, acceptance and rejection criteria, and frequency of use.

A.3.10.2 Quality control operations. Procedures should address quality control operations specifying the type, procedures, rating criteria, action criteria, records, and frequency of use.

A.3.10.3 Performance verification operations. Procedures should address performance verification operations specifying the type, procedures, equipment, judgment, and action criteria, records, and frequency of use.

A.3.10.4 Inspection operations. Records of inspection operations should cover the tests or inspections made, the materials group (e.g. lot, batch.) inspected, the controlling documentation, the date of completion of inspection, the amount of material tested, and acceptance, rejection, or other final disposition of the material.

A.3.11 Tool, gauge, and test equipment maintenance and calibration. Procedures should address the maintenance and calibration procedures, and the frequency of scheduled actions, for tools, gauges, and test equipment in accordance with the requirements of ANSI/NCSL Z540.3 or equivalent. For electrical test see MIL-STD-883 electrical test equipment accuracy requirements.

A.3.11.1 Equipment calibrations. Records should cover the scheduled calibration intervals for each equipment item, the dates of completion of actual calibration, identification of the group performing the calibration, and certification of the compliance of the equipment with documented requirements after calibration, in accordance with ANSI/NCSL Z540.3 or equivalent.

A.3.12 Examples of assembly and verification travelers. Screening and conformance inspection verification travelers should be maintained on a current basis. When in-line inspections replace end-of-line verifications (i.e., alternate group A or B) the traveler should include evidence of required inspections. The traveler should include information necessary to adequately detail the steps utilized in the production and testing of the devices, including all manufacturer imposed tests. As a guide, the following information should be available:

a. Name or title of operation and specification number of each process or test.

b. Identify PIN, date code, and manufacturer internal lot identification number.

c. Date of test and operator identification.

d. Calibration control number or equipment identification of all major equipment components used for test.

e. Quantity tested and rejected for each process or test and actual quantity tested, if sampled.

f. Serial numbers of passing and failing devices, when applicable.

g. Time in and out of process, or test, if critical to process, or test, results (i.e., burn-in and 96-hour window).

h. Specific major conditions of test that are verifiable by operator including times, temperature, and rpm.

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i. The percent defective calculated and the pattern failure analysis for burn-in.

j. Burn-in or life test board serial number or test circuit identification number and revision.

k. All required variables data except for electrical tests (use attachments if applicable).

l. For electrical tests, test program number and revision, and identify when variables data is required.

A.3.13 Failure and defect analysis and data feedback. Procedures should address methods for identification, handling, analysis, and disposition of failed or defective devices.

A.3.13.1 Procedure in case of test equipment failure or operator error. Whenever a device is believed to have failed as a result of faulty test equipment or operator error, the failure will be entered in the test record which will be retained for review along with a complete explanation verifying why the failure is believed to be invalid.

NOTE: ESD failures will be counted as rejects and not attributed to equipment or operator error for screening, group A, and end-point electrical tests of screening, CI and PI, and qualification and method 5005 of MIL-STD-883.

A.3.13.1.1 Procedure for sample tests. When it has been established that a failure is due to test equipment failure or operator error, and it has been established that the sample device has been damaged or degraded, a replacement device from the same inspection lot may be added to the sample. The replacement device will be subjected to all tests to which the discarded device was subjected prior to its failure and to any remaining specified tests to which the discarded device was not subjected prior to its failure. The manufacturer, at their own risk, has the option of replacing the failed device and continuing with the tests before the validity of the test equipment failure or operator error has been established.

A.3.13.1.2 Procedure for screening tests. When it has been established that a lot failure during screening test is due to operator or equipment error, and it has been established that the remaining product has not been damaged or degraded, the lot, or surviving portion of the lot, may be resubmitted to the corrected screening test in which the error occurred. Failures verified as having been caused by test equipment failure or operator error will not be counted in the PDA calculation (when applicable).

A.3.13.2 Failure and corrective action reports. When the procedures of A.3.13.1.1 and A.3.13.1.2 are used in continuing sample tests or resubmitting lots for screening tests, the manufacturer will document the results of their failure investigations and corrective actions.

A.3.14 Failure analysis and corrective action program. The manufacturer should develop the procedures for testing, analyzing, and taking corrective actions on failed parts from all stages of manufacturing, including field returns. The program should include the specific steps to be followed in order to correct any process that is out of control. The manufacturer should also develop procedures for corrective actions to nonconformities other than failed parts.

A.3.14.1 Reports and analyses of defective devices and failures. Records of defective devices should cover the source from which each device was received, the test or operation during which failure occurred or defects were observed, and prior testing or screening history of the device, the date of receipt, and the disposition of the device. Records of failure and defect analyses should cover the nature of the reported failure or defect (failure or defect mode), verification of the failure or defect, the nature of any device discrepancies which were found during analysis (failure or defect mechanism), assignment of the failure activating cause if possible, the date of completion of the analysis, identification of the group performing the analysis, disposition of the device after analysis, and the distribution of the record. The record should also address the relationship of observed failure or defect modes in related lots or devices and, where applicable, corrective action taken as a result of the findings.

A.3.15 Atmospheric control and handling.

A.3.15.1 ESD handling control program. Procedures should address the ESD handling control program documentation. This includes methods, equipment and materials, training, packaging, handling, and procedures for handling ESD sensitive devices.

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A.3.15.2 Cleanliness and atmosphere control in work areas. Procedures should address instructions for cleanliness and atmosphere control in each work area in which unsealed devices, or parts thereof, are processed or assembled. Controlled work areas should be established in accordance with ISO 14644-1 or equivalent. Airborne particulate class limits shall be as defined by ISO 14644-1. A method for class verification and reverification shall be documented and implemented. ISO 14644-2 may be used for a guide. Action and absolute control limits (at which point work stops until corrective action is completed) based on historical data and criticalness of the process in each particular area, should be established. A method for the identification and control of foreign material, equivalent to or better than the foreign material control program described in method 2017 of MIL-STD-883, should be employed.

A.3.16 Control of quality records.

A.3.16.1 Records to be maintained. Records shall be legible and maintained which will adequately describe the processes, materials, inspections, and tests which affect the quality of the device for appropriate amounts of time such that quality concerns and customers are properly supported (e.g. method 5011 of MIL-STD-883 test records, Group C, QML, package evaluation testing, and alternate methods). The records pertaining to production processes, incoming, and in-process inspections should be retained for a minimum of 3 years (7 years for Class K) and those pertaining to performance verification retained for a minimum of 5 years (7 years for Class K) after performance of the inspections. Records pertaining to alternate methods, group C testing, QML, package evaluation, and method 5011 testing shall be retained for 5 years (7 years for Class K) after the process or materials affected have been removed from the qualified flow.

A.3.16.1.1 Computerized records. Computerized records are optional provided they clearly and objectively indicate that all requirements of this document have been met. The computerized records for traceability, screening, and conformance inspection should be readily accessible and available to Government personnel for review and an appropriate electronic or hard copy provided to the qualifying activity as required. Computerized records, when used, should be maintained with controls sufficient to easily provide the necessary information and traceability, including identification of individual and time of input. The integrity of the system and the data should be maintained.

A.3.16.2 Altered records. Altered records should identify all information necessary to maintain proper traceability and the integrity of the original data and justification for the change.

A.3.17 Internal quality audits.

A.3.17.1 Self-audit requirements. The manufacturer should have a self-audit program which assists in determining what areas need improvement. The self-audit program should be approved, monitored, and controlled by the manufacturer's TRB, when applicable.

A.3.17.1.1 Self-audit representatives. The designated auditors should be independent from the area being audited. If the use of an independent auditor is not practical; then, as a minimum, another individual should be assigned to participate in the audit or review the results with the auditor from the area. The auditors should be trained in the area to be audited, in the applicable defense specification requirement, and provided with an appropriate checklist for annotating deficiencies. Prior to the audit, the assigned auditor should review the previous audit checklist and deficiencies to assure corrective actions have been implemented and are sufficient to correct the deficiencies.

A.3.17.1.2 Audit deficiencies. All audit deficiencies should be documented on the appropriate checklist and a copy submitted to the department head for corrective action. All corrective actions should be agreed to by the quality organization or review board.

A.3.17.1.3 Audit follow-up. All audit reports should be filed and maintained. A procedure should be established to follow up on all audit deficiencies to assure that the corrective actions have been implemented in a timely manner. The system (e.g., management review) should also review the acceptability and timeliness of all corrective actions and determine if any deficiencies have repeated since the last required self-audit. If any deficiencies have occurred two or more times in the predetermined time period, additional corrective actions should be taken to assure immediate correction of the problem including notification of applicable organizations.

A.3.17.1.4 Audit schedules. The original audit frequency is established by the manufacturer normally not to exceed 1 year for each area.

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A.3.17.1.5 Self-audit report. The manufacturer keeps the self-audit report on file for the established amount of time prescribed by the manufacturer's record retention requirements, and makes the self-audit report, deficiencies, and corrective actions taken available for review by the qualifying activity.

A.3.17.1.6 Self-audit areas. The self-audit should be performed on all areas which directly affect the quality of the device.

A.3.17.1.7 Self-audit checklist. The audit checklist should be approved and maintained under document control. The checklist is intended to assure that the quality assurance system is adequate and followed by all personnel in each area.

A.3.18 Personnel training and testing. The procedures should address the training and testing practices employed to establish, evaluate, and maintain the skills of personnel engaged in reliability critical work including the form, content, and frequency of use.

A.3.18.1 Personnel training and testing. Records should cover the nature of training or testing given (e.g., when it was given, how long it lasted, and who was trained and tested). An effective training program should address various types of training (e.g. formal or on-the-job.) identification of critical areas, evaluation and re-evaluation, and the use of trained personnel.

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APPENDIX B

Appendix B has been combined with the previous appendix. The appendix letter will be held for future use.

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APPENDIX B

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APPENDIX C

GENERIC PERFORMANCE VERIFICATIONS FOR HYBRID
AND MULTICHIP MODULE TECHNOLOGIES

C.1 SCOPE

C.1.1 Scope. This appendix is intended to be used by manufacturers in developing their baseline flow of processes, tests, and inspections. This appendix provides an acceptable standard which may be used to verify the performance requirements of compliant devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. Manufacturers may demonstrate a test and inspection system that achieves at least the same level of quality as could be achieved by complying with this appendix. These standards may be used as is, or as modified in accordance with 3.9.1. The test flow presented in this appendix may not be appropriate for all technologies. For these types of devices this appendix should be used as a starting point in developing an appropriate test flow.

C.1.2 Description of Appendix C. This appendix contains the standard testing and inspection approach to verifying the performance requirements of this specification. This approach is a five-step approach consisting of an element evaluation program, a process control program, a screening program, a conformance inspection (CI) and periodic inspection (PI) program, and a qualification program.

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C.2 APPLICABLE DOCUMENTS

C.2.1 General. The documents listed in this section are specified in sections C.3, C.4, C.5, C.6, or C.7 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections C.3, C.4, C.5, C.6, or C.7 of this specification, whether or not they are listed.

C.2.2 Government documents.

* C.2.2.1 Specifications, standards, and handbooks. The following specifications, standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-19500 - Semiconductor Devices, General Specification for.
MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Test Method Standard for Electronic and Electrical Component Parts.
MIL-STD-750 - Test Method Standard for Semiconductor Devices.
MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-981 - Design, Manufacturing and Quality Standards for Custom Electromagnetic Devices for Space Applications.

(Copies of these documents are available online at https://quicksearch.dla.mil)

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* C.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP142 – Obtaining and Accepting Material for Use in Hybrid/MCM Products.
JESD213 – Standard Test Method Utilizing X-RAY Fluorescence (XRF for Analyzing Component Finishes and Solder Alloys to Determine Tin (Sn) – Lead (Pb) Content.

(Copies of these documents are available online at https://www.jedec.org/)

ELECTRONIC COMPONENTS INDUSTRY ASSOCIATION (ECIA)

ECIA EIA-469 – Standard Test Method for Destructive Physical Analysis (DPA) of Ceramic Monolithic Capacitors

(Copies of this document are available online at https://www.ecianow.org)

C.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

C.3 ELEMENT EVALUATION

* C.3.1 Description of element evaluation. Element evaluation is used to verify that procured materials and devices meet their specified characteristics and are adequate to perform as intended under the conditions experienced in the application. Element characteristics required to assure device performance and assembly process capability shall be identified. These evaluations should be completed on all materials prior to their use in production devices (see table C-I). These evaluations may be modified by the manufacturer based on:

a. Element quality and reliability history.

b. Device quality and reliability history.

c. Supplier history.

d. Supplier/manufacturer relationship.

e. Possible impact of element evaluation failure after assembly.

NOTE: Elements used in compliant hybrid microcircuits with element evaluation successfully completed prior to the implementation date of this specification are permitted and shall follow the element evaluation requirements in MIL-PRF-38534 at the time element evaluation was initiated.

Acquiring activities may request as part of a purchase order that all internal raw elements of a specific hybrid under contract be fully compliant to the latest element evaluation requirements of this specification.

Elements may be assembled into the device prior to final element lot acceptance. The hybrid manufacturer will have a system, approved by the qualifying activity, to maintain traceability of all such elements for the purpose of element containment. This system should be employed only when a work stoppage situation is encountered, schedule is affected, or when a lengthy test is required. For Class K devices, elements may be assembled into the device only with acquiring activity approval. For all classes, element evaluation will be successfully completed prior to device shipment.

C.3.1.1 Element evaluation guidance. JEP142 provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in hybrid/MCM products. JEP 142 is not an alternate element evaluation and shall not supersede any element evaluation requirements of Class H and Class K of this document.

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C.3.2 General.

C.3.2.1 Sequence of testing. Subgroups within a group (table) of tests may be performed in any sequence, but individual tests within a subgroup will be performed in the sequence indicated.

C.3.2.2 Sample selection. Samples will be randomly drawn from inspection lots or in-line production samples as applicable. The sample size columns in the evaluation tables give minimum quantities to be evaluated with applicable accept number enclosed in parentheses.

C.3.2.3 Class requirements. Class K and Class H element evaluation requirements are identified by X's in the appropriate column locations of evaluation tables.

C.3.2.4 Location of element evaluation. Element evaluation may be performed at the element supplier facility (or other facility approved by the device manufacturer) or at the device manufacturing facility.

C.3.2.5 Characteristics. Characteristics to be verified will be those necessary for compatibility with the element acquisition documents and assembly procedures and at least those which cannot be verified after assembly, but could cause functional failure.

C.3.2.6 Protection from electrostatic discharge. Suitable handling precautions and grounding procedures will be taken to protect ESDS elements from accidental damage.

C.3.2.7 Electrical test specifications. Electrical test parameters, values, limits (including deltas when applicable), and conditions will be specified in the element acquisition documents.

* TABLE C-I. Element evaluation summary.

Element	Paragraph	Table or MIL-STD-883 method
Microcircuit dice	C.3.3	Table C-II
Semiconductor dice	C.3.3	Table C-II-1
Wire Bondable and Surface Mount Resistors.	C.3.4	Table C-III
Capacitors, Ceramic	C.3.4	Table C III-1
Chip Capacitors, Solid Tantalum	C.3.4	Table C III-2
Capacitors, MOS – NMOS	C.3.4	Table C III-3
Coils, Transformers	C.3.4	Table C III-4
Surface acoustic wave (SAW) elements	C.3.5	Table C-IV
Alternate evaluation	C.3.6	N/A
Substrate evaluation	C.3.7	Table C-V
Package evaluation	C.3.8	Table C-VI
Integral substrate/package evaluation	C.3.9	Table C-VII
Polymeric material evaluation	C.3.10	Method 5011
Sub-assembly evaluation	C.3.11	Table C-VII-1

* C.3.3 Microcircuit and semiconductor dice. Microcircuit and semiconductor dice from each wafer lot will be evaluated in accordance with tables C-II, C-II-1 and C.3.3.1 through C.3.3.6.1. For Class H devices, element evaluation testing is not required for JANHC or JANKC discrete semiconductor MIL-PRF-19500 qualified die or for MIL-PRF-38535 Class Q or Class V qualified die that is supplied on a SMD and listed on the applicable QML. For Class K devices, element evaluation is not required for JANKC discrete semiconductor MIL-PRF-19500 qualified die or for MIL-PRF-38535, Class V qualified die that is supplied on a SMD and listed on the applicable QML.

C.3.3.1 Subgroup 1, 100 percent electrical test of dice. Each die will be electrically tested, which may be done at the wafer level provided all failures are identified and removed from the lot when the dice are separated from the wafer. When wafer/die level testing requirements are not specified in the procurement documents, the manufacturer/die supplier will choose the parameters, conditions, and limits to assure compliance with the electrical characteristics.

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C.3.3.2 Subgroup 2, 100 percent visual inspection of dice. Each die will be visually inspected to ensure conformance with the applicable die related requirements of method 2010 of MIL-STD-883; methods 2069, 2070, 2072, and 2073 of MIL-STD-750; and the element acquisition documents.

C.3.3.3 Sample evaluation of assembled dice.

* C.3.3.3.1 Test samples. A sample of dice from each wafer lot will be evaluated in accordance with tables C-II and C-II-1, subgroups 3 through 6 as applicable, and C.3.3.3.2 through C.3.3.6.1.

* C.3.3.3.2 Test sample preparation. All test samples being assembled by the hybrid manufacturer shall use the same methods, materials, and conditions (such as die attach and wirebond type) used during normal production of the device. If the test samples are not being prepared by the hybrid manufacturer, all test samples shall be assembled using the same or similar assembly methods, materials, and conditions the device will see during normal production.

C.3.3.4 Subgroups 3 and 4.

C.3.3.4.1 Sample size. The Class H sample will consist of at least ten die from each wafer lot. The Class K sample will consist of three die from each wafer and a total of at least ten die from each wafer lot. If one wafer is evaluated, then ten die shall be tested. If ten wafers are evaluated, then 30 die (three from each wafer) shall be tested.

C.3.3.4.2 Internal visual. Each sample will be visually inspected to ensure conformance with the applicable requirements of method 2010 of MIL-STD-883; methods 2069, 2070, 2072, and 2073 of MIL-STD-750; and the element acquisition documents.

C.3.3.4.3 Electrical test. For interim, post burn-in, and final electrical tests, the minimum requirements for microcircuits and semiconductor dice will include static tests at each of the following:

a. +25°C.

b. Maximum rated operating temperature.

c. Minimum rated operating temperature.

C.3.3.5 Subgroup 5.

C.3.3.5.1 Sample size. From each wafer lot, a sample of at least five die requiring ten bond wires minimum will be selected.

C.3.3.5.2 Wire bond strength testing. For wire bond strength testing:

a. A minimum of ten wires consisting of die-to-package, die-to-die, or die-to-substrate bonds will be destructively pull tested. An equal number of bonds will be tested on each sample die.

b. For beam lead and flip-chips, five devices shall be tested.

c. The element metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample shall be selected in accordance with C.3.3.5.1 and subjected to subgroup 5 evaluation. If the second sample contains no failures, the bonding test results are acceptable and the lot of dice is acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of dice shall be rejected.

d. The rejected wafer lot may be resubmitted to subgroup 5 evaluation if the failure was not due to defective die metallization.

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C.3.3.6 Subgroup 6, scanning electron microscope (SEM).

C.3.3.6.1 Sample selection and reject criteria. Microcircuit sample selection and reject criteria shall be in accordance with method 2018 of MIL-STD-883 on a homogeneous lot. Discrete semiconductor devices with oxide steps or expanded contacts shall be tested with the sample selection and reject criteria in accordance with method 2077 of MIL-STD-750. In cases when dice are very large and comprise a large area of the wafer, the qualifying activity may approve other alternate sample selection plans.

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TABLE C-II. Microcircuit dice evaluation requirements.

Subgroup	Class		Test	Specification or Standard	Method	Condition	Comments	Quantity (accept number)	Reference paragraph MIL-PRF-38534
	K	H							
1	X	X	Element Electrical	Per Acquisition Document			25°C	100%	C.3.3.1
2		X	Element Visual	MIL-STD-883	2010	B		100%	C.3.3.2
	X		Element Visual	MIL-STD-883	2010	A			
3		X	Internal Visual	MIL-STD-883	2010	B		10(0)	C.3.3.3
	X		Internal Visual	MIL-STD-883	2010	A			C.3.3.4.2
4	X		Initial Electrical	Per Acquisition Document			25°C Record Data	10(0)	
	X		Temperature Cycle	MIL-STD-883	1010	C	20 Cycles		C.3.3.3
	X		Mechanical Stress 1/	MIL-STD-883 - Constant Acceleration	2001	A	Y1 Direction		
				MIL-STD-883 - Mechanical Shock	2002	B	Y1 Direction		
	X		Interim Electrical	Per Acquisition Document			25°C Record Data		C.3.3.4.3
	X		Burn-In 2/	MIL-STD-883	1015		240hrs Min. at Tc or Ta = 125ºC Min.		
	X		Post-BI Electrical 3/	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
	X		Steady State Life 2/	MIL-STD-883	1005		1000hrs at Tc or Ta =125°C Min. or 500hrs at Tc=150°C Min.		
	X	X	Final Electrical 3/	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
5	X	X	Wirebond Evaluation 4/	MIL-STD-883	2011		Bake for 1 hour minimum @ +300ºC (Bimetallic bonds only)	10(0) or 20(1) wires	C.3.3.3 C.3.3.5
6	X		SEM 5/	MIL-STD-883	2018			See 5/	C.3.3.6

See footnotes at end of table.

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* TABLE C-II. Microcircuit dice evaluation requirements - Continued.

1/ Either test method is applicable.
2/ High power devices may be tested at Max Tj when Ta/Tc would cause Tj to exceed max operating temperature.
3/ Perform Delta Limit Calculation results against the previous electrical test performed when required by the acquisition document.
4/ Bond wires must be selected to accurately reflect the wire bond system used on the hybrid.
5/ The quantity accept (reject) requirements specified herein for element evaluation supersede the sample size and selection requirements of method 2018 of MIL-STD-883. If the die are from a known homogeneous single wafer, then the sample size shall be 4 devices randomly selected from the wafer. If the die are from a non-homogeneous wafer lot (traceability is unknown or no objective evidence is available for verification), then the sample size shall be 8 devices randomly selected from the population. If the die are from known homogeneous multiple (two or more) wafers, then the sample size shall be 4 devices randomly selected from each of two wafers in the lot, 8 devices total. If any wafer from the lot fails, all remaining wafers in the lot must be tested (4 devices randomly selected from each wafer) to be verified as acceptable for use.

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TABLE C-II-1. Semiconductor dice evaluation requirements.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
1	X	X	Element Electrical	X	X	X	X	X	X	Per Acquisition Document			25°C	100%	C.3.3.1
2	X	X	Element Visual					X		MIL-STD-750	2069			100%	C.3.3.2
	X	X		X							2070				
	X	X		X	X				X		2072				
	X	X				X	X				2073				
3	X	X	Internal Visual					X		MIL-STD-750	2069			10(0)	C.3.3.3
	X	X		X							2070				C.3.3.4.2
	X	X		X	X				X		2072				
	X	X				X	X				2073				
4	X		Initial Electrical 1/	X	X	X	X	X	X	Per Acquisition Document			25°C Record Data	10(0)	
	X		Temperature Cycle 2/	X	X	X	X	X	X	MIL-STD-883	1010	C	20 Cycles		C.3.3.3
	X			X	X	X	X	X	X	MIL-STD-750	1051	C	20 Cycles		
	X		Surge			X				MIL-STD-750	4066	B			
	X						X					A			

See footnotes at end of table.

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TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode – Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
4	X		Mechanical Stress 2/	X	X	X	X	X	X	MIL-STD-883 - Constant Acceleration	2001	A	Y1 Direction 5000g	10(0)	
										MIL-STD-750 - Constant Acceleration	2006				
	X			X	X	X	X	X	X	MIL-STD-883 - Mechanical Shock	2002	B	Y1 Direction		
										MIL-STD-750 - Mechanical Shock	2016		Y1 Direction 1500g		
	X		Interim Electrical 1/	X	X	X	X	X		Per Acquisition Document			25°C Record Data		C.3.3.4.3
	X		High Temperature Reverse Bias (HTRB) 3/	X	X					MIL-STD-750	1039	A	80% Min. of rated VCB (bipolar), as applicable.		C.3.3.3
	X							X		MIL-STD-750 - Burn-in (Power MOSFET) MIL-STD-750 - Gate Bias (IGBT)	1042	B	80% Min. of rated VGS.		
	X					X	X			MIL-STD-750 - Burn-in (Power) MIL-STD-750 - Reverse Bias (Zener, Rectifier)	1038	A	80% Min. of rated VR or VRWM when DC conditions are specified. 95-100% of VRWM, when half sine condition is specified.		

See footnotes at end of table.

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TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
4	X		Interim Electrical 1/ 3/	X	X	X	X	X	X	Per Acquisition Document			25°C Record Data	10(0)	C.3.3.4.3
	X		Burn-In	X	X					MIL-STD-750	1039	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X							X		MIL-STD-750	1042	A	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X					X	X			MIL-STD-750	1038	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X								X	MIL-STD-750	1040	B	240hrs Min at Tj=Max rated, +0°C, -25°C		
	X		Post BI Electrical 1/ 4/	X	X	X	X	X	X	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3

See footnotes at end of table.

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* TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

Subgroup	Class K	Class H	Test	Transistor - Signal	Transistor - Power	Diode - Zener	Diode - Power, Rectifier	IGBT, MOSFET - Power	SCR	Specification or Standard	Method	Condition	Comments	Quantity (Accept number)	Reference paragraph MIL-PRF-38534
4	X		Steady State Life	X	X					MIL-STD-750	1039	B	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C	10(0)	
	X							X		MIL-STD-750	1042	A	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C 80% Vds Min.		
	X					X	X			MIL-STD-750	1038	B	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C		
	X								X	MIL-STD-750	1040	B	1000hrs at Tj=125°C 500hrs at Tj=150°C 240hrs at Tj=175°C		
	X	X	Final Electrical 1/ 4/	X	X	X	X	X	X	Per Acquisition Document			25°C, -55°C, 125°C Record Data		C.3.3.4.3
5	X	X	Wirebond Evaluation 2/ 5/	X	X	X	X	X	X	MIL-STD-883	2011		Bake for 1 hour minimum @ +300ºC (Bimetallic bonds only)	10(0) or 20(1) wires	C.3.3.3 C.3.3.5
	X	X		X	X	X	X	X	X	MIL-STD-750	2037				
6	X		SEM 2/ 6/ 7/	X	X			X	X	MIL-STD-883	2018			See 7/	C.3.3.6
										MIL-STD-750	2077				

See footnotes at end of table.

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TABLE C-II-1. Semiconductor dice evaluation requirements - Continued.

1/ Test parameters chosen from applicable MIL-PRF-19500 slash sheet, applicable manufacturer's data sheet, and/or acquistion document.
2/ Either test method is applicable.
3/ When High Temp Reverse Bias (HTRB) is performed, leakage current shall be measured on each device before any other specified parametric test is performed and completed within 16 hours of HTRB completion.
4/ When required by the acquisition document, perform delta limit calculations.
5/ Select bond wires that represent the wire bond process used in the hybrid.
6/ SEM is not required for semiconductor dice without expanded metallization (reference method 2077 of MIL-STD-750).
7/ The quantity accept (reject) requirements specified herein for element evaluation supersede the sample size and selection requirements of method 2018 of MIL-STD-883 and method 2077 of MIL-STD-750. If the die are from a known homogeneous single wafer, then the sample size shall be 4 devices randomly selected from the wafer. If the die are from a non-homogeneous wafer lot (traceability is unknown or no objective evidence is available for verification), then the sample size shall be 8 devices randomly selected from the population. If the die are from known homogeneous multiple (two or more) wafers, then the sample size shall be 4 devices randomly selected from each of two wafers in the lot, 8 devices total. If any wafer from the lot fails, all remaining wafers in the lot must be tested (4 devices randomly selected from each wafer) to be verified as acceptable for use.

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* C.3.4 Passive elements. Passive elements from each inspection lot will be evaluated in accordance with tables C-III, C-III-1, C-III-2, C-III-3, C-III-4, and C.3.4.1 through C.3.4.7. This evaluation is not required when the elements are acquired as MIL specification qualified parts having the minimum product levels and/or established reliability levels and are listed on the QPL.

C.3.4.1 Subgroup 1, 100 percent electrical test of passive elements. Each passive element will be electrically tested at +25°C as specified in the element acquisition documents.

C.3.4.2 Subgroup 2, visual inspection of passive elements. Passive elements will be visually inspected to assure conformance with the applicable passive element related requirements of method 2032 of MIL-STD-883, and the passive element acquisition documents.

a. Each Class K passive element will be visually inspected.

b. Class H elements will be sample inspected using a sample size and (accept number) of 22 (0).

* C.3.4.3 Test sample preparation for subgroups 3 through 7 (as applicable).

a. For Class H and Class K passive elements, when assembly is required to perform electrical tests, test samples may be assembled such that the assembly methods and conditions the element will see during normal assembly will be simulated. Electrical probe testing may be performed in lieu of assembly.

b. The total test sample will contain at least ten wires (an equal number on each element) if wire bonding assembly is applicable.

* C.3.4.4 Sample electrical test of passive elements. Sample passive elements will be electrically tested at +25°C for the following characteristics (minimum):

a. Resistors: DC resistance.

b. Capacitors:

(1) Ceramic type: Dielectric withstanding voltage, insulation resistance, capacitance, and dissipation factor.

(2) Tantalum type: DC leakage current, capacitance, dissipation factor and equivalent series resistance.

(3) Metal insulation semiconductor type (MIS): Dielectric withstanding voltage, DC leakage current, and capacitance.

c. Inductors: Dielectric withstanding voltage, insulation resistance, inductance, Q, SRF and DC resistance.

d. Transformers and coils: Dielectric withstanding voltage, insulation resistance, induced voltage (when required), inductance and DC resistance.

e. Crystals: Frequency, insulation resistance and equivalent resistance.

C.3.4.5 Visual examination. Elements will be visually examined for evidence of corrosion or damage attributable to the test and conditioning sequence.

C.3.4.6 Wire bond strength testing. Wire bond strength testing applies to elements which are wire bonded during the device assembly operation. The sample will include at least five elements and ten bond wires minimum.

a. At least ten wires, consisting of element-to-substrate, element-to-package, or element-to-element bonds will be destructively pull tested. An equal number of bonds will be tested on each sample element.

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b. The element metallization will be acceptable if no failure occurs. If only one wire bond fails, a second sample will be selected and subjected to the test in accordance with C.3.4.6.a. If the second sample contains no failures, the bonding test results and the element lot are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot will be rejected.

c. The element inspection lot may be resubmitted to evaluation if the failure was not due to defective element metallization.

* C.3.4.7 Voltage conditioning or aging. Voltage conditioning or aging shall be performed in accordance with the appropriate passive device specification. When there is no applicable device specification, or the requirements of the device specifications are not appropriate, the manufacturer shall document the procedure being used. Below are some examples of performance specifications used for passive element conditioning requirements:

a. Resistors:

MIL-PRF- 914 - Resistor Networks, Fixed, Film, Surface Mount, Nonestablished Reliability, and Established Reliability, General Specification For.

MIL-PRF-32159 - Resistors, Chip, Fixed, Film, Zero Ohm, Industrial, High Reliability, Space Level, General Specification for.

MIL-PRF-39007 - Resistors, Fixed, Wire Wound (Power Type), Nonestablished Reliability, Established Reliability, and Space level, General Specification for

MIL-PRF-55182 - Resistors, Fixed, Film, Nonestablished Reliability, Established Reliability, and Space Level, General Specification for.

MIL-PRF-55342 - Resistors, Chip, Fixed, Film, Nonestablished Reliability, Established Reliability Space Level, General Specification for.

b. Capacitors:

MIL-PRF-123 - Capacitors, Fixed, Ceramic, Dielectric, (Temperature Stable and General Purpose), High Reliability General Specification for.

MIL-PRF-49470 - Capacitor, Fixed, Ceramic Dielectric, Switch Mode Power Supply (General Purpose and Temperature Stable), Standard Reliability and High Reliability, General Specification for.

MIL-PRF-55365 - Capacitor, Fixed, Electrolytic (Tantalum), Chip, Established Reliability, Nonestablished Reliability, and High Reliability, General Specification for.

MIL-PRF-55681 - Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established and Nonestablished Reliability, General Specification for.

MIL-PRF-32535 - Capacitor, Chip, Fixed, Ceramic Dielectric (Temperature Stable and General Purpose), Extended Range, High Reliability and Standard Reliability, General Specification for.

c. Coils, transformers:

MIL-PRF-27 - Transformers and Inductors (Audio, Power, and High Power Pulse) General Specification for.

MIL-PRF-15305 - Coils, Fixed and Variable, Radio Frequency, General Specification for.

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* TABLE C-III. Wire Bondable and Surface Mount Resistors. 1/ 2/

Subgroup	Class		Test	Wire Bondable Resistors	Surface Mount Resistors	Standard or Specification	Method / Paragraph	Condition	Comments	Quantity (accept number)		Ref Para MIL-PRF-38534
	K	H								Class K Samples	Class H Samples	
1	X	X	Element Electrical	X	X	MIL-PRF-55342	3.8		25C	100%	100%	C.3.4.1
2		X	Visual Inspection	X	X	MIL-STD-883	2032	H			22(0)	C.3.4.2
	X			X	X	MIL-STD-883	2032	K		100%		
	X	X	Device Finish 3/		X	MIL-PRF-38534				2 (0)	2 (0)	
3	X		Element Electrical	X	X	MIL-PRF-55342	3.8		Measure & Record DC Resistance @ 25C	10(0)		C.3.4.4
	X		Thermal Shock or Temperature Cycle	X	X	MIL-STD-202	107	F	-65C to +150C, 10 Cycles	10(0)		C.3.4.3
						MIL-STD-883	1010	C	-65C to +150C, 10 Cycles			
	X		Mechanical Shock or Constant Acceleration	X	X	MIL-STD-883	2002	B	Y1 Direction	10(0)		
							2001	A	Y1 Direction			

See footnotes at end of table.

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TABLE C-III. Wire Bondable and Surface Mount Resistors - Continued. 1/ 2/

Subgroup	Class		Test	Wire Bondable Resistors	Surface Mount Resistors	Standard or Specification	Method / Paragraph	Condition	Comments	Quantity (accept number)		Ref Para MIL-PRF-38534
	K	H								Class K Samples	Class H Samples	
3	X		Power Conditioning	X	X	MIL-PRF-55342	3.10	4.8.4	100 hours @ 70°C, 1.5X Rated Power	10(0)		
		X	Element Electrical	X	X	Acquisition Document or MIL-PRF-55342	3.8		Measure & Record DC Resistance @ 25C		10(0)	C.3.4.4
	X		Element Electrical 4/	X	X	MIL-PRF-55342	3.8		Measure & Record DC Resistance @ 25C Tolerance and Delta R.	10(0)		C.3.4.4
4	X	X	Wirebond Evaluation	X		MIL-PRF-55342	3.19.3			10 (0) or 20 (1) wires	10 (0) or 20 (1) wires	C.3.4.3 C.3.4.6
				X		MIL-STD-883	2011					

See footnotes at end of table.

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* TABLE C-III. Wire Bondable and Surface Mount Resistors - Continued. 1/ 2/

1/ Samples shall be taken from each production lot for each resistance value.
2/ Parts procured as MIL-PRF-55342 product level T or with Established Reliability (ER) failure rate R, S, U, or V are acceptable for use as is.
3/ Using a recognized methodology (e.g. method 2037 of MIL-STD-883, JESD213) verify that finishes containing Tin (Sn) have a minimum of 3% lead (Pb) by weight per MIL-PRF-38534.
4/ Delta R shall not exceed +/-0.5% after completion of test(s), unless otherwise specified in acquisition document.

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TABLE C-III-1. Capacitors, Ceramic. 1/ 2/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity (accept number)	Reference paragraph MIL-PRF-38534
	K	H							
1	X	X	Element Electrical	MIL-PRF-38534			25C	100%	C.3.4.1
2		X	Visual Inspection 3/	MIL-STD-883	2032	H		22 (0)	C.3.4.2
	X			MIL-STD 883	2032	K		100%	
				MIL-PRF-123			Appendix B (Chips)		
				MIL-PRF-49470			Para. 3.8 & 4.8.3 (Stacked)		
	X		Prohibited Material Inspection	MIL-STD-1580	Reqmt. 9.		Insure body (electrodes) & termination inspected for prohibited material.	5 (0)	
	X	X	Device Finish 4/	MIL-PRF-38534				5 (0)	
3	X		Thermal Shock/Temperature Cycle 5/	MIL-STD-202	107	B	20 cycles (-55C to +125C)	100%	C.3.4.3
				MIL-STD-883	1010	C	20 cycles (-65C to +150C)	100%	

See footnotes at end of table.

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TABLE C-III-1. Capacitors, Ceramic - Continued. 1/ 2/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity	Reference paragraph MIL-PRF-38534
	K	H						(accept number)	
3	X		Acoustic Imaging (CSAM) 6/				Use ECIA EIA-469 as a guideline	100%	
	X		Voltage Conditioning 3/ 7/	MIL-PRF-123	Para. 4.6.6.2		Devices ≤ 200Vdc 2X rated voltage 125C, 168 hrs min./ 264 hrs max.	100% PDA in accordance with MIL-PRF-123, Table XVI, overall requirement and 1 unit or ≤ 0.1% PDA in last 48Hrs.	C.3.4.7
				MIL-PRF-49470	Para. 4.8.5.2		Devices >200Vdc 1.2-2X rated voltage (consult manufacturer) 125C, 168 hrs min./ 264 hrs max.		

See footnotes at end of table.

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TABLE C-III-1. Capacitors, Ceramic - Continued. 1/ 2/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity	Reference paragraph MIL-PRF-38534
	K	H						(accept number)	
3		X	Dielectric Withstanding Voltage 3/ 7/	MIL-PRF-123	Para. 3.13		DC rated voltages: ≥500V ≤ 1000V dc test at 150% min <500Vdc test at 250% min.	10 (0)	
				MIL-PRF-49470	Para. 3.11				
	X		Dielectric Withstanding Voltage 3/ 7/	MIL-PRF-123	Para. 3.13		DC rated voltages: ≥500V ≤ 1000V dc test at 150% min <500Vdc test at 250% min.	100%	
				MIL-PRF-49470	Para. 3.11				
		X	Insulation Resistance 3/ 7/	MIL-PRF-123	Para. 3.14		Room	10 (0)	
				MIL-PRF-49470	Para. 3.10				
	X		Insulation Resistance, Room 3/ 7/	MIL-PRF-123	Para. 3.14			100%	
				MIL-PRF-49470	Para. 3.10				
	X		Insulation Resistance, Hot 3/ 7/	MIL-PRF-123	Para. 3.14		+125C	100%	
				MIL-PRF-49470	Para. 3.10				

See footnotes at end of table.

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TABLE C-III-1. Capacitors, Ceramic - Continued. 1/ 2/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity	Reference paragraph MIL-PRF-38534
	K	H						(accept number)	
3		X	Capacitance 3/ 7/	MIL-PRF-123	Para. 3.11			10 (0)	
				MIL-PRF-49470	Para. 3.13				
	X		Capacitance 3/ 7/	MIL-PRF-123	Para. 3.11			100%	
				MIL-PRF-49470	Para. 3.13				
		X	Dissipation Factor 3/ 7/	MIL-PRF-123	Para. 3.12			10 (0)	
				MIL-PRF-49470	Para. 3.12				
	X		Dissipation Factor 3/ 7/	MIL-PRF-123	Para. 3.12			100%	
				MIL-PRF-49470	Para. 3.12				
	X		Thermal Shock / Temperature Cycle 5/ 8/	MIL-STD-202	107	A	100 cycles (-55C to +125C)	Ref. MIL-PRF-123 Table XIX	C.3.4.3
				MIL-STD-883	1010	C	100 cycles (-65C to +150C)	Ref. MIL-PRF-123 Table XIX	
	X		Life Test 3/ 7/ 8/ 9/	MIL-PRF-123	Para. 3.23		1000 hrs (Interim Elec. 250 hrs, Final 1000 hrs)	Ref. MIL-PRF-123 Table XIX	
				MIL-PRF-49470	Para. 3.26				
	X		Element Electrical 3/ 7/ 9/	MIL-PRF-123	Para. 3.23		Measure & Record	Ref. MIL-PRF-123 Table XIX	C.3.4.4
				MIL-PRF-49470	Para. 3.26				

See footnotes at end of table.

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TABLE C-III-1. Capacitors, Ceramic - Continued. 1/ 2/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity	Reference paragraph MIL-PRF-38534
	K	H						(accept number)	
4 8/	X	X	Wire Bond Evaluation	MIL-STD-883	2011		Where applicable	10 (0) wires or 20 (1) wires	C.3.4.3 C.3.4.6
	X	X	Solderability	MIL-STD-202	208		Where applicable	K- 10 (0), or 20 (1) H- 5(0)	
				MIL-STD-883	2003				
	X		Terminal Strength 3/ 10/	MIL-PRF-123	Para. 3.16			10 (0)	C.3.4.6
				MIL-PRF-49470	Para. 3.24				
	X		Destructive Physical Analysis (DPA) 3/ 11/	MIL-PRF-123	Para. 3.15			Ref. MIL-PRF-123 Table XVII Group 1. 12/	
				MIL-PRF-49470	Para. 3.7				
5 8/	X		Voltage Temperature Limits 3/ 7/	MIL-PRF-123	Para. 3.19		None (Does Not Apply to X5R/X7R/X7S and other commercial ceramics)	12 (1)	
				MIL-PRF-49470	Para. 3.16				
	X		Humidity, steady state, low voltage	MIL-PRF-123	Para. 3.20			12 (0)	
	X		Moisture Resistance (85C/85%RH)	MIL-PRF-49470	Para. 3.21			12 (1)	

See footnotes at end of table.

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TABLE C-III-1. Capacitors, Ceramic - Continued. 1/ 2/

1/ Base Metal Electrode (BME) Capacitors used in Class H hybrid devices shall be evaluated in accordance with MIL-PRF-32535. BME capacitors used in Class K hybrid devices shall be evaluated in accordance with MIL-PRF-32535 product level T.
2/ Evaluation in accordance with this table is not required for elements procured as MIL-PRF-123, MIL-PRF-32535 product level T, MIL-PRF-49470 product level T, or MIL-PRF-55681 with Established Reliability failure rate S.
3/ Where MIL-PRF-123 and MIL-PRF-49470 are identified, use of either specification is acceptable. However, remain consistent in selection and use the standard to which the part was made. If MIL-PRF-49470 is used to evaluate Class K elements, then testing shall be in accordance with product level T requirements.
4/ Using a recognized methodology (e.g. method 2037 of MIL-STD-883, JESD-213) verify that finishes containing Tin (Sn) have a minimum of 3% Lead (Pb) by weight per MIL-PRF-38534.
5/ Either test method is acceptable.
6/ Utilize a methodology equivalent to or better than that which is specified in MIL-PRF-123 para. 4.6.1. For stacked components Acoustic Imaging must be done on individual pre-stacked components.
7/ Higher voltage devices (>250V) which are not covered by MIL-PRF-123 or MIL-PRF-49470 shall be examined under the rules established in MIL-PRF-49470.
8/ Testing is destructive.
9/ Interim and Final measure - Capacitance, Insulation Resistance and Dissipation Factor at 25C, Insulation Resistance at 125C.
10/ Consult manufacturer for case sizes not addressed in MIL-PRF-123 or MIL-PRF-49470.
11/ This test is not required to be performed in sequence
12/ Use sample sizes specified in MIL-PRF-123 Table XVII for group 1.

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TABLE C-III-2. Chip Capacitors, Solid Tantalum. 1/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity (accept number)	Reference Paragraph MIL-PRF-38534
	K	H							
1	X	X	Element Electrical	MIL-PRF-38534		25C	Per Aquisition Document	100%	C.3.4.1
2	X	X	Device Finish 2/	MIL-STD-883	2037		For terminations containing Sn	5 (0)	
	X		Visual Inspection	MIL-STD-883	2032			100%	C.3.4.2
		X						22 (0)	
3	X		Reflow Conditioning	MIL-PRF-55365	Para. 4.7.10			100%	
	X		Thermal Shock (Unmounted)	MIL-STD-202	Test Method 107	A 3/	-55 to 125C, 5 cycles	100%	
	X		Surge Current (SC)	MIL-PRF-55365	Para. 4.7.18	C		100%	
	X		Weibull FRL Grading	MIL-PRF-55365	Para. 4.7.20	C	Retain test results Read & Record Data	100%	
	X		DC Leakage	MIL-PRF-55365	Para. 4.7.6			100%	
		X						10 (0)	

See footnotes at end of table.

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TABLE C-III-2. Chip Capacitors, Solid Tantalum - Continued. 1/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity (accept number)	Reference Paragraph MIL-PRF-38534
	K	H							
3	X		Capacitance	MIL-PRF-55365 and	Para. 4.7.7		Retain test results Read & Record Data	100%	
		X		MIL-STD-202	305			10 (0)	
	X		Dissipation Factor	MIL-PRF-55365	Para. 4.7.8			100%	
		X						10 (0)	
	X		ESR	MIL-PRF-55365	Para. 4.7.14			100%	
		X						10 (0)	
	X		+3 sigma cull required for DF, ESR, DC Leakage	MIL-PRF-55365		MIL-PRF-55365 1.2.1.6 Table III	Remove parts that fail +3 sigma cull.	100%	
4	X		Radiographic Inspection	MIL-PRF-55365	Para. 3.5			100%	
5	X	-	Stability at low and high temperature	MIL-PRF-55365	Para. 3.19			22 (0)	
6 4/	X	X	Wire Bond Evaluation	MIL-STD-883	2011		For wire bonding applications	10 (0) wires or 20 (1) wires	C.3.4.3 C.3.4.6
	X	X	Solderability	MIL-STD-202	208		For soldering applications	5(0)	
	X		Destructive Physical Analysis	MIL-STD-1580				5 (0)	
7	X		Life Test	MIL-PRF-55365	Para. 4.7.19	Per Table VI	2000 Hrs at 125C	24 (1)	

1/ For Class H hybrid devices, element evaluation in accordance with this table is not required for capacitors that are compliant to MIL-PRF-55365 and are listed on the QPL. For Class K hybrids, element evaluation in accordance with this table is not required for capacitors procured as QPL MIL-PRF-55365 product level T or product level M with minimum Weibull FRL C combined with surge current option C.

2/ Using a recognized methodology (e.g. method 2037 of MIL-STD-883, JESD-213) verify that finishes containing Tin (Sn) have a minimum of 3% Lead (Pb) by weight per MIL-PRF-38534. Device finish test may be conducted by hybrid manufacturer upon receipt of components. Device finish test may be conducted following visual inspection at the discretion of the capacitor manufacturer.

3/ Method 107 of MIL-STD-202 Condition A modified to adjust upper temperature limit to +125

4/ Subgroup 6 tests may be conducted in any order.

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TABLE C-III-3. Capacitors, MOS – NMOS. 1/

Subgroup	Class		Test	Standard or Specification	Method	Condition	Comments	Quantity (accept number)		Reference paragraph MIL-PRF-38534
	K	H						Class K	Class H	
1	X	X	Element Electrical	Per acquisition document			Measure at 25C	100%	100%	C.3.4.1
2		X	Visual Inspection	MIL-STD-883	2032	H			22(0)	C.3.4.2
	X			MIL-STD-883	2032	K		100%		
	X	X	Device Finish 2/	MIL-PRF-38534			Per acquisition document	2 (0)	2 (0)	
3	X		Thermal Shock or Temperature Cycle 3/	MIL-STD-202	107	F	10 cycles (-65C to +150C)	10(0)		C.3.4.3
				MIL-STD-883	1010	C	10 cycles (-65C to +150C)			
	X		Mechanical Shock or Constant Acceleration 3/	MIL-STD-883	2002	B	Y1 Direction	10(0)		
					2001	A	Y1 Direction			
	X	X	Element Electrical	Per acquisition document			Measure & Record at 25C	10(0)	10(0)	C.3.4.4
	X		Voltage Conditioning	Per acquisition document			100 Hours, 70C, WV	10(0)		C.3.4.7
	X		Element Electrical 4/	Per acquisition document			Measure & Record at 25C	10(0)		C.3.4.4
4	X	X	Wire Bond Evaluation	MIL-STD-883	2011			10 (0) or 20 (1) wires	10 (0) or 20 (1) wires	C.3.4.3 C.3.4.6

1/ Samples shall be taken from each production lot for each capacitance value.
2/ Using a recognized methodology (e.g. method 2037 of MIL-STD-883, JESD-213) verify that finishes containing Tin (Sn) have a minimum of 3% Lead (Pb) by weight per MIL-PRF-38534.
3/ Either test method is acceptable.
4/ Delta requirements for any electrical parameters shall meet limits as specified in the acquisition document.

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TABLE C-III-4. Coils, transformers.

Subgroup	Class			Test	Standard or Specification	Method	Condition	Comments	Quantity (accept number)	Reference paragraph MIL-PRF-38534
	K Closed	K Open 1/	H Open and Closed 1/							
1	X	X	X	Element Electrical	Acquisition Document			25°C	100%	C.3.4.1
2	X	X		Visual Inspection	MIL-STD-883 and MIL-STD-981	2032		MIL-STD-981: 5.5.3, 5.5.9, 5.5.12	100%	C.3.4.2
			X	Visual Inspection	MIL-STD-883	2032			22(0)	
3	X			Temperature Cycle	MIL-STD-883	1010	C	10 cycles	10(0)	C.3.4.3
	X			Mechanical Shock or Constant Acceleration 2/	MIL-STD-883	2002	B	Y1 direction	10(0)	
						2001	A	Y1 direction		
	X			Burn-In	MIL-STD-981	Section 5.6.7.3.4	Class S	T = Max Rating, 96hrs, Max Load	10(0)	
	X	X	X	Visual Inspection	MIL-STD-883 and MIL-STD-981	2032		MIL-STD-981: 5.5.3, 5.5.9, 5.5.12	10(0)	C.3.4.3 C.3.4.5
	X	X	X	Element Electrical	Acquisition Document				10(0)	C.3.4.3 C.3.4.4

See footnotes at end of table.

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TABLE C-III-4. Coils, transformers - Continued.

Subgroup	Class			Test	Standard or Specification	Method	Condition	Comments	Quantity (accept number)	Reference paragraph MIL-PRF-38534
	K Closed	K Open 1/	H Open and Closed 1/							
4 3/	X	X	X	Device Finish	MIL-STD-883 or JESD 213	2037		Not required for components that contain no solder or tin (e.g., ferrite magnetics with copper wires).	5(0)	
	X	X	X	Wire bondability	MIL-STD-883	2011		Where Applicable	H-5(0) K-10(0) or 20(1)	C.3.4.3 C.3.4.6
	X	X	X	Solderability	MIL-STD-883	2003		Where Applicable	H-2(0), K-5(0)	
	X	X	X	Terminal Strength	MIL-STD-981	Para. 5.6.7.4		Where Applicable	H-2(0), K-5(0)	C.3.4.6

1/ Magnetic elements built in house by the hybrid manufacturer may be tested per the Class K open construction requirements or Class H requirements, as applicable. Elements must be qualified with the hybrid and not manufactured for sale as a separate qualified component. Construction techniques and materials must meet or exceed that of MIL-STD-981 (where applicable).
2/ Either test method is acceptable.
3/ Group 4 tests may be conducted in any order.

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C.3.5 Surface acoustic wave (SAW) element evaluation. SAW elements will be evaluated in accordance with table C-IV and C.3.5.1 through C.3.5.3.

C.3.5.1 Radio frequency (RF) probe test. Each SAW element will be RF probe tested as specified in the device specification. This RF probe test may be done at the wafer level provided all failures are identified and removed from the lot when the elements are separated from the wafer. RF probe testing will be performed at +25°C unless otherwise specified by the device specification.

C.3.5.2 Visual inspection. Each SAW element will be visually inspected to ensure conformance with the requirements of method 2032 of MIL-STD-883.

C.3.5.3 Wire bond evaluation. From each inspection lot of SAW elements, a randomly selected sample of at least two elements will be evaluated for wire bond pull strength.

a. A minimum of ten wires will be bonded and destructively pull tested in accordance with method 2011 of MIL-STD-883.

b. The SAW element metallization will be acceptable if no failure occurs. If only one wire bond fails, a second sample will be selected and subjected to the test in accordance with C.3.5.3.a. If the second sample contains no failures, the bonding test results and the element lot are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot will be rejected.

c. The element inspection lot may be resubmitted to wire bond evaluation if the failure was not due to defective element metallization.

d. With acquiring activity approval, destructive bond pull tests may be performed on test coupons that provide the specified test requirements. Test coupons shall be processed with the same element production lot.

TABLE C-IV. SAW element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883, method	Quantity (accept number)	Reference paragraph
	K	H				
1	X	X	RF electrical probe		100 percent	C.3.5.1
2	X	X	Visual inspection	2032	100 percent	C.3.5.2
3	X	X	Wire bond evaluation	2011	10 (0) wires or 20 (1) wires	C.3.5.3

C.3.6 Alternate element evaluation. Alternate element evaluation will be used only in cases where full device performance cannot be adequately ascertained outside the actual end item (e.g., hybrid microcircuit RF component). The sample built into devices shall successfully complete evaluation prior to release of the balance of the incoming lot. In lieu of packaged element evaluation tests in accordance with C.3.3, C.3.4, and C.3.5, elements may be assembled into devices and screened in accordance with table C-IX through final electrical. Acceptance of these elements will be based on the ability of the device to meet all group A, subgroups 1, 2, and 3 (plus 4, 7, and 9, as applicable) electrical tests required for the device. A minimum of ten elements or 100 percent of the elements, whichever is less, (0 defects) will be assembled into at least 3 devices. Devices assembled for the purpose of element evaluation are deliverable provided all of the provisions of this specification are met. Element wire bond evaluation for elements may be accomplished using a second or additional sample of elements wire bonded for that purpose only. When the device build option for evaluation is selected, the manufacturer will establish and maintain a sample plan or procedure to identify the sample prior to electrical test. In case of lot failure when alternative element evaluation is used, all of the device samples and the inspection lots will be rejected. When the manufacturer chooses to analyze the failed devices to isolate the cause of failure and this analysis determines that the cause of failure is not related to the element being tested, and that the element has been correctly stressed during the required screening and testing, then the inspection lot may be accepted. If the element has not been correctly stressed, the failed device may be reworked or new sample replacement devices may be assembled.

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C.3.7 Substrate evaluation. Substrates will be evaluated in accordance with table C-V and C.3.7.1 through C.3.7.5.3.3.

NOTE: Substrates fabricated by the device manufacturer using a qualified process will be exempt from this evaluation.

C.3.7.1 Definition. For the purpose of substrate evaluation, a substrate inspection lot will consist of homogeneous substrates having the same number of layers, manufactured using the same facilities, processes, materials, and vacuum deposited, plated, or printed as one lot.

C.3.7.2 Electrical test parameters. Electrical test parameters, values, limits, and conditions will be as specified in the applicable device specification.

C.3.7.3 Subgroup 1, 100 percent electrical testing. Each substrate will be electrically tested at +25°C, if and as specified in the applicable device specification.

C.3.7.4 Subgroup 2, 100 percent visual inspection. Each substrate will be visually inspected to ensure conformance with the applicable requirements of method 2032 of MIL-STD-883, and the applicable device specification.

C.3.7.5 Subgroups 3, 4, and 5 general requirements. From each inspection lot of substrates, a randomly selected sample will be evaluated. Destructive tests may be performed on test coupons which provide the required test data. The test coupons shall be made with the same materials that were used in the manufacturing of the inspection lot and processed at the same time as the inspection lot.

C.3.7.5.1 Subgroup 3. A minimum of five samples will be submitted to subgroup 3 testing.

C.3.7.5.1.1 Physical dimension. Inspect in accordance with method 2016 of MIL-STD-883, and the applicable device specification.

C.3.7.5.1.2 Visual inspection. Inspect in accordance with method 2032 of MIL-STD-883, and the applicable device specification.

C.3.7.5.1.3 Electrical. Substrates will be electrically tested at +25°C for the following characteristics (minimum). Requirements will be as specified in the applicable device specification.

a. Resistors: DC resistance.

b. Capacitors: Capacitance. As specified in the applicable device specification, test for dielectric withstanding voltage, insulation resistance, and dissipation factor.

c. For multilayered substrates, continuity and isolation testing will be performed to verify the interconnection of conductors as specified in the applicable device specification.

C.3.7.5.2 Subgroup 4. A minimum of three samples that have been subjected to, and passed, subgroup 3 testing will be submitted to subgroup 4 testing.

C.3.7.5.2.1 Conductor thickness. Measure conductor thickness in accordance with the applicable device specification. Conductor thickness will meet the requirements specified in the applicable device specification.

C.3.7.5.2.2 Conductor resistivity. Measure conductor resistivity in accordance with the applicable device specification. Conductor resistivity will meet the requirements specified in the applicable device specification.

C.3.7.5.2.3 Film adhesion. Perform film adhesion testing in accordance with acceptable industry standards. The substrate and tape will show no evidence of peeling or flaking of metallization.

C.3.7.5.2.4 Solderability. For solderable substrates only, perform solderability testing if specified in the applicable device specification.

C.3.7.5.3 Subgroup 5. A minimum of two samples that have been subjected to, and passed, subgroup 3 testing will be submitted to subgroup 5 testing.

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C.3.7.5.3.1 Temperature coefficient of resistance (TCR): Perform TCR testing for resistors in accordance with method 304 of MIL-STD-202. TCR will meet the requirements specified in the applicable device specification.

a. Thick film type: Test as a minimum, two resistors from each resistor paste sheet resistance value. One from the smallest and one from the largest area resistors at -55°C using a reference reading at +25°C, or temperatures as specified in the device specification.

b. Thin film type: Test as a minimum, the highest value resistor at +125°C using a reference reading at +25°C, or temperatures as specified in the device specification.

c. If specified in the applicable device specification, TCR tracking testing will be performed. TCR tracking will meet the requirements specified in the applicable device specification.

C.3.7.5.3.2 Wire bond strength testing. For wire bondable substrates, perform wire bond strength testing in accordance with method 2011 of MIL-STD-883. The sample will include at least two substrates and ten bond wires minimum. For gold metallized Class K substrates that at the device level are intended to contain aluminum wire bonds, aluminum wires will be placed as specified in the device specification and these wire bond samples will be baked for 1 hour at +300°C in either an air or an inert atmosphere prior to the performance of wire bond strength testing.

a. At least ten wires, consisting of substrate to substrate bonds, will be destructively pull tested. An equal number of bonds will be tested on each sample substrate.

b. The substrate metallization will be acceptable if no failure occurs. If only one wire bond fails, a second sample of a minimum of ten wires will be prepared using the same wire type/size and the same type equipment as the failed bond(s). If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the substrate inspection lot will be rejected.

c. The substrate inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective substrate metallization.

C.3.7.5.3.3 Die shear strength testing. Perform shear strength testing in accordance with method 2019 of MIL-STD-883. At least two die for each substrate will be attached and tested for each die attachment method as specified in applicable device specification. If a failure occurs at less than the specified force and is not due to defective substrate materials, the lot will be resubmitted to die shear evaluation and the failure mode documented.

TABLE C-V. Substrate evaluation requirements.

Subgroup	Class		Test	MIL-STD-883 Method	Quantity (accept number)	Reference paragraph
	K	H				
1	X	X	Electrical testing		100 percent	C.3.7.3
2	X	X	Visual inspection	2032	100 percent	C.3.7.4
3	X	X	Physical dimensions	2016	5 (0)	C.3.7.5.1.1
	X	X	Visual inspection	2032		C.3.7.5.1.2
	X	X	Electrical			C.3.7.5.1.3
4	X	X	Conductor thickness or conductor resistivity		3 (0)	C.3.7.5.2.1 C.3.7.5.2.2
	X	X	Film adhesion			C.3.7.5.2.3
	X	X	Solderability			C.3.7.5.2.4
5	X	X	TCR		2 (0)	C.3.7.5.3.1
	X	X	Wire bond evaluation	2011	10 (0) wires or 20 (1) wires	C.3.7.5.3.2
	X	X	Die shear evaluation	2019	2 (0)	C.3.7.5.3.3

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C.3.8 Package evaluation. Package cases or covers will be evaluated in accordance with table C-VI and C.3.8.1 through C.3.8.8.

C.3.8.1 Definitions.

C.3.8.1.1 Package inspection lot. A package inspection lot will consist of homogeneous packages of the same type and outline dimensions (may differ only in lead length and lead count), manufactured using the same facilities, processes, materials (multiple material lots are acceptable), and plated as one lot within a 6 month time frame (if plating is applicable).

C.3.8.1.2 Cover inspection lot. A cover inspection lot will consist of homogeneous covers of the same type and outline dimension, manufactured using the same facilities, processes, materials (multiple material lots are acceptable), and plated as one lot within a 6 month timeframe (if plating is applicable).

C.3.8.2 General.

a. From the package inspection lot, a randomly selected sample will be subjected to package evaluation.

b. Subgroups 1, 2, 3, 4, and 5 of table C-VI will be accomplished for each package inspection lot.

c. Subgroups 1 and 2 of table C-VI will be accomplished for each cover inspection lot.

d. Subgroup 6 shall be performed in accordance with C.3.8.8.

e. For lead integrity, a quantity of 3 packages minimum with an accept number of 15 (0) leads will be tested. If the 15 (0) lead requirement cannot be met with three packages then all of the leads from the three packages will be tested with zero failures. Based on package design / lead configuration (unless otherwise specified), additional lead integrity testing on 3 (0) leads minimum may be required for test condition A1 and E. Choose all conditions that apply for lead integrity.

NOTE: Test condition A1 does not apply to case ground brazed leads.

f. For solderability testing, a quantity of 3 packages minimum with an accept number of 15 (0) will be tested. If the 15 (0) lead requirement cannot be met with three packages then all of the leads from the three packages will be tested with zero failures.

g. The same samples may be used for subgroups 1, 2, 3, 4, and 5.

C.3.8.3 Subgroup 1. Separately verify case and cover dimensional compliance with the acquisition documents.

C.3.8.4 Subgroup 2. Visual inspection of cases and covers (100 percent). Device finish shall be in accordance with the acquisition document.

C.3.8.5 Subgroup 3. The subgroup shall be performed in sequence if the package is seal tested unlidded. As an option, the packages may be evaluated by performing package seal and leak test (method 1014 of MIL-STD-883) and lead integrity test may be performed before seal or after seal provided devices are leak tested after lead integrity.

C.3.8.6 Subgroup 4. For metal cases with leads separated by an insulator, measure insulation resistance between the metal body of the case and the leads that are isolated from the case. This test does not apply to non-metallic cases.

C.3.8.7 Subgroup 5. Solderability shall be performed per table C-VI. Subgroup 1-4 samples may be used to perform subgroup 5 test.

C.3.8.8 Subgroup 6. Separately verify case and cover for compliance with subgroup 6 of table C-VI. Corrosion in the internal cavity area will not be cause for rejection. Salt atmosphere shall be performed one time only for Class H and at 6-month intervals for Class K unless there is a change in material or plating.

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TABLE C-VI. Package evaluation requirements.

Subgroup	Class		Test	Specification or Standard			Quantity (accept number)	Reference paragraph
	K	H			Method	Condition		
1	X	X	Physical dimensions	MIL-STD-883	2016	Acquisition document	3 (0)	C.3.8.3
2	X	X	Visual Inspection 1/	MIL-STD-883	2009		100 percent	C.3.8.4
	X	X	Device Finish 2/	MIL-PRF-38534	N/A	Acquisition document	3 (0)	C.3.8.4
3	X	X	Thermal shock	MIL-STD-883	1011	C	3 (0)	C.3.8.2 and C.3.8.5
	X	X	High temperature bake	MIL-STD-883	1008	1 hour at +150°C		
	X	X	Lead integrity	MIL-STD-883	2004 2028	A1 (braze attached leads, 3 lead minimum). B1 (rigid leads and terminals only) B2 (lead fatigue) D (pad adhesion of leadless chip carriers) E (plating integrity of flexible and semi-flexible lead, 3 leads minimum).		
					2028 3/	Pin grid array leads		
	X	X	Seal		1014	A4 Unlidded cases		
4	X	X	Metal package isolation		1003	600 V dc 100 nA maximum	3 (0)	C.3.8.6
5	X	X	Solderability	MIL-STD-883	2003	Soldering temperature +245°C ± 5°C	3 (0)	C.3.8.7
6	X	X	Salt atmosphere		1009	A	3 (0)	C.3.8.8

1/ JESD 9 may be used as a guideline to enhance MIL-STD-883, method 2009.
2/ Using a recognized methodology (e.g. EDS, XRF) verify that finishes containing tin (Sn) have a minimum of 3 percent lead (Pb) by weight per MIL-PRF-38534 (JESD213 is also acceptable). Not required on packages with gold plated bodies and pins.
3/ B1 of method 2004 can be used as an option.

C.3.9 Integral substrate/package (ISP) evaluation. (ISP) will be evaluated in accordance with table C-VII and C.3.9.1 through C.3.9.10.

C.3.9.1 ISP inspection lot. For the purpose of ISP evaluation, an ISP inspection lot shall consist of ISP of the same type; manufactured using the same facilities, processes and materials (multiple material lots are acceptable), within 90 days.

C.3.9.2 General.

a. Section C.3.9 is intended to be used as an end-of-line ISP acceptance procedure performed at the completion of the ISP construction and prior to assembly of the device.

b. ISP elements fabricated by the hybrid device manufacturer using a MIL-PRF-38534 qualified process will be exempt from this evaluation as long as C.3.7 and C.3.8 are used for the components of the ISP.

c. Subgroups 1, 2, 3, 4, 5, 6, and 7 of table C-VII will be accomplished for each inspection lot.

d. For lead integrity, a quantity of three packages minimum with an accept number of 15 (0) will be tested. If the 15 (0) lead requirement cannot be met with three packages then all of the leads from the three packages will be tested with zero failures. Based on package design / lead configuration (unless otherwise specified), additional lead integrity testing may be required for test condition A1 and E. Choose all conditions that apply for lead integrity

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e. For solderability testing, a quantity of three packages minimum with an accept number of 15 (0) leads will be tested. If the 15 (0) lead requirement cannot be met with three packages then all of the leads from the three packages will be tested with zero failures.

f. The same samples may be used for subgroups 3, 4, 5, 6, and 7 of table C-VII.

g. Subgroups 8 shall be performed in accordance with C.3.9.10.

C.3.9.3 Subgroup 1. Each element will be electrically tested at +25°C as specified in the device specification. If none is stated, the device manufacturer shall use their standard procedure.

NOTE: This may be satisfied by performing a continuity/isolation test.

C.3.9.4 Subgroup 2. Each element will be visually inspected to ensure conformance to the applicable requirements of method 2009 and method 2032 of MIL-STD-883, and the applicable device specification. This inspection shall be limited to the features that are inspectable.

C.3.9.5 Subgroup 3 Device finish shall be in accordance with the acquisition document.

C.3.9.6 Subgroup 4. The physical dimensions will be verified against the device specification.

C.3.9.7 Subgroup 5. Wire bond strength testing. For wire bondable devices, perform wire bond strength testing in accordance with method 2011 of MIL-STD-883. The sample size shall include at least two ISP devices and ten bond wires minimum. For gold metallized Class K ISPs that at the hybrid level are intended to contain aluminum wire bonds, aluminum wires shall be placed as specified in the device specification and these wire bond samples shall be baked for one hour at 300°C $\pm$10°C in either air or an inert atmosphere prior to the performance of wire bond strength testing.

a. At least ten wires, consisting of substrate to substrate bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample ISP device.

b. The ISP metallization shall be acceptable if no failures occur. If only 1 wire bond fails, a second sample of a minimum of ten additional wires shall be prepared using the same wire type/size and the same type of equipment as the failed bond. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the ISP lot shall be rejected.

c. The ISP inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective ISP metallization.

C.3.9.8 Subgroup 6. The subgroup shall be performed in sequence if the package is seal tested unlidded. As an option, the packages may be evaluated by performing package seal and leak test (method 1014 of MIL-STD-883) and if package seal is performed, lead integrity test may be performed before or after seal.

C.3.9.9 Subgroup 7. Prior to solderability testing, the elements shall be submitted to a preconditioning temperature of +250°C $\pm$10°C for a period of 6 $\pm$0.5 hours, or equivalent. (See C.6.3.2.6 herein for examples of equivalent conditions) and then tested to the requirements of method 2003 of MIL-STD-883

C.3.9.10 Subgroup 8. Corrosion in the internal cavity area shall not be cause for rejection. This test shall be performed one time only for the life of the program, or as needed to evaluate changes in the fabrication process.

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TABLE C-VII. Integral substrate/package element evaluation requirements.

Subgroup	Class		Test	Specification or standard	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H			Method	Condition		
1	X	X	Electrical testing	Acquisition document			100 percent	C.3.9.3
2	X	X	Visual inspection 1/		2032 and 2009		100 percent	C.3.9.4
3	X	X	Device finish used 2/	MIL-PRF-38534	N/A	Acquisition document	3 (0)	C.3.9.5
4	X	X	Physical dimensions	MIL-STD-883	2016	Acquisition document	3 (0)	C.3.9.6
5	X	X	Wire bond evaluation	MIL-STD-883	2011		10 wires (0) 20 wires (1)	C.3.9.7
6	X	X	Thermal shock	MIL-STD-883	1011	C	3 (0)	C.3.9.2 and C.3.9.8
	X	X	Lead integrity	MIL-STD-883	2004	A1 (braze attached leads, 3 lead minimum). B1 (rigid leads and terminals only) B2 (lead fatigue) D (pad adhesion of leadless chip carriers) E (plating integrity of flexible and semi-flexible lead, 3 leads minimum).		
					2028 3/	Pin grid array leads		
	X	X	Seal	MIL-STD-883	1014	A4		
7	X	X	Solderability	MIL-STD-883	2003	Solder temperature +245°C ± 5°C	3 (0)	C.3.9.9
8	X	X	Salt atmosphere	MIL-STD-883	1009	A	3 (0)	C.3.9.10

1/ JESD 9 may be used as a guideline to enhance MIL-STD-883, method 2009.
2/ Using a recognized methodology (e.g. EDS, XRF) verify that finishes containing tin (Sn) have a minimum of 3 percent lead (Pb) by weight per MIL-PRF-38534 (JESD213 is also acceptable). Not required on packages with gold plated bodies and pins.
3/ B1 of method 2004 can be used as an option.

C.3.10 Polymeric material evaluation. The polymeric materials used in device applications will be subjected to and pass the evaluation procedures detailed in method 5011 of MIL-STD-883.

C.3.11 Sub-assembly element evaluation. Sub-assemblies used inside of hybrid microcircuits shall meet the requirements specified herein.

NOTE: Sub-assemblies that are produced by the hybrid manufacturer or an outside QML certified hybrid manufacturer for the applicable class are exempt from this requirement and apply only to parts procured from other outside source(s).

C.3.11.1 Acceptance of sub-assembly.

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C.3.11.2 Elements of sub-assemblies. Elements used in sub-assemblies (e.g. substrate, wire, active elements, passive elements, attach material, coatings, encapsulates and/or other materials) shall receive element evaluation prior to assembly of the sub-assembly as specified in Appendix C for the respective element type and class level.

NOTE: All polymeric material used in subassemblies is required to pass certification and acceptance testing in accordance with method 5011 of MIL-STD-883.

C.3.11.3 Production and inspection lot. The sub-assembly shall meet the production lot and inspection lot definition of Appendix A or equivalent and all materials shall be traceable per requirements of paragraph A.3.8.

C.3.11.4 Process control. The sub-assembly, as required, shall meet the process control requirements of Appendix C (e.g. wirebond process control, die shear) or equivalent.

C.3.11.5 Sample selection. Samples shall be selected from each sub-assembly inspection lot and subjected to the sections of table C-VII-1 according to the applicable class level.

C.3.11.6 Sub-assembly element evaluation requirements.

C.3.11.6.1 Subgroup 1. When testing requirements are not specified in the procurement document, the manufacturer of the sub-assembly shall choose the parameters, conditions, and limits to assure compliance with the electrical characteristics. Electrical testing shall be performed 100 percent at 25ºC as a minimum.

C.3.11.6.2 Subgroup 2. 100 percent internal visual inspection shall be performed to the applicable class level in accordance with method 2017 of MIL-STD-883. If coatings or sealing operations are performed, all inspections shall be performed prior to the coating or seal operations and any other operation that would obscure the sub-assembly workmanship. If the sub-assembly is an open construction, inspection will be required to meet method 2017 of MIL-STD-883.

C.3.11.6.3 Subgroup 3. Each sample shall be inspected in accordance with the applicable requirements of the sub-assembly to method 2009 of MIL-STD-883. If the sub-assembly is an open construction, inspection will be required to meet method 2017 of MIL-STD-883.

C.3.11.6.4 Subgroup 4. Using a recognized methodology, finishes containing tin (Sn) shall have a minimum of 3 percent lead (Pb) by weight. All other finishes shall be in accordance with the procurement document.

C.3.11.6.5 Subgroup 5. The sub-assembly shall be sample screened based on its construction technology as indicated in subgroup 5. As applicable, the samples may be mounted in accordance with its end item application.

C.3.11.6.5.1 Temperature cycling. Each sample sub-assembly shall be subjected to a minimum of 100 temperature cycles to method 1010 of MIL-STD-883 to assure bond integrity of the encapsulated bond wires. Non-encapsulated sub-assemblies shall require 10 cycles.

C.3.11.6.5.2 Interim electrical test. Each sample sub-assembly shall be electrically tested at 25ºC and the maximum specified operating temperature in accordance with the procurement document. When testing is not specified in the procurement document, the manufacturer of the sub-assembly shall choose the parameters, conditions, and limits to assure compliance with the electrical characteristics.

C.3.11.6.5.3 Post burn-in electrical test. Each sample sub-assembly shall be electrically tested at minimum temperature, 25ºC, and maximum specified operating temperature in accordance with the procurement document. When testing is not specified in the procurement document, the manufacturer of the sub-assembly shall choose the parameters, conditions, and limits to assure compliance with the electrical characteristics.

C.3.11.6.6 Subgroup 6. If the sub-assembly is encapsulated, sealed or contains metallic element attach (for power elements), the sub-assembly shall be inspected to either radiography method 2012 or Ultrasonic inspection of die attach method 2030 of MIL-STD-883.

C.3.11.6.7 Subgroup 7. Wirebonding is applicable to sub-assembly end item external wire bonds. The sub-assembly shall receive a destruct wire bond evaluation in accordance with method 2011 of MIL-STD-883.

a. At least 10 wires shall be destructively pull tested from a minimum of two samples. Additional samples may be used to meet the 10 wire minimum criteria.

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b. The bond pull will be acceptable if no failure occurs. If only one wire bond fails, a second sample of a minimum of 10 wires will be prepared using the same type equipment as the failed bond(s). If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the inspection lot will be rejected.

c. The production/inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective substrate metallization.

C.3.11.6.8 Subgroup 8. If applicable to the sub-assembly, all elements from two samples shall be die shear tested in accordance with method 2019 of MIL-STD-883. If a failure occurs at less than the specified force and is not due to defective materials, then the lot shall be resubmitted to die shear evaluation and the failure mode documented.

* Table C-VII-1 Sub-assembly element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept No.)	Reference Paragraph
	K	H		Method	Condition		
1	X	X	Element electrical		+25°C only	100%	C.3.11.6.1
2	X	X	Internal Visual	2017	H or K	100%	C.3.11.6.2
3	X	X	External Visual	2009/2017	H or K	10(0)	C.3.11.6.3
4	X	X	Device Finish	N/A	N/A	5(0)	C.3.11.6.4
5	X	X	Temperature cycling	1010	C, 100 /10 cycles 1/	10 (0)	C.3.11.6.5.1
	X		Constant Acceleration or Mechanical Shock	2001 2002	Y1 direction @ 3Kg or Y1 direction, Cond B		
	X	X	Interim electrical				C.3.11.6.5.2
	X		Burn-in	1015	240 hours Min. @ +125°C		
	X		Post Burn-in electrical				C.3.11.6.5.3
6	X		Radiographic or Ultrasonic Inspection	2012 2030		10(0)	C.3.11.6.6
7	X	X	Wire bond evaluation 2/	2011		2 devices, 10 (0) wires or 20 (1) wires	C.3.11.6.7
8	X	X	Die Shear 3/	2019		2 devices, all elements	C.3.11.6.8

1/ Un-encapsulated devices require a minimum of 10 cycles.
2/ Wire bond evaluation shall be performed to test the user's external wire bond connections. Internal wire bond connections are subjected to 100% temperature cycling in Subgroup C5 to assure bond integrity, reference paragraph C.3.11.6.5.1. Wirebond evaluation is not required for un-encapsulated devices.
3/ If die shear is performed prior to application of final protective coating, this test is not required.

C.4 PROCESS CONTROL

C.4.1 Description of process control. Process control is a methodology used to detect defective processes prior to completion of assembly. This section outlines the requirements for process control on two processes though process control may be applied to other areas. The indicated processes will be controlled in accordance with table C-VIII and C.4.2 and C.4.3.

C.4.2 Wire bonding.

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C.4.2.1 General. A process machine/operator evaluation will be performed:

a. When a machine is put into operation.

b. Periodically while in operation, not to exceed 4 hours.

c. When the operator is changed. Change of certified auto wire bond operators is allowed without machine re-evaluation if all other machine conditions for evaluation are maintained.

d. When any machine part has been changed.

e. When any machine adjustment of the process parameters has been made.

f. When the spool of wire is changed.

g. When a new device type is started (unless the machine was evaluated using test samples that also simulate the new device type, see C.4.2.2).

C.4.2.2 Standard evaluation circuit (test coupon or test vehicle). Standard evaluation circuits (test coupons or test vehicles) that simulate the production device metal bonding system (e.g., thick film, thin film, aluminum bonding pads, plated gold) may be destructively evaluated in lieu of the product.

C.4.2.3 Process machines. Process machines not meeting the evaluation requirements will not be used.

C.4.2.4 Corrective action of process machine. A process machine may be returned to operation only after appropriate corrective action has been implemented and the machine has been evaluated and passed testing in accordance with table C-VIII as required.

C.4.2.5 Data record. A data record will be maintained and identifiable to each machine, operator, shift, and date of test.

C.4.2.6 Wire bond process setup

C.4.2.6.1 Process machine/operator evaluation. Sample wires from three devices or a test sample will be destructively pull tested in accordance with method 2011 of MIL-STD-883, and as follows:

a. Class H devices: A minimum of ten wires total consisting of wire bonds to elements metallization bonding systems (e.g., thick film, thin film, aluminum bonding pads, plated gold) typical of device assembly operation will be tested.

b. Class K devices: A minimum of 15 wires total will be tested. As a minimum, wires tested will include one each from a typical transistor, diode, capacitor, and resistor die, and five wires from the header to the substrate, as applicable.

c. Class H and Class K: Evaluation results are acceptable if no failure occurs at less than the value given in method 2011 of MIL-STD-883. If any of the sample wires fail, the machine/operator will be deactivated and corrective action taken. When a new sample has been prepared, tested, and has passed this procedure, the machine/operator has been certified or recertified, it can be returned to service.

C.4.2.6.2 Lot sample bond strength. From each wire bonding lot, a random sample of at least two devices will be nondestructively tested in accordance with method 2023 of MIL-STD-883. This requirement does not apply to devices that are 100 percent nondestructively tested. Alternately, destructive pull testing in accordance with method 2011 may be performed. Devices with known visual wire bonding rejects will not be excluded from this sample.

a. A wire bonding lot consists of devices that are consecutively bonded using the same setup and wire, by one machine/operator (operator changes are allowed for autobonders) during the same period not to exceed 4 hours.

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b. In each sample device, at least 15 wires will be tested, including one wire from each type of transistor, diode, capacitor, and resistor chips, three wires from each type of integrated circuit, and five wires connecting package leads, as applicable. If there are less than 15 wires in the device, all wires will be tested. Sample devices will be inspected for lifted wires. Lifted wires resulting from bond pull testing will be counted as nondestruct pull test failures.

c. The wire bonding lot will be acceptable if no failure occurs. If one wire/bond fails, another sample of two devices will be selected and 100 percent nondestructively tested. If the second sample contains no failures, the wire bonding lot is acceptable. If the second sample also contains failure(s), or more than one wire/bond fails in the first sample, the bonding machine/operator will be removed from the operation.

d. The failures will be investigated and appropriate corrective action will be implemented. The machine/operator will be recertified in accordance with C.4.2.6.1 before being returned to operation. All devices bonded since the previous certification (lot sample bond strength test) will be subjected to 100 percent nondestructive bond strength testing (Class H).

e. For RF/microwave devices, test sample circuits that simulate the production device may be destructively evaluated in lieu of the product (see C.4.2.2). When test sample circuits are used, the data from this test will be used for SPC monitoring of the process/product.

C.4.3 Seal testing. All Class K devices shall receive fine leak testing after sealing, and prior to any other testing, without pressurization (bomb) within one hour of removal from sealing atmosphere. Class K devices may be sealed with any amount of helium tracer gas and shall pass the corresponding leak rate, or the helium leak rate may be calculated based on the helium tracer gas atmosphere.

37 percent Helium – 3.7×10^{-8} atm cc/sec He.
10 percent Helium – 1.0×10^{-8} atm cc/sec He.
5.0 percent Helium – 5.0×10^{-9} atm cc/sec He.
3.0 percent Helium – 3.0×10^{-9} atm cc/sec He.

Calculation:
He leak rate = 1×10^{-7} x He%/100%

If failure occurs, the lid seal rework requirements will be followed.

However, in lieu of back filling with helium, pressurization after seal and fine leak test may be performed to the applicable Class K reject (L) rate of TM 1014 of MIL-STD-883 used for screening in accordance with the different conditions allowed (helium, radioisotope, cumulative, OLT, etc.), no seal rework will be permitted and the failed parts will be scrapped or delidded for rework.

CAUTION NOTE: The use of helium fill for high voltage devices may lead to ionization of the helium and cause the parts to fail. The device manufacturer shall document the design accordingly if sealing in helium tracer gas or if other gas is damaging to the device.

C.4.4 Internal gas analysis process monitor. The manufacturer shall develop and document a system to utilize method 1018, of MIL-STD-883, as a guideline to monitor the sealing process. Levels of all gases reported, including moisture, shall be evaluated to the extent necessary to detect any variation in the sealing process, based upon the manufacturer's data. Reported gases shall be used to aid in identifying possible process deficiencies or evidence of out-of-control conditions.

C.4.5 Testing for pure tin finishes. The manufacturer will develop a test plan that will assure no parts used in the hybrid have a pure tin finish.

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TABLE C-VIII. Process control summary.

Operation	Class		MIL-STD-883		Paragraph
	K	H	Method	Condition	
Wire bonding	X X	X X	2011 2023		C.4.2
Seal	X		1014	A	C.4.3
Internal gas analysis	X	X	1018		C.4.4

C.5 DEVICE SCREENING

C.5.1 Description of device screening. Screening is a series of tests and inspections performed on each device in each lot in order to eliminate products which do not meet the performance requirements. Each device will be subjected to and pass all of the applicable screening tests and inspections in accordance with table C-IX and C.5.2 through C.5.13.

C.5.2 General.

a. Additional tests and inspections may be performed where experience indicates justifiable concern for specific quality characteristics.

b. Electrical test parameters, values, limits (including deltas), and conditions will be as specified on the device specification.

c. All devices that fail any test criterion in the screening sequence will be removed from the lot at the time of observation, or immediately at the conclusion of the test, in which the failure was observed.

d. When PDA, pattern failure, or delta limits have been specified, or other conditions for lot acceptance have been imposed, the required data will be recorded and maintained as a basis for lot acceptance.

e. Once rejected and verified as a device failure, rework and subsequent rescreening in accordance with the limitations of this specification may be performed.

f. Tests will be performed in the order specified in table C-IX, except as specified in C.5.11 and C.5.12.

C.5.3 Pre-seal burn-in test. Pre-seal burn-in is optional.

C.5.4 Non-destructive bond pull test for Class K devices. Non-destructive 100 percent bond pull test shall be performed for Class K devices. The total number of failed wires and the total number of devices failed will be recorded. The lot will have a PDA of 2 percent or one wire, whichever is greater based on the number of wires pulled in the wire bond lot or production lot. If the lot fails and resubmission is to be considered, the failed lot shall be subjected to failure analysis to determine the root cause(s) of the failures, and what corrective action, or rework is needed. The failure analysis shall also address the strength and bond integrity of the passing bonds in relationship to the process norm. The analysis, root cause, and corrective action shall be documented. After corrective action to bring the bond strengths back to process norms, a resubmission of the failed lot may be made which shall include 100% nondestructive pull of any rebonded wires, with zero failures allowed. Lots failing the Class K PDA requirement or resubmission shall not be delivered as Class H, G, D, or E product.

C.5.5 Internal visual inspection. Devices awaiting pre-seal inspection and accepted devices awaiting further processing will be stored in a controlled environment until sealed as specified in method 2017 of MIL-STD-883.

C.5.6 Visual inspection for damage. The manufacturer may inspect for damage after each thermal or mechanical screening step, or at any subsequent time in the screening sequence.

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C.5.7 Particle impact noise detection (PIND) test. PIND will be performed in accordance with test method 2020 of MIL-STD-883, condition A or B. For Class K devices, condition A shall be used unless otherwise specified. For Class K screening, the lot may be accepted on any of the five runs if the percentage of defective devices is less than 1 percent (or one device, whichever is greater). All defective devices will be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, will be rejected.

C.5.8 Pre-burn-in electrical test.

a. Pre-burn-in electrical testing is optional except when delta limit measurements are required. However, devices may be tested to remove defects prior to further screening and to form a basis for application of PDA criteria.

b. This test need not include all device parameters, but will include those measurements most sensitive to, and effective in removing, electrically defective devices.

c. When delta limits are specified in the device specification, the measurements will be recorded, and traceability will be maintained from the device to the corresponding electrical test data.

C.5.9 Burn-in. Burn-in will be performed on each device.

C.5.9.1 General.

a. Pre-burn-in (interim burn-in for Class K) and post burn-in electrical parameters as specified in the device specification will be measured.

b. Burn-in electrical conditions will be as specified in the device specification.

c. Delta limits will be defined in the device specification when required.

d. Delta measurements will be made on parameters specified in the device specification.

e. The manufacturer will determine and document, prior to beginning burn-in, the criteria for the formation of burn-in lots (e. g., devices submitted to burn-in at one time, a production lot, or an inspection lot). The burn-in lot will be $\geq$ 41 devices or all devices submitted to burn-in during a 1 week period.

f. The manufacturer will not conduct burn-in in addition to that specified.

g. Unless otherwise specified in the device specification, PDA, and pattern failure, analysis will be applicable only to +25°C static tests (group A, subgroup 1).

C.5.9.2 Burn-in period.

a. Class K devices will be burned-in in accordance with the time-temperature regressions specified in method 1015 of MIL-STD-883. The burn-in time will be equally divided into two successive burn-ins. Interim electrical tests in accordance with the device specification will be performed after the first burn-in to determine acceptable devices for the second burn-in.

b. Class H devices will be burned-in in accordance with the time-temperature regressions specified in method 1015 of MIL-STD-883.

C.5.9.3 Failure analysis of burn-in screen failures for Class K devices. Catastrophic failures (e.g., shorts or opens measurable or detectable at +25°C) after burn-in will be analyzed. Analysis of catastrophic failures may be limited to a quantity and degree sufficient to establish failure mode and cause. Failure analysis results will be documented and available to the Government representatives.

C.5.9.4 Lots resubmitted for burn-in. Burn-in lots that do not exceed twice the allowable PDA may be resubmitted for burn-in one time only (e.g., if the PDA limit is ten percent, then the lot may be resubmitted if less than twenty percent). Failure analysis for other than Class K is not required. Resubmitted lots will be kept separate from new lots and will be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the PDA series. The number of pattern failures allowed will be the same as required for the original burn-in.

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C.5.9.5 Burn-in acceptance criteria. At the option of the manufacturer, burn-in acceptance will be based on PDA or pattern failures. Either option, or both, may be applied to a burn-in lot as acceptance criteria (i.e., if a lot exceeds PDA requirements, then pattern failure analysis may be used to determine if the lot is acceptable without performing a resubmitted burn-in).

C.5.9.5.1 General. Pattern failures are multiple device failures within a device burn-in lot with the same root cause of failure. When the PDA or pattern failures applies to delta limits, the delta parameter values measured after burn-in (100 percent screening test) will be compared with the delta parameter values measured prior to that burn-in.

C.5.9.5.2 PDA option.

C.5.9.5.2.1 PDA Class H. For Class H, the PDA will be 10 percent or one device, whichever is greater, regardless of burn-in lot size.

C.5.9.5.2.2 PDA Class K. For Class K, the PDA will be 2 percent or one device, whichever is greater, regardless of burn-in lot size. Class K PDA will be calculated on failures occurring during the second half of burn-in only.

C.5.9.5.3 Pattern failure option.

C.5.9.5.3.1 Pattern failure option, Class H. For Class H devices, when acceptance is based on pattern failures, all multiple device static failures at +25°C shall be analyzed to determine root cause. Multiple device failures with the same root cause (three or more, depending on lot size) will be considered a “pattern failure”. If a “pattern failure” is established, the lot will be rejected; otherwise, the lot will be accepted regardless of PDA. In all cases, lots with device failures that do not exceed the PDA are acceptable and do not require pattern failure analysis. The number of device failures with the same root cause that establish a “pattern failure” will be based on lot size, as follows:

Lot size (x)	Number of failures that establish a pattern
$x \leq 20$	3
$21 \leq x \leq 40$	4
$40 < x \leq 100$	5
$100 < x \leq 300$	6
$300 < x \leq 500$	11
$500 < x$	16

EXAMPLE 1: Lot size is 25 with four device static failures at +25°C.

If all four device static failures do not have the same root cause of failure (i.e., 3 or less failures with the same root cause), then no “pattern failure” exists and the passing 21 devices are acceptable.

If all four device static failures have the same root cause of failure, then a “pattern failure” exists and the lot should be rejected.

EXAMPLE 2: Lot size is 400 with 15 device static failures at +25°C.

The lot is acceptable (i.e., 10 percent PDA allows 40 device static failures).

EXAMPLE 3: Lot size 400 with 41 device static failures at +25°C.

If ten or less of the device static failures are due to the same root cause, then a “pattern failure” does not exist and the lot is acceptable.

If 11 or more of the device static failures are due to the same root cause, then a “pattern failure” has been established and the lot is unacceptable.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or non-screenable defects, the lot will be rejected.

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C.5.9.5.3.2 Pattern failure option, Class K. For Class K, when acceptance is based on pattern failures, all multiple device static failures at +25°C shall be analyzed to determine root cause. The lot will be stopped and placed on hold if:

a. Any two device static failures within the burn-in lot have the same root cause of failure (i.e., pattern failure established),or

b. The total number of device static failures in the burn-in lot exceeds 5 percent.

The lots may be reworked and recovered if the failure is due to:

a. A defect that can be effectively removed by rescreening the entire burn-in lot or,

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or non-screenable defects, the lot will be rejected.

C.5.10 Final electrical test.

a. Final electrical testing will include all parameters, limits, and conditions of test which are specifically identified in the device specification as final electrical test requirements. As a minimum, final electrical testing will include group A electrical test, table C-Xa, subgroups 1, 2, and 3 (plus subgroups 4, 7, and 9 as applicable).

b. Final electrical testing satisfies end-point electrical test requirements specified in the preceding test methods, and need not be duplicated.

C.5.11 Seal (fine and gross leak).

a. For Class K devices, the seal test may be performed in any sequence between the final electrical test and external visual, but it will be performed after all shearing and forming operations on the terminals.

b. For Class H devices, the seal test may be performed in any sequence between the constant acceleration/mechanical shock test (or PIND, if applicable) test and external visual, but it will be performed after all shearing and forming operations on the terminals.

c. For Class K and H devices, all device lots (sublots) having any physical processing steps that may affect the seal (e.g., solder dipping to the glass seal.) performed following seal or external visual will be retested for hermeticity and visual defects. This will be accomplished by performing, and passing, as a minimum, a sample seal test (method 1014 of MIL-STD-883) using an acceptance criteria of a quantity (accept number) of 45 (0), and an external visual inspection (method 2009 of MIL-STD-883) on the entire inspection lot (sublot). For devices with leads that are not glass sealed, and that have a lead pitch less than or equal to .050 inch (1.27 mm), the sample seal test will be performed using an acceptance criteria of a quantity (accept number) of 15 (0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample will be subjected to the fine and gross seal tests and all devices that fail will be removed from the lot for final acceptance.

C.5.12 Radiography for Class K devices. Radiographic inspection can be performed anytime after PIND.

C.5.12.1 Solder sealed devices. Solder sealed devices will be tested 100 percent in accordance with method 2012 of MIL-STD-883.

C.5.12.2 Non-solder sealed devices. Non-solder sealed devices will be tested 100 percent in accordance with method 2012 of MIL-STD-883, unless otherwise specified.

NOTE: Radiography should only be deleted if the manufacturer and customer determine it to be unapplicable; or, of limited value for a given design or technology.

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C.5.13 External visual screen. The final external visual screen will be conducted in accordance with, method 2009 of MIL-STD-883, after all other 100 percent screens have been performed. The manufacturer will inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116 (0). If one or more rejects occur in this sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for failed criteria and remove the failed devices from the lot. If the doubled sample also fails, the manufacturer will be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification will be no less than that used for the original inspection for the failed criteria.

TABLE C-IX. Device screening.

Test or inspection	MIL-STD-883		Requirement		Reference paragraph
	Method	Condition	Class K	Class H	
Preseal burn-in	1030		Optional	Optional	C.5.3
Non-destructive bond pull	2023		100 percent	Optional	C.5.4
Internal visual	2017		100 percent	100 percent	C.5.5
Temperature cycling	1010	C, 10 cycles	100 percent	100 percent	C.5.6
Mechanical shock or constant acceleration	2002 2001	B, (Y1 direction only) 3,000 g's, Y1 direction only	100 percent	100 percent	C.5.6
PIND	2020	Condition A shall be used for Class K, unless otherwise specified	100 percent	Optional	C.5.7
Pre-burn-in electrical test	In accordance with applicable device specification		100 percent	Optional	C.5.8
Burn-in	1015		100 percent	100 percent	C.5.9
Final electrical test	In accordance with applicable device specification		100 percent	100 percent	C.5.10
Seal (fine and gross)	1014		100 percent	100 percent	C.5.11
Radiographic	2012		100 percent	Optional	C.5.12
External visual screen	2009		100 percent	100 percent	C.5.13

C.6 CONFORMANCE INSPECTION AND PERIODIC INSPECTION

C.6.1 Description of conformance inspection and periodic inspection. Conformance inspection (CI) and periodic inspection (PI) is a series of tests and inspections performed on samples of devices that have passed screening. These tests and inspections are used to further verify the performance requirements on a sample basis. Sample testing is necessary due to the fact that many of these tests are either destructive, expensive, or time consuming. Group A is considered CI, whereas groups B, C, and D are considered PI. CI and PI will consist of the tests and inspections specified herein. Devices will not be accepted or approved for delivery until all applicable CI and PI requirements have been met. The acquiring activity may approve delivery if groups A, B, C1, C3, C4, C5 and D testing have been completed and group C2, steady-state life test, has commenced. The manufacturer will maintain traceability of all devices delivered to the acquiring activity prior to completion of CI and PI testing for the purpose of notification/recall in case of test failure.

C.6.2 General. CI and PI for a given device type is determined by selection of a requirements option flow (see Table C-X). The requirements option flow selected will determine the CI and PI requirements for the specific device manufactured. Where applicable, inspection lot sampling will be in accordance with Appendix F of this specification. Except where the use of final electrical test rejects or simulation samples (i.e., test coupons or test vehicles) are allowed, all devices will have been previously screened and subjected to and passed all final electrical tests. Successful completion of CI and PI for a given product assurance level will satisfy the requirements for any lower level device manufactured on the same certified line. If a lot is withdrawn in a state of failing to meet requirements and is not resubmitted, it will be considered a failed lot and reported as such.

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C.6.2.1 Inspection lots. Inspection lots consist of a quantity of devices of a single device type (required for group A) or several different circuit types (allowed for groups B, C3, and D tests only) in a single package type and lead finish submitted at one time for final acceptance. All devices within each inspection lot will be finally sealed in the same period not exceeding 13 weeks.

* C.6.2.2 Inspection lot formation. Inspection lot formation is required if the inspection lot is to be formally accepted by the lot related CI and PI testing of this specification (option 2 end-of-line inspection) or method 5005 of MIL-STD-883. If in-line process verification testing (option 1 in-line inspection) is used, inspection lot formation is not required.

NOTE: The device manufacturer has the right to elect not to use any solution or solvent identified within this specification, or related specifications, that has also been identified by the American Congress of Government Industrial Hygienists as being a potential or suspect carcinogen. Where the device manufacturer elects not to use a material, they shall notify the acquiring or qualifying activities and the customer in writing in clear, unambiguous language not subject to misinterpretation that this right has been exercised.

TABLE C-X. CI and PI summary.

Requirement	Reference	Option 1 (in-line)	Option 2 (end-of-line)
General	Paragraph	C.6.3	C.6.4
Group A (CI)	Paragraph	C.6.3.1	C.6.4.1
	Table	C-Xa	C-Xa
Group B (PI)	Paragraph	C.6.3.2	C.6.4.2
	Table	N/A	C-Xb
Group C (PI)	Paragraph	C.6.3.3	C.6.4.3
	Table	C-Xc	C-Xc
Group D (PI)	Paragraph	N/A	C.6.4.4
	Table	N/A	C-Xd

C.6.2.3 Sample selection. The number of hybrid microcircuits to be tested will be chosen (independent of lot size) by the manufacturer in accordance with the applicable requirements of options 1 or 2 herein. Initial samples and resubmitted samples, when applicable, will be randomly selected from the inspection lot. Lot acceptance is based on an accept number of zero. If a failure occurs, the failed subgroup or test may be performed once using double the sample size, or 100 percent, with zero failures allowed. For group C inspection, limited sample quantities may be used to meet the requirements of C.6.1 for production start-up. When limited sampling is used for start-up, a subsequent full sample, group C test will be performed within 6 months of initial group C or prior to exceeding the limited usage requirements of C.6.3.3.1.c, whichever comes first.

C.6.2.4 End-point. Electrical end-points will be measured and recorded when applicable.

C.6.2.5 Data. Test results will be recorded by inspection lot identification code (date code), or each inspection lot, when applicable. For in-line group B inspections, where inspection lots are not applicable, data records or logs will be maintained and available for review by the qualifying and acquiring activities. A summary of attributes results for all tests and measurements shall be part of the test report unless 100 percent recorded data is provided. Variable data will be provided when required by the device specification.

C.6.2.6 Non-functional samples. Electrically rejected devices from the same inspection lot may be used in all subgroups when end-point measurements are not required, provided that the devices have been subjected to all device screening conditions through burn-in.

C.6.3 Option 1 (in-line inspection). Option 1 CI and PI will be satisfied by in-line inspections and tests in accordance with C.6.3.1, through C.6.3.4.

C.6.3.1 Group A electrical testing. Group A electrical testing will be performed in accordance with table C-Xa, C.6.3.1.1 through C.6.3.1.4 and the applicable device specification.

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C.6.3.1.1 Group A general requirements. Group A subgroups will, as a minimum, include the final electrical testing subgroups 1, 2, and 3 (plus subgroups 4, 7, and 9, as applicable) and any other subgroups required by the device specification. Each inspection lot or sublot will be tested. A procedure for performing group A inspection in accordance with one or more of the following methods will be available for review by the qualifying activity. Each of these three methods are equivalent, therefore, the manufacturer may choose to use any of the three.

a. Sampling: A single sample may be used for all subgroup testing. Where the required size exceeds the lot size, 100 percent inspection will be allowed.

b. Sequence of test: Group A testing by subgroup, or within subgroups, may be performed in any sequence after subgroup 1, or alternate subgroups, (see method 1015 of MIL-STD-883) are performed.

C.6.3.1.2 End-of-line sample testing.

a. Production performs all required final electrical screening tests.

b. Quality assurance or quality designate randomly pulls samples in accordance with table C-Xa and performs acceptance testing.

C.6.3.1.3 In-line sample testing. Test samples for each individual group A subgroup will be randomly selected from the inspection lot after 100 percent screening of that subgroup (or subgroups, in the event that multiple subgroups are tested at the same temperature in sequence with the same test program). All devices in the inspection lot or sublot will be available for selection as a test sample and a fully random sample will be selected in accordance with table C-Xa from the total population of devices. In addition, a different person will check the entire test setup and verify the use of the correct test program prior to testing the group sample.

C.6.3.1.4 In-line verification testing. In-line verification testing, generally, is performed in conjunction with final electrical tests at screening which satisfy the requirements of group A testing and need not be repeated. Therefore, if the screening tests are performed with the verification defined here, the requirements of group A have been met.

a. For each test setup (and operator for manual testing) production will test a correlation unit to ensure that the accuracy requirements of MIL-STD-883 are being met.

b. Testing will be performed using the verified setup.

c. At the completion of testing (or at least once each week) or following a change of operators for manual testing, a different person designated by quality assurance verifies the production testing by:

(1) Visually inspecting to confirm that the correct test fixture, equipment, software, and procedures were used.

(2) Review actual testing or data of a controlled, known good, device utilizing the fixtures, equipment, software, and procedure(s) that were used by production. The device type being tested will be of the same device type as the known good device, or will be similar to the known good device per the criteria of section 6.4.43 of this specification. Variables data for all applicable group A tests at +25°C will be read and recorded for the controlled unit. This data will be maintained with the lot or traceable to the lot.

(3) Failure of the verification test will, as a minimum, require engineering to perform a detailed review of hardware, software, setup, and parts. If the engineering review does not locate the problem, the verification unit will undergo failure analysis. The appropriate corrective action shall be taken based on the failure analysis results. The entire group of devices being considered for acceptance at the time of the failure may then be retested for the appropriate subgroup(s) acceptance, one time only, by repeating in-line verification testing. If the failure analysis does not specifically locate the problem, the lot may be reconsidered for acceptance, one time only, for 100 percent retesting of all of the devices to all of group A requirements and by repeating in-line verification testing.

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TABLE C-Xa. Group A electrical test.

Subgroup	Parameters	Quantity (accept number)
1	Static test at +25°C	116 (0)
2	Static tests at maximum rated operating temperature	76 (0)
3	Static tests at minimum rated operating temperature	45 (0)
4	Dynamic tests at +25°C	116 (0)
5	Dynamic tests at maximum rated operating temperature	76 (0)
6	Dynamic tests at minimum rated operating temperature	45 (0)
7	Functional tests at +25°C	116 (0)
8	Functional tests at maximum and minimum rated operating temperatures	76 (0)
9	Switching tests at +25°C	116 (0)
10	Switching tests at maximum rated operating temperature	76 (0)
11	Switching tests at minimum rated operating temperature	45 (0)

C.6.3.2 Group B inspection. Group B inspection will be satisfied by performing in-line inspection sample monitoring as follows. Electrically rejected devices or test vehicles or coupons may be used in all subgroup tests in lieu of actual product.

C.6.3.2.1 Physical dimensions. Randomly select devices from devices at final inspection such that, as a minimum, two devices of each package configuration presented for inspection are inspected each month. Confirm that all critical dimensions affected by the assembly process (e.g., package length, width, height, pin length, etc.) meet the requirements of the device specification. Critical dimensions unaffected by assembly processes may be inspected at final visual inspection or as a part of incoming (receiving) inspection.

C.6.3.2.2 Resistance to solvents. Each inspection lot of marking ink will be tested prior to acceptance in accordance with method 2015 of MIL-STD-883. This series of tests will be performed on each type of surface which is used as the marking surface on completed devices (e.g., silver plate, abraded nickel plate, non-abraded nickel plate.). One piece of each surface type will be tested in each solvent. Each week one device or element (lid or package) representative of each of the marking surfaces of each device marked during the week will be tested in accordance with method 2015 of MIL-STD-883, except that only "solvent D" is required.

C.6.3.2.3 Internal visual and mechanical. Internal visual and mechanical inspection will be performed at pre-seal visual inspection in accordance with the requirements of method 2014 of MIL-STD-883. As a minimum, one device of each device type received at pre-seal visual inspection each month will be inspected.

C.6.3.2.4 Bond strength. Wire bond strength in-line inspection will be performed as a part of wire bond certification and in accordance with method 2011 of MIL-STD-883. Each wire bond process (e.g., thermosonic gold, ultrasonic aluminum, thermal compressions gold) will be tested weekly. Where more than one machine exists for a specific process, the test sample will be rotated between machines such that all machines are tested at least once during each 13 week period when in operation. At the time of certification, an additional minimum 10 wires total (15 wires for Class K) will be bonded in the certification sample part(s). After completion of certification bond pulls, the parts with the additional 10 wires (15 wires for Class K) intact will be preconditioned for 1 hour at +300°C minimum in either air or an inert atmosphere followed by destructive pull tests. Bond strength requirements (i.e., minimum pull forces) will be as specified in table C-Xb-1. No failures are allowed.

C.6.3.2.5 Die shear. Die shear testing will be performed on two devices as a part of group C inspection (i.e., first lot and any element attach changes). Die shear testing during group C will be performed in accordance with method 2019 of MIL-STD-883.

C.6.3.2.6 Solderability. Solderability testing will be performed as a part of incoming inspection (i.e., package evaluation) as follows:

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Packages will be temperature aged to one of the following conditions prior to performing the solderability test.

6 ±0.5 hours at T_A = +250°C, ±10°C

22 ±1 hours at T_A = +200°C, ±8°C

160 ±8 hours at T_A = +150°C, ±6°C

When the device process flow includes an operation in which the package lead finish is changed prior to delivery of the device (i.e., a solder coating is applied), this operation will be performed on the package evaluation sample packages subsequent to the temperature aging. Following the temperature aging (and the lead finish application, if applicable), the sample packages will be solderability tested in accordance with method 2003 of MIL-STD-883 including an 8 hour (±15 min) steam aging.

C.6.3.2.7 Seal. Seal tests will be performed in accordance with method 1014 of MIL-STD-883. One-hundred percent testing will be performed on all devices between final electrical test and external visual.

* C.6.3.3 Group C inspection.

a. For Class H processes and products, Group C inspection will be performed only on the first inspection lot submitted for inspection and as required to evaluate or qualify changes. Group C inspection will be performed in accordance with table C-Xc under the PI column or the QML column and as outlined herein. For QML qualification, refer to section C.7 herein of this specification.

b. For Class K processes and products, Group C inspection will be performed on the first inspection lot submitted for inspection and as required to evaluate or qualify changes. Group C inspection will be performed periodically within a maximum of five years for periodic re-qualification. The qualifying or acquiring activity may shorten the periodicity requirement as needed for certain products based upon program needs, product failures, etc. Group C inspection will be performed in accordance with table C-Xc under the QML column and as outlined herein. For QML qualification, refer to section C.7 herein of this specification. Periodic re-qualification shall not require Subgroup C5 testing. Subgroup C4 shall only require two samples for testing regardless of quantity of wirebonds or elements contained in the devices and may be performed on Class K screened products. These samples may contain rework. Except for these differences, all other requirements and allowances of initial qualification and change qualification shall apply for periodic re-qualification of Class K processes and products.

NOTE: The qualifying activity may approve alternate test plans for small lots of devices for group C inspection.

* C.6.3.3.1 General.

a. Group C sample selection: Samples for group C will be drawn from the first inspection lot submitted and also periodically for Class K processes and products in accordance with the requirements of paragraph C.6.3.3.

b. Subgroup sampling: Subgroup 1 samples (or electrical rejects or mechanical samples, see C.6.2.6) will be used for the subgroup 3 and subgroup 4 tests.

c. Limited usage samples: (See C.6.2.3 for group C production start-up). A minimum of five devices will be subjected to subgroup 2 when all three criteria listed below are met. A sample of 22 devices shall be selected otherwise.

(1) A maximum of 500 devices in a single order against a single drawing (SMD or contractor prepared document).

(2) A maximum of 2,000 devices acquired against a single drawing (SMD or contractor prepared document) on a given equipment-acquisition contract or program.

(3) A maximum of 2,000 devices acquired against a single drawing (SMD or contractor prepared document) during a 12 month period for a given device and manufacturer.

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d. Tests will be performed in the order specified in table C-Xc.

TABLE C-Xb. Group B testing (option 2 only).

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	K	H		Method	Condition		
1	X	X	Physical dimension	2016		2(0)	
2			Not used				
3	X	X	Resistance to solvents	2015		3(0)	
4	X	X	Internal visual and mechanical	2014		1(0)	C.6.4.2.1
5	X	X	Bond strength: a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2(0)	C.6.4.2.2
6	X	X	Die shear strength	2019		2(0)	C.6.4.2.3
7	X	X	Solderability	2003	Solder temperature +245°C ± 5°C	1(0)	C.6.4.2.4
8		X	Seal: a. Fine b. Gross	1014	 A or B C or D	15(0)	C.6.4.2.5

TABLE C-Xb1. Bond strength requirements.

Gold or aluminum wire diameter, X (inches)	Minimum bond strength (grams)
X < 0.001	0.5
X = 0.001	1.0
0.001< X ≤ 0.003	(Method 2011 of MIL-STD-883, table I, post-seal requirement) minus 1 gram
0.003 < X	(Method 2011 of MIL-STD-883, figure 2011-1, post-seal requirement) minus 10 percent

C.6.3.3.2 Wire bond strength for option 1 PI product qualification. Two devices minimum will be tested to assure conformance to the applicable requirements of method 2011 of MIL-STD-883. Sample criteria will be based on the number of wires pulled using a sample size (accept number) of 22 (0) for Class H and a sample size (accept number) of 45 (0) for Class K devices. If the 45 (0) requirement for Class K cannot be met with two devices then all wires in two devices will be pulled with a minimum of 22 wires being pulled with zero failures. Sample wires will include one wire from each type transistor, diode, capacitor, and resistor chip; three wires from each type of integrated circuit; and five wires from package leads, as applicable. For test conditions F and H, test three dice for each method of interconnection, or all flip chips and beam lead dice, if less. The minimum allowable bond strength will be the post-seal bond strength requirements of method 2011 of MIL-STD-883.

C.6.3.3.3 Element shear for option 1 PI product qualification. The element (die/chip) shear test will be performed to a quantity (accept number) 22 (0) of the elements in the devices, or all elements in the two sample devices, whichever is less. The shear sample will be uniformly divided among all element types (or all elements, if less) in the device and will be performed in a minimum of two devices. The sample will include typical resistor, capacitor, integrated circuit, and discrete semiconductor elements. Alternative element shear may be conducted in accordance with C.7.5.4.12.1.

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C.6.3.3.4 Qualification to electrostatic discharge sensitivity (ESDS) classes. Initial qualification to an ESD class or re-qualification after a major change shall consist of determining the ESD level in accordance with any one of the four following options.

(1) Testing the devices to Subgroup 5 of Table C-Xc using method 3015 of MIL-STD-883 to determine the actual ESD classification designators in accordance with 3.9.5.8.2.

(2) Testing the devices to Subgroup 5 of Table C-Xc using method 3015 of MIL-STD-883 using alternate testing method to test once at 250 V to determine ESD classification designator 0 or 1A IAW 3.9.5.8.2.

NOTE: If any device(s) fail at 250 V, it is classified as Class 0. If all devices pass at 250 V, it is classified as Class 1A.

(3) Classifying the hybrid to the lowest electrostatic voltage class level of the active devices ESDS listed in accordance with MIL-PRF-38535 that are accessible to leads of the device by analysis. Support data (from device testing or IC manufacturers' ESD results) will be retained by the hybrid manufacturer for all device types compliant with this specification.

(4) Classify the hybrid device as Class 0 (see 3.9.5.8.2 herein) without performing the ESD testing.

C.6.3.3.5 Resistance to soldering heat. Products qualified or re-qualified after 9 September 2009 require testing to method 2036 of MIL-STD-883 unless called out by contract, resistance to soldering heat testing is to be done for table C-Xc group C PI testing prior to any other subgroup 1 testing. This test is performed at qualification/requalification or design changes which may affect this test. The manufacturer shall determine for each device design the applicable conditions from test method 2036 of MIL-STD-883 that are appropriate for the mounting conditions and, assure by testing or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.

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TABLE C-Xc. Group C testing.

Subgroup	Class		Test	MIL-STD-883			Quantity (accept number)	Reference paragraph
				Method	Conditions			
	K	H			PI	QML		
1	X	X	Resistance to Soldering Heat	2036	1/	N/A	5 (0)	C.6.3.3.5
	X	X	External visual	2009				
	X	X	PIND 2/	2020	N/A	A 3/		C.7.5.4.1
	X		Temperature cycling	1010	C, 20 cycles	C, 100 cycles		C.7.5.4.2
		X	Temperature cycling	1010	C, 10 cycles	C, 100 cycles		C.7.5.4.2
	X	X	Mechanical shock	2002	B, Y1 direction 4/	B, Y1 direction		C.7.5.4.3
	X	X	Constant acceleration	2001	3,000 g's, Y1 direction 4/	5,000 g's, Y1 direction		C.7.5.4.4
	X	X	Random vibration 5/	2026	N/A	F		C.7.5.4.5
	X	X	Seal (fine and gross) 6/	1014				
	X	X	PIND	2020	N/A	A, 1 pass 3/		C.7.5.4.1
	X	X	Visual examination	1010				C.7.5.4.6
	X	X	End-point electrical	7/				C.7.5.4.7
2	X	X	Steady-state life test	1005	1,000 hours at +125°C or equivalent in accordance with method 1005	1,000 hours at +125°C or equivalent in accordance with method 1005	8/ 22 (0) or 5 (0)	C.7.5.4.8
	X	X	End-point electrical	7/				C.7.5.4.7
3	X	X	Internal gas analysis	1018			9/ 3 (0)	C.7.5.4.9
4	X	X	Internal visual	2017	Option 1 only		9/ 2 (0)	C.7.5.4.10
	X	X	Wire bond strength	2011	Option 1 only			C.7.5.4.11, C.6.3.3.2
	X	X	Element shear	2019 or 2027	Option 1 only			C.7.5.4.12, C.6.3.3.3
5 10/	X	X	ESD a. End point electrical b. ESDS c. End point electrical	3015	Group A-1 Group A-1	N/A	3 (0)	C.6.3.3.4

See footnotes at end of table.

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TABLE C-Xc. Group C testing - Continued.

1/ This test is performed at qualification/requalification or design changes which may affect this test. The manufacturer shall determine for each device design the applicable conditions from test method 2036 of MIL-STD-883 that are appropriate for the mounting conditions and, assure by testing or through their assembly processes, that the part is subjected to an equivalent time/temperature stress.
2/ Manufacturer may choose to do PIND before temperature cycling at their option.
3/ Condition B may be used when specified in the applicable device specification or acquisition order.
4/ Either mechanical shock or constant acceleration can be performed for periodic inspection (PI).
5/ This test is only required on devices that contain magnetics, stacked elements, insulated wires, flex circuit, or high profile elements that exceed a 2 to 1 ratio of the height to the width. As an option, it is allowable to perform random vibration before mechanical shock or constant acceleration.
6/ Leak testing for C1 may be performed as specified or at the end of C1 testing.
7/ In accordance with the applicable device specification.
8/ When group C, subgroup 2 is being performed for QML qualification or limited PI, a sample size (accept number) of 5 (0) may be used. For class I changes the manufacturer shall use the required sample size for PI.
9/ Subgroups 3 and 4 samples will have received subgroup 1 environmental exposure. Subgroup 3 samples may be used to perform subgroup 4 tests.
10/ Group C5 may be performed after C1 and before C3.

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C.6.3.4 Nonconformance. Should failure occur in any of the above in-line inspections, an analysis to determine cause will be performed and corrective action, as necessary, will be imposed. The cause of failure, applicable corrective action, and disposition of product affected by the failure will be documented. This documentation will be available for qualifying and acquiring activity review.

C.6.4 Option 2 (end-of-line). Option 2 CI and PI will be satisfied by end-of-line inspections and tests in accordance with C.6.4.1 through C.6.4.5.

C.6.4.1 Group A electrical testing. Group A testing will be performed in accordance with table C-Xa, C.6.3.1 through C.6.3.1.4, and the applicable device specification.

C.6.4.2 Group B inspection. Group B inspection will be performed on each inspection lot for each package type and lead finish in accordance with table C-Xb and C.6.4.2.1 through C.6.4.2.5.

C.6.4.2.1 Internal visual and mechanical. The criteria for internal visual and mechanical examination will be the general requirements for design and construction, the requirements of the device specification and confirmation that the actual device construction is in accordance with the design documentation on file.

C.6.4.2.2 Bond strength. Destructive wire bond pull tests will be performed in accordance with method 2011 of MIL-STD-883 and as follows. Testing may be accomplished in-line anytime after device wire bonding. Coupons which simulate actual production processes and materials may be used in lieu of actual product.

a. Two devices will be pre-conditioned and tested.

b. Sample devices will be pre-conditioned for one hour minimum at +300°C minimum in either air or an inert atmosphere.

c. Sampling criteria will be based on the number of wires pull tested using a sample size (accept number) as follows:

   (1) Class H: 22 (0) wires, 11 wires each device (or all wires, if less).

   (2) Class K: 44 (0) wires, 22 wires each device (or all wires, if less).

d. Sample wire locations will include wires from the following device locations, as applicable:

   (1) One wire from each type transistor, diode, capacitor, and resistor chip/die.

   (2) Three wires from each type integrated circuit.

   (3) Five wires connecting to package leads.

e. The minimum allowable bond strength will be in accordance with table C-Xb-1.

C.6.4.2.3 Die shear strength. The element (die/chip) shear test will be performed to a quantity (accept number) of 22 (0) of the elements in the devices, or all elements in the two sample devices, whichever is less. The shear sample will be uniformly divided among all element types (or all elements, if less) in the device and will be performed in a minimum of two devices. The sample will include typical resistor, capacitor, integrated circuit, and discrete semi-conductor elements. Alternative element shear may be conducted in accordance with C.7.5.4.12.1.

C.6.4.2.4 Solderability. At least 15 leads (or all leads, if less) will be randomly selected, identified, and tested.

C.6.4.2.5 Seal (fine and gross). This test is not required if the 100 percent seal test screening is performed between the final electrical test and external visual.

C.6.4.3 Group C inspection. Group C inspection will be in accordance with C.6.3.3 except table C-Xc, subgroup 4 tests are not required.

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C.6.4.4 Group D inspection. Group D inspection will be performed on the first inspection lot submitted, and at intervals not exceeding 26 weeks, for additional inspection lots (except as modified in C.6.4.4.4 and C.6.4.4.5 herein). Group D inspection will be performed in accordance with table C-Xd and C.6.4.4.1 through C.6.4.4.5.

NOTE: Group D testing is not required when package evaluation has been performed at incoming inspection.

C.6.4.4.1 Samples. Sealed empty packages that have been subjected to the handling and stress conditions of screening may be used for group D testing.

C.6.4.4.2 End-point electrical measurements. End-point electrical measurements are not required.

C.6.4.4.3 Lead integrity. Lead integrity testing will be performed on 15 leads minimum, or all leads if there are fewer than 15 leads for each device package.

C.6.4.4.4 Subgroup 3. Verify complete package (may verify case and cover separately) for compliance with subgroup 3. Corrosion in the internal cavity area is not cause for rejection. This test is performed one time for Class H and at 26 week intervals for Class K unless a change in material or plating is made.

C.6.4.4.5 Subgroup 4. For metal cases with leads separated by an insulator, measure insulation resistance between the metal body of the case and the leads that are isolated from the case. This test does not apply to non-metallic cases. This test will be performed once for Class H unless a change in insulator material is made, and on every group D lot for Class K.

TABLE C-Xd. Group D package related tests.

Subgroup	Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
		Method	Condition		
1	Thermal shock	1011	C	5(0)	
	Stabilization bake	1008	+150°C, 1 hour	5(0)	
	Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carrier) B1 for rigid leads (pin grid array leads)	1(0)	C.6.4.4.3
	Seal: a. Fine b. Gross	1014	 A or B C or D	5(0)	
2	Not used				
3	Salt atmosphere	1009	A	5(0)	C.6.4.4.4
4	Metal package isolation	1003	600 V dc, 100 nA maximum	3(0)	C.6.4.4.5

C.6.4.5 Nonconformance. Lots which fail subgroup requirements of groups A, B, C, and D may be resubmitted in accordance with the provisions of C.6.4.5.1. A failed lot which is reworked, or is rescreened, (resubmittal to inadvertently missed process steps is not considered a rescreen) may not be resubmitted to the failed subgroups (and will be counted as a failure) for periodic groups B, C, and D PI coverages. The lot may be resubmitted only to the failed subgroup to determine its' own acceptance. If a lot is not resubmitted, or fails the resubmission, the lot will not be shipped and the compliant marking and all references to this document will be removed.

C.6.4.5.1 Resubmission of failed lots. Resubmitted lots will be kept separate from new lots and will be clearly identified as resubmitted lots. When any lot submitted for CI and PI fails any subgroup requirement of groups A, B, C, and D tests, it may be resubmitted once for that particular subgroup at double the sample size with zero failures allowed. A second resubmission using double the initial sample size with zero failures allowed is permitted only if failure analysis is performed to determine the mechanism of failure for each failed device from the prior submissions and it is determined that failure is due to:

a. A defect that can be effectively removed by rescreening the entire lot, or

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or nonscreenable defects, the lot will not be resubmitted.

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C.7 QUALIFICATION

C.7.1 Description of qualification. The following criteria have traditionally been used to qualify all processes and materials used in the manufacture of chip and wire devices. It may not, however, be adequate for all, or new, technologies, in which case it should be used as a starting point for developing a qualification program. These criteria are intended to be used to characterize all process and materials used in the manufacture of the device. These criteria will be used to determine the acceptability of the processes and materials. All parts built using processes and materials that have successfully completed characterization and have been verified by the qualifying activity are considered qualified.

C.7.2 Rework qualification. Devices containing any unqualified rework will not be shipped until the rework has been successfully qualified. The rework and repair provisions will apply.

C.7.2.1 Qualification of rework. If any rework is to be qualified, and unless otherwise allowed, the manufacturer will build a qualification lot of reworked devices in which certified rework processes are performed. Standard evaluation circuits may be used. Qualification of rework by this method will require qualifying activity approval of the test plan and authorization to test (ATT) prior to assembly of the lot.

C.7.2.2 Delid/relid rework qualification procedures. If delid/relid rework is to be qualified, a qualification lot of delidded/relidded devices will be assembled that includes adequate devices for five qualification samples plus reserve units. Qualification of two or more delid/relid cycles require that the samples be delidded and relidded N+1 times to qualify "N" delid/relid cycles. The N+1 delid/relid rework operations will be performed on qualification devices that have been fully screened. In addition to the original screen, there will be N screens performed for N+1 delid/relid operations. The final screen will occur after the last delid/relid cycle.

NOTE: One delid/relid qualification will require no additional delid/relid operation.

C.7.2.3 Alternate qualification procedures for die/wire bond rework. The manufacturer may elect to review the initial production lot(s) from which qualification samples are selected for the occurrence of certified rework processes. The devices containing the rework to be qualified will be among those selected for qualification. If the amount of rework that was performed does not meet the sample size requirements, then additional die/bond rework will be performed on the selected rework samples, or more rework samples, to meet the minimum sample size requirements. If the initial qualification does not cover all certified rework, then subsequent production lot(s) will be reviewed for the occurrence of the unqualified rework until all certified rework is qualified. Delid/relid rework will not be qualified by these procedures.

C.7.3 Qualified manufacturers list (QML) qualification lot. The manufacturer may elect to perform the QML qualification in accordance with C.7.5 on an inspection lot of shippable product; or, the manufacturer may choose to build a lot of devices specifically for QML qualification and test them in accordance with C.7.5. Devices specifically built for QML qualification may either be actual product or standard evaluation circuits. Any actual products from the qualification lot are shippable as a compliant product after successful completion of qualification tests, subgroups 1, 3, 5, and 7 of table C-Xb, and table C-Xd tests.

* C.7.4 Qualification test requirements. QML qualification will be accomplished by successful performance of group C testing to QML requirements as specified herein. For options 1 and 2, the group C testing will be the QML qualification tests and inspections specified in table C-Xc, under the QML column.

NOTE: For Class K devices qualified after 06/03/2020, requalification per Table C-Xc under the QML column will be required no later than five years after original qualification date and no later than every five years thereafter. For Class K devices qualified prior to 06/03/2020, requalification per Table C-Xc under the QML column will be required no later than 06/03/2025 and no later than every five years thereafter.

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C.7.5 QML-38534 qualification. All tests, test methods, test conditions, and limits will be in accordance with MIL-STD-883 and as specified herein. If a qualification lot is withdrawn due to: (1) failing to meet qualification requirements or (2) lack of failure analysis, corrective action, and (3) no retesting is performed, the certification of the process or material (or both) to be covered by that qualification will be removed by the qualifying activity.

NOTE: The device manufacturer has the right to select to not to use any solution or solvent identified within this specification, or related specifications, that has also been identified by the American Congress of Government Industrial Hygienists as being a potential or suspect carcinogen. Where the device manufacturer elects not to use a material, they shall notify the acquiring or qualifying activities and the customer in writing in clear, unambiguous language not subject to misinterpretation that this right has been exercised.

C.7.5.1 Qualification eligibility. All processes to be qualified, and which are to be included on QML-38534, shall have been certified by the qualifying activity. Additional processes and materials may be added to the baseline flow using E.5 (major change) herein, with qualifying activity approval.

C.7.5.2 Test samples. Devices used for qualification will have been assembled using certified process (or as allowed by the Qualifying Activity) and screened in accordance with the applicable sections of C.6 herein. Qualification tests will be performed at facilities which have a laboratory suitability granted by the qualifying activity or approved by the manufacturer's TRB. DLA Land and Maritime Form VQH-42H, "Device Product Baseline", or its equivalent, will be used to baseline the specific processes and materials used in the qualification device. The screening level used in the qualification parts (e.g. class H or K or company defined) is the minimum baseline screening for qualified parts. For example, devices screened to class H requirements and qualified, cover class K devices, however class K screened devices that have been qualified have extra screening and do not cover class H devices unless the rejects were zero (e.g. PIND, non-destructive bond pull, Class K internal visual, and x-ray).

C.7.5.2.1 Standard evaluation circuits. The manufacturer may elect to design and build a functional standard evaluation circuit (device) in lieu of utilizing actual product. If qualification is to be performed on a lot of devices built specifically for QML qualification, the device will be representative of the physical complexity of the product that will be covered by its testing. Standard evaluation circuits will not be used for group C PI product qualifications.

C.7.5.2.2 Sample selection. The sample size for each test is listed in the corresponding subgroups of the group C table C-Xc. Except for designated rework and nonfunctional devices, test samples will be randomly selected from the inspection lot. The manufacturer will retain a sufficient number of test devices from the lot to designate reserve samples.

C.7.5.2.3 Rework samples. For approval of rework qualification, the rework sample will be prepared in accordance with the manufacturer's baselined rework procedure. Three out of five devices tested in group C, subgroup 1 will have undergone the rework to be qualified. Two out of the three (3 (0)) devices tested in group C, subgroup 3 will contain the rework to be qualified. One of the two devices tested in group C, subgroup 4 will contain the rework to be qualified. The die and wire sample size requirements of C.7.5.4.11 and C.7.5.4.12 will be applied to reworked wire bonds and replaced die. Each rework method will be considered a different process.

C.7.5.2.4 Nonfunctional samples. Electrical rejects from final electrical testing in screening can be used in any subgroup of qualification tests where electrical testing is not required (e.g., for group C3, the rejects shall be subjected to group C1 prior to testing to group C3).

C.7.5.2.5 Disposition of samples. Samples destructively tested during qualification testing will be submitted to the qualifying activity with the qualification test report. Other devices in the qualification inspection lot will be properly disposed of.

C.7.5.3 Test failures.

C.7.5.3.1 Resubmission of failed samples or lots (or both). Resubmission of failed samples, or additional samples from the same production lot, are not allowed unless such failures are due to equipment or operator errors in accordance with Appendix A. Notification of the qualifying activity is required.

C.7.5.3.2 Failures. All test failures will be reported to the qualifying activity, along with (if applicable) the resulting failure analysis and corrective actions needed to assess qualification status or alternatives.

C.7.5.4 Technology capability verifications. Table C-Xc under the QML column and C.7.5.4.1 through C.7.5.4.12 detail the testing requirements for qualification for both Class H and Class K devices.

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C.7.5.4.1 PIND. The devices will show no evidence of loose particles. Any device showing loose particles when tested as specified herein will be analyzed. Failure of PIND will not jeopardize qualification provided the manufacturer demonstrates that the loose particle control is established and random samples, from product fabricated using the baselined process, are PIND tested after corrective action implementation. These random samples will have been screened (see C.5). The retest requirements will be determined based on the nature of the changes made as a result of the corrective action. Compliant Class H will receive 100 percent PIND screening until the manufacturer demonstrates to the qualifying activity that these requirements are met.

C.7.5.4.1.1 Loose particle recovery. The loose particles that caused the failures will be recovered and analyzed for the cause and source. If the analysis fails to locate the particles causing failure, the device will be carefully delidded and examined in an attempt to locate the particles. Captured particles will be evaluated at 30X minimum and the offending portion of the process will be identified and corrected.

C.7.5.4.2 Temperature cycling. Temperature cycling will be done in accordance with method 1010 of MIL-STD-883.

C.7.5.4.3 Mechanical shock. When QML qualification is being performed, constant acceleration is not an option in place of mechanical shock. Both tests are required for qualification.

C.7.5.4.4 Constant acceleration. For QML qualification, a stiffener plate (e.g., .125 inch (3.18 mm) aluminum) may be attached to the base of the package to prevent damage due to "oil canning" of the package.

C.7.5.4.5 Random vibration. When applicable, this test will be in accordance with the procedure given within method 2026 of MIL-STD-883.

C.7.5.4.6 Visual examination. The visual examination will be in accordance with the procedure of method 1010 or 1011 of MIL-STD-883.

C.7.5.4.7 Electrical requirements. Electrical end-points will be measured (and recorded when required) before starting and after completion of all tests in subgroups 1 and 2 of group C tests. Data from group A, or final electrical test, may be used as the initial end-point electrical before starting subgroup 1 and 2. Electrical end-point limits, life test conditions, and intermediate measurement requirements will be specified as required by the applicable device specification. Test samples which require variable data will be serialized prior to tests.

C.7.5.4.8 Steady-state life test. Steady-state life testing will be performed on each initial lot of each device type. If group C, subgroup 2 testing is being performed for QML qualification only, the sample size will be five with zero failures allowed. In addition, if group C2 testing is being performed for QML qualification only and life test has previously been completed, a 1,000-hour bake at +150°C followed by end-point electrical testing may be performed in lieu of steady-state life testing.

C.7.5.4.9 Internal gas analysis. An internal gas content sample of three devices (zero failures) will be selected from the subgroup 1 sample. The use of screened electrical rejects, or representative mechanical samples, is permissible provided these samples have seen, as a minimum, the environmental exposures required in subgroup 1 (e.g., temperature cycle or thermal shock, mechanical shock or constant acceleration, and seal tests as applicable). The internal gas analysis shall meet the requirements of method 1018 of MIL-STD-883.

C.7.5.4.10 Internal visual. In addition to the criteria of method 2017 of MIL-STD-883, this inspection will verify that no damage has occurred to, and no contamination is present on, the elements and substrate. Manufacturer may disregard damage done by delidding and shall be recorded.

* C.7.5.4.11 Wire bond strength for QML qualification. Two devices minimum will be tested to ensure the post-seal bond strength requirements of method 2011 of MIL-STD-883. The bond strength test will be performed on a sample size (accept number) of 15 (0) bond wires for each wire bond process (including each rework method outlined in C.7.5.4.11.1 as a separate process) material (wire metallization and size), and bonding surface (posts, substrate metallization, and die pad) present in the device. Each 15 piece sample of wires will contain an even distribution of all wire sizes that can be qualified by that sample. No failures will be allowed. Additional devices will be added, if necessary, to meet the required wire sample size. For periodic requalification of Class K processes and products as required in paragraph C.6.3.3, only two devices shall be tested regardless of the quantity of wirebonds contained in the devices. The test wires will be predesignated.

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C.7.5.4.11.1 Wire bond strength for QML rework qualification. Each of the following wire bond rework methods will be considered as separate methods requiring QML qualification:

a. Gold ball bonds on substrate wires.

b. Gold ball bonds on crescent bonds.

c. Gold ball bonds on top of gold ball bonds.

* C.7.5.4.12 Element shear for QML qualification. Two devices minimum will be tested to ensure the die shear strength requirements of method 2019 of MIL-STD-883. The die shear test will be performed to a quantity (accept number) of 5 (0) elements for each element attach process (including element replacement as a separate process) and material present in the device. The materials considered will include the attach medium, element backing, and substrate/package attach area surface. Each five piece sample of elements will contain an even distribution of all element sizes that can be qualified by that sample. No failures will be allowed. Additional devices will be added if necessary to meet the required element sample size. For periodic requalification of Class K processes and products as required in paragraph C.6.3.3, only two devices shall be tested regardless of the quantity of wirebonds contained in the devices. The test elements will be predesignated.

C.7.5.4.12.1 Alternative to element shear testing. The manufacturer may utilize method 2027 of MIL-STD-883 to test the strength of organic and solder/alloy attachments on selected elements, except that the accept/reject criteria shall be based on an acceleration on the element of 50,000 g's in the Y1 direction (i.e., the minimum acceptable pull strength shall be 50,000 times the weight of the element).

NOTE: This alternative test is only appropriate for elements whose element thickness or mass is small in proportion to the area of attach (e.g., 10 mil thick GaAs die). The acceptance level is more severe than die shear testing for many element types. In cases where the element is relatively massive compared to the attachment area (e.g., tantalum capacitors), this method will give a false indication of die attach strength, pass, or fail.

C.7.5.4.13 Marking Qualification.

a. For ink marking, the qualification sample size shall be 3 devices, marked and cured. If samples are sealed during marking process, the marking cure temperature shall not exceed the epoxy cure temperature.

b. For laser marking, qualification lots shall consist of 3 pieces of every combination of metallization plating/underplating and laser marking method. Samples shall be subjected to the following tests in the order given with no failures: salt atmosphere (TM 1009), external visual (TM 2009), and fine and gross leak testing (TM 1014). The loss in plating material shall be measured to ensure minimum plating thicknesses are satisfied.

C.7.5.4.14 Marking rework qualification. Mark and cure part, then use process to remove marking. If package is sealed, process temperature shall not exceed epoxy cure temperature. For abrasive removal processes, after removal of marking, measure loss in plating material to ensure the minimum plating thicknesses are satisfied, then expose it to salt atmosphere (TM 2009). Perform resistance to solvents (TM 2015), external visual (TM 2009), fine and gross leak (TM 2014) in that order; no failures.

C.7.5.4.14.1 Laser marking rework. Rework of laser marking is not allowed.

C.7.5.4.14.2 Stick on labels. For stick on labels, fungus and adhesion tests shall also be performed after standard rework qualification testing.

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APPENDIX D

GENERIC PERFORMANCE VERIFICATIONS FOR NON-HERMETIC DEVICE TECHNOLOGIES

D.1 SCOPE

D.1.1 Scope. This appendix is intended to be used by manufacturers in developing their baseline flow of processes, screens, and Periodic Inspections / Qualified Manufacturers List (PI/QML) for non-hermetic devices. This appendix provides an acceptable standard which will be used to verify the performance requirements for compliance of non-hermetic and open architecture devices. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. Manufacturers may demonstrate a test and inspection system that achieves at least the same level of quality as could be achieved by complying with this appendix. These standards may be used as is or as modified in accordance with 3.9.1. The test flow presented in this appendix may not be appropriate for all non-hermetic or open architecture devices. For these types of devices, this appendix should be used as a starting point in developing an appropriate test flow.

D.1.1.1 Definitions.

Non-hermetic device - A device which has all or some of the elements not hermetically sealed and is categorized as follows:

a. Cavity non-hermetic device - A cavity device having construction utilizing non-hermetic (polymeric) seals.

b. Non-cavity non-hermetic device – A non-cavity device having construction utilizing molding compounds or other materials encapsulation the internal elements.

c. Open non-hermetic device – A open device having construction with minimal or no protection of the internal elements.

d. Open architecture device (OA) – A single substrate with hermetically sealed hybrid or multichip cavity(s) in which all bare die, chip and wire, or flip chip are mounted in the hermetically sealed area. Non-hermetic packaged components integral to the substrate (resistors, capacitors, coils, tranformers, and transistors) which are typically mounted on printed circuit boards are not hermetically sealed.

NOTE: Non-hermetic devices should be used with caution and in appropriate end item use environments. Refer to D.3.2 for non-hermetic requirements.

D.1.2 Description of appendix D. This appendix contains the standard testing and inspection approach to verify the performance requirements of this appendix. This is a five-step approach consisting of an element evaluation program, a process control program, a screening program, a conformance inspection program (CI), and a periodic inspection / Qualified Manufacturer's List (PI / QML). Some of the traditional tests of appendix C (hermetic devices) may not be applicable to these type of devices including: Fine and gross leak, particle impact noise detection test (PIND), and internal gas analysis content. The non-hermetic test methods described in this appendix are in addition to appendices A, E, F, and G.

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D.1.3 Performance requirements. Two quality assurance classes are provided for in this appendix. The classes are described below.

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D.1.3.1 Performance requirements for Class L non-hermetic, and open architecture devices. Class L is the highest quality class provided for in this appendix. This class will include the element evaluation flow, in-process inspection flow, screening flow, conformance inspection (CI) and the periodic inspection (PI) / qualification manufacturers list (QML) flow. These devices will be specified over the temperature range of -55°C to +125°C or as specified in the device specification. Manufacturers of these devices will be fully certified and qualified in accordance with this appendix. Verification of the applicable performance requirements will be performed as described in D6, D7, and D8 herein.

D.1.3.2 Performance requirements for Class F non-hermetic and open architecture devices. Class F is a standard quality class provided for in this appendix. This class will include the element evaluation flow, in-process inspection flow, screening flow, conformance inspection (CI) and the periodic inspection (PI) / qualification manufacturer list (QML) flow. These devices will be specified over the temperature range of -55ºC to +125ºC, or a lesser range as specified by the acquisition document, e.g. SMD, SCD, or catalog. Manufacturers of these devices will be fully certified and qualified in accordance with this appendix. Verification of the applicable performance requirements will be performed as described in D6, D7, and D8 herein.

D.1.3.3 Performance requirements for radiation hardness assurance (RHA) devices. Compliant RHA devices will meet the additional performance requirements of appendix G.

D.2 APPLICABLE DOCUMENTS

D.2.1 General. The documents listed in this section are specified in sections D.3, D.4, D.5 D.6, D.7, or D.8 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections D.3, D.4, D.5, D.6, D.7 or D.8 of this specification whether or not they are listed.

D.2.2 Government documents.

* D.2.2.1 Specifications, standards, and handbooks. The following specifications, standards and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 - Electronic and Electrical Component Parts
MIL-STD-750 - Test Methods for Semiconductor
MIL-STD-883 - Test Methods Standard Microcircuits

(Copies of these documents are available online at https://quicksearch.dla.mil).

* D.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

JEDEC PUBLICATION

JEP142 – Obtaining and Accepting Material for Use in Hybrid/MCM Products.

JEDEC STANDARDS

JESD22-A101 – Steady State Temperature Humidity Bias Life Test.
JESD22-A102 – Accelerated Moisture Resistance – Unbiased Autoclave.
JESD22-A110 – Highly Accelerated Temperature and Humidity Stress Test (HAST).
JESD22-A113 – Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing.

(Copies of these documents are available online at https://www.jedec.org/).

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APPENDIX D

GEIA STANDARDS

SSB-1 - Guideline for Using Plastic Encapsulated Microcircuits and Semiconductors in Military, Aerospace and Other Rugged Applications

(Copies of these documents are available online at https://www.techamerica.org/).

IPC-Association Connecting Electronics Industries (IPC)

IPC/JEDEC J-STD-020 - Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.
IPC/JEDEC J-STD-035 - Acoustic Microscopy for Non-Hermetic Encapsulated Electronic Components.

(Copies of these documents are available online at https://www.jedec.org).

D.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

D.3 GENERAL

D.3.1 Non-hermetic device guidelines. The SSB-1 guideline document addresses many of the issues involved with non-hermetic devices and provides tools for reliability assessment. The qualification tables and classifications herein are based on the reliability assessment of SSB-1.

D.3.2 Non-hermetic device requirements.

D.3.2.1 Cavity device capability. The cavity non-hermetic device shall be capable of passing the following specified tests (e.g. temperature cycle, autoclave, highly accelerated temperature and humidity stress test (HAST), centrifuge, vibration, mechanical shock, PIND, and gross leak as applicable) without degradation of device or device failure. The testing specified herein may not characterize the polymer-sealed cavity sufficiently to assure acceptable moisture protection, and therefore may not meet typical long term application requirements. The device shall also be capable of passing end item use applications specified in the device specification (reference D.9.2.2 herein).

D.3.2.2 Non-cavity device capability. The non-cavity non-hermetic device shall be capable of passing the following specified tests (e.g. temperature cycle, autoclave, highly accelerated temperature and humidity stress test (HAST), centrifuge, vibration, mechanical shock, and PIND as applicable) without degradation of device or device failure. The device shall also be capable of passing end item use applications specified in the device specification (reference D.9.2.2 herein).

D.3.2.3 Open device capability. The open non-hermetic device shall be capable of passing the following specified tests (e.g. temperature cycle, centrifuge, vibration and mechanical shock as applicable) without degradation of device or device failure. The device shall also be capable of passing end item use applications specified in the device specification (reference D.9.2.2 herein).

D.3.2.4 Device design and construction. Non-hermetic device design and construction shall be in accordance with the applicable requirements of appendix E and the device device specification or SMD. Special considerations shall be given for non-hermetic design and construction techniques; however, the device shall be capable of passing all applicable tests and screens of this appendix or the device specification.

D.3.3 Periodic process monitoring. The manufacturer shall have a system in place to periodically monitor the non-hermetic assembly process and reliability. As required by the acquiring activity source control drawing (SCD), statement of work (SOW), (SMD) or periodic process monitoring shall apply to D.7 herein, preconditioning (as applicable) and subgroup C1 on a reduced sample basis (half the quantity of devices specified in the tables listed in this appendix). It is recommended that the periodic process monitoring be specified in the acquisition document and be performed every 2 years. Other methods of periodic process monitoring specified in the acquisition document are acceptable as technology and end use environments are unique.

D.3.4 Hermetic cavity requirements.

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D.3.4.1 Hybrid cavity capability. The hermetic cavity shall be capable of passing all hybrid/multichip module requirements specified in Appendix E without degradation of device or device failure. Classes F and L OA devices with a hermetically sealed cavity shall be required to meet the seal requirements of Classes H and K respectively, in method 1014 of MIL-STD-883.

D.4 ELEMENT EVALUATION

D.4.1 Description of element evaluation. Element evaluation is used to verify that procured materials and devices meet their specified characteristics and are adequate to perform as intended under the conditions experienced in the application. Element characteristics required to assure device performance and assembly process capability shall be identified. These evaluations shall be completed on all materials prior to their use in production devices (see table D-I). These evaluations shall be modified by the manufacturer based on:

a. Element quality and reliability history.

b. Device quality and reliability history.

c. Supplier history.

d. Supplier/manufacturer relationship.

e. Possible impact of element evaluation failure after assembly.

NOTE: Elements may be assembled into the device prior to final element lot acceptance. The hybrid manufacturer shall have a system, approved by the qualifying activity, to maintain traceability of all such elements for the purpose of element containment. This system shall be employed only when a work stoppage situation is encountered, schedule is affected or when a lengthy test is required. For Class L devices, elements may be assembled into the device only with acquiring activity approval. For all classes, element evaluation shall be successfully completed prior to device shipment.

D.4.1.1 Element evaluation guidance. JEP142 provides guidance regarding design considerations, material assessment techniques, and recommendations for material acceptance prior to use in Hybrid/MCM products. JEP142 is not an alternate element evaluation and shall not supersede any element evaluation requirements of Class F and Class L of this document.

D.4.2 General.

D.4.2.1 Sequence of testing. Subgroups within a group (table) of tests may be performed in any sequence, but individual tests within a subgroup shall be performed in the sequence indicated.

D.4.2.2 Sample selection. Samples shall be randomly drawn from inspection lots or in-line production samples as applicable. The sample size columns in the evaluation tables give minimum quantities to be evaluated with applicable accept number enclosed in parentheses.

D.4.2.3 Class requirements. Class L and Class F element evaluation requirements are identified by X's in the appropriate column locations of evaluation tables.

D.4.2.4 Location of element evaluation. Element evaluation may be performed at the element supplier facility (or other facility approved by the device manufacturer) or at the device manufacturing facility.

D.4.2.5 Characteristics. Characteristics to be verified shall be those necessary for compatibility with the element acquisition documents and assembly procedures and at least those which cannot be verified after assembly, but could cause functional failure.

D.4.2.6 Protection from electrostatic discharge. Suitable handling precautions and grounding procedures shall be taken to protect ESDS elements from accidental damage.

D.4.2.7 Electrical test specifications. Electrical test parameters, values, limits (including deltas when applicable), and conditions shall be specified in the element acquisition documents.

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TABLE D-I. Element evaluation summary.

Element	Paragraph	Table or MIL-STD-883 method
Microcircuit and semiconductor dice	D.4.3	Table D-II
Passive elements	D.4.4	Table D-III
Saw elements	D.4.5	Table D-IV
Alternate element evaluation	D.4.7	N/A
Substrate evaluation	D.4.8	Table D-V
Package evaluation	D.4.9	Table D-VI
Integral Substrate/Package evaluation	D.4.10	Table D -VII
Polymeric material evaluation	D.4.11	Method 5011

D.4.3 Microcircuit and semiconductor dice. Microcircuit and semiconductor dice from each wafer lot shall be evaluated in accordance with table D-II and D.4.3.1 through D.4.3.6.1. For Class F devices, element evaluation testing is not required for JANHC or JANKC discrete semiconductor MIL-PRF-19500 qualified die or for MIL-PRF-38535 Class Q or V qualified die that is supplied on an SMD and listed on the applicable QML. For Class L devices, element evaluation is not required for JANKC discrete semiconductor MIL-PRF-19500 qualified die or for MIL-PRF-38535 Class V qualified die that is supplied on an SMD and listed on the applicable QML.

D.4.3.1 Subgroup 1, 100 percent electrical test of dice. Each die shall be electrically tested, which should be done at the wafer level provided all failures are identified and removed from the lot when the dice are separated from the wafer. When wafer/die level testing requirements are not specified in the procurement documents, the manufacturer/die supplier shall choose the parameters, conditions, and limits to assure compliance with the electrical characteristics.

D.4.3.2 Subgroup 2, 100 percent visual inspection of dice. Each die shall be visually inspected to ensure conformance with the applicable die related requirements of method 2010 of MIL-STD-883, condition A for Class L and condition B for Class F; methods 2069, 2070, 2072, and 2073 of MIL-STD-750 and the element acquisition documents.

D.4.3.3 Sample evaluation of assembled dice.

D.4.3.3.1 Test samples. A sample of die from each wafer lot shall be evaluated in accordance with table D-II, subgroups 3 through 6 as applicable, and D.4.3.3.2 through D.4.3.6.1.

D.4.3.3.2 Test sample preparation. Test samples may be assembled such that similar assembly methods and conditions the element shall see during normal production assembly shall be simulated. Electrical probe testing may be performed in lieu of assembly.

D.4.3.4 Subgroups 3 and 4.

D.4.3.4.1 Sample size. The Class F sample shall consist of at least ten die from each wafer lot. The Class L sample shall consist of three die from each wafer and a total of at least ten die from each wafer lot. (If one wafer is evaluated, then ten die shall be tested, if ten wafers are evaluated, then 30 die (three from each wafer) shall be tested).

D.4.3.4.2 Internal visual. Each sample shall be visually inspected to assure conformance with the applicable requirements of method 2010 of MIL-STD-883; methods 2069, 2070, 2072 and 2073 of MIL-STD-750; and the element acquisition documents.

D.4.3.4.3 Electrical test. For interim, post burn-in, and final electrical tests, the minimum requirements for microcircuits and semiconductor dice shall include static tests at each of the following:

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a. At + 25°C.

b. Maximum rated operating temperature.

c. Minimum rated operating temperature.

NOTE: Final electrical tests satisfy end-point electrical test requirements specified in preceding test methods and need not be repeated.

D.4.3.5 Subgroup 5.

D.4.3.5.1 Sample size. From each wafer lot, a sample of at least five die requiring ten bond wires minimum shall be selected.

D.4.3.5.2 Wire bond strength testing. For wire bond strength testing:

a. A minimum of ten wires consisting of die-to-package, die-to-die, or die-to-substrate bonds shall be destructively pull tested. An equal number of bonds shall be tested on each sample die.

b. For beam lead and flip-chips, five devices shall be tested.

c. The element metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample shall be selected in accordance with D.4.3.5.1 and subjected to subgroup 5 evaluation. If the second sample contains no failures, the bonding test results are acceptable and the lot of dice is acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the lot of dice shall be rejected.

d. The rejected wafer lot should be resubmitted to subgroup 5 evaluation if the failure was not due to defective die metallization.

D.4.3.6 Subgroup 6, scanning electron microscope (SEM).

D.4.3.6.1 Sample selection and reject criteria. Microcircuit sample selection and reject criteria shall be in accordance with method 2018 of MIL-STD-883 on a homogeneous lot. Discrete semiconductor devices with oxide steps or expanded contacts shall be tested with the sample selection and reject criteria in accordance with method 2077 of MIL-STD-750. In cases when dice are very large and comprise a large area of the wafer, the qualifying activity may approve other alternate sample selection plans.

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TABLE D-II. Microcircuit and semiconductor dice evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	L	F		Method	Condition		
1	X	X	Element electrical			100 percent	D.4.3.1
2	X	X	Element visual	2010 1/ 2069 1/ 2070 1/ 2072 1/ 2073		100 percent	D.4.3.2
3	X	X	Internal visual	2010 1/ 2069 1/ 2070 1/ 2072 1/ 2073		2/10 (0)	D.4.3.3 D.4.3.4.2
4	X		Temperature cycling	1010	C	2/ 10 (0)	D.4.3.3
	X		Mechanical shock or Constant acceleration	2002 2001	B, Y1 direction 3,000 g's, Y1 direction		
	X		Interim electrical				D.4.3.4.3
	X		Burn-in	1015	240 hours minimum at +125°C		
	X		Post burn-in electrical				D.4.3.4.3
	X		Steady-state life	1005			
	X	X	Final electrical				D.4.3.4.3
5	X	X	Wire bond evaluation	2011		10 (0) wires or 20 (1) wires	D.4.3.3 D.4.3.5
6	X		SEM	2018 1/ 2077		See method 2018 of MIL-STD-883 or method 2077 of MIL-STD-750	D.4.3.6

1/ MIL-STD-750 methods.
2/ For Class L sample sizes see D.4.3.4.1.

D.4.4 Passive elements. Passive elements from each inspection lot shall be evaluated in accordance with table D-III and D.4.4.1 through D.4.4.7. This evaluation is not required when the elements are acquired from the established reliability series of specifications and is listed on the QPL.

D.4.4.1 Subgroup 1, 100 percent electrical test of passive elements. Each passive element shall be electrically tested at +25°C as specified in the element acquisition documents.

D.4.4.2 Subgroup 2, visual inspection of passive elements. Passive elements shall be visually inspected to assure conformance with the applicable passive element related requirements of method 2032 of MIL-STD-883, Class K for Class L, and Class H for Class F, and the passive element acquisition documents.

a. Each Class L passive element shall be visually inspected.

b. Class F elements shall be sample inspected using a sample size and (accept number) of 22 (0).

D.4.4.3 Test sample preparation for subgroups 3 and 4.

a. For Class F and L passive elements, when assembly is required to perform electrical tests, test samples shall be assembled such that the assembly methods and conditions the element will see during normal assembly will be simulated. Electrical probe testing may be performed in lieu of assembly.

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b. The total test sample shall contain at least ten wires (an equal number on each element) if wire bonding assembly is applicable.

D.4.4.4 Sample electrical test of passive elements. Sample passive elements shall be electrically tested at +25°C for the following characteristics (minimum):

a. Resistors: DC resistance.

b. Capacitors:

(1) Ceramic type: Dielectric withstanding voltage, insulation resistance, capacitance, and dissipation factor.

(2) Tantalum type: DC leakage current, capacitance, and dissipation factor.

(3) Metal insulation semiconductor type (MIS): DC leakage current, capacitance, and dielectric withstanding voltage.

c. Inductors: DC resistance, inductance, and Q.

d. Transformers and coils: Dielectric withstanding voltage and insulation resistance.

e. Crystals: Frequency and equivalent resistance.

D.4.4.5 Visual examination. Elements shall be visually examined for evidence of corrosion or damage attributable to the test and conditioning sequence.

D.4.4.6 Wire bond strength testing. Wire bond strength testing applies to elements which are wire bonded during the device assembly operation. The sample will include at least five elements and 10 bond wires minimum.

a. At least ten wires, consisting of element-to-substrate, element-to-package, or element-to-element bonds shall be destructively pull tested. An equal number of bonds shall be tested on each sample element.

b. The element metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample shall be selected and subjected to the test in accordance with D.4.4.6.a. If the second sample contains no failures, the bonding test results and the element lot are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot shall be rejected.

c. The element inspection lot may be resubmitted to evaluation if the failure was not due to defective element metallization.

* D.4.4.7 Voltage conditioning or aging. Voltage conditioning or aging shall be performed in accordance with the appropriate passive device specification. When there is no applicable device specification, or the requirements of the device specifications are not appropriate, the manufacturer shall document the procedure being used. Below are some examples of defense specifications used for passive element conditioning requirements:

a. Resistors:

MIL-PRF- 914 - Resistor Networks, Fixed, Film, Surface Mount, Nonestablished Reliability, and Established Reliability, General Specification for.
MIL-PRF-32159 - Resistors, Chip, Fixed, Film, Zero Ohm, Industrial, High Reliability, Space Level, General Specification for.
MIL-PRF-39007 - Resistors, Fixed, Wire-Wound (Power Type), Nonestablished Reliability, Established Reliability, and Space Level, General Specification for.
MIL-PRF-55182 - Resistors, Fixed, Film, Nonestablished Reliability, Established Reliability, and Space Level, General Specification for.
MIL-PRF-55342 - Resistors, Chip, Fixed, Film, Nonestablished Reliability, Established Reliability Space Level, General Specification for.

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b. Capacitors:

MIL-PRF-123 - Capacitors, Fixed, Ceramic, Dielectric, (Temperature Stable and General Purpose), High Reliability General Specification for.
MIL-PRF-49470 - Capacitor, Fixed, Ceramic Dielectric, Switch Mode Power Supply (General Purpose and Temperature Stable), Standard Reliability and High Reliability, General Specification for.
MIL-PRF-55365 - Capacitor, Fixed, Electrolytic (Tantalum), Chip, Established Reliability, Nonestablished Reliability, and High Reliability, General Specification for.
MIL-PRF-55681 - Capacitor, Chip, Multiple Layer, Fixed, Ceramic Dielectric, Established Reliability and Nonestablished Reliability, General Specification for.

c. Coils, transformers:

MIL-PRF-27 - Transformers and Inductors (Audio, Power, and High Power Pulse) General Specification for.
MIL-PRF-15305 - Coils, Fixed and Variable, Radio Frequency, General Specification for.

d. Crystals:

MIL-PRF-3098 - Crystal Units, Quartz, General Specification for.

TABLE D-III. Passive element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	L	F		Method	Condition		
1	X	X	Element electrical			100 percent	D.4.4.1
2	X	X	Visual inspection	2032		100 percent 22 (0)	D.4.4.2
3	X		Temperature cycling	1010	C	10 (0)	D.4.4.3
	X X		Mechanical shock or Constant acceleration	2002 2001	B, Y1 direction 3,000 g's, Y1 direction		
	X X		Voltage conditioning or Aging				D.4.4.7
	X		Visual inspection	2032			D.4.4.5
	X	X	Electrical				D.4.4.4
4	X	X	Wire bond evaluation	2011		10 (0) wires or 20 (1) wires	D.4.4.3 D.4.4.6

D.4.5 Surface acoustic wave (SAW) element evaluation. SAW elements shall be evaluated in accordance with table D-IV and D.4.5.1 through D.4.5.3.

D.4.5.1 Radio frequency (RF) probe test. Each SAW element shall be RF probe tested as specified in the device specification. This RF probe test may be done at the wafer level provided all failures are identified and removed from the lot when the elements are separated from the wafer. RF probe testing will be performed at +25°C unless otherwise specified by the device specification.

D.4.5.2 Visual inspection. Each SAW element shall be visually inspected to assure conformance with the requirements of method 2032 of MIL-STD-883.

D.4.5.3 Wire bond evaluation. From each inspection lot of SAW elements, a randomly selected sample of at least two elements will be evaluated for shall bond pull strength.

a. A minimum of ten wires shall be bonded and destructively pull tested in accordance with method 2011 of MIL-STD-883.

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b. The SAW element metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample shall be selected and subjected to the test in accordance with D.4.5.3.a. If the second sample contains no failures, the bonding test results and the element lot are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot shall be rejected.

c. The element inspection lot may be resubmitted to wire bond evaluation if the failure was not due to defective element metallization.

d. With acquiring activity approval, destructive bond pull tests may be performed on test coupons that provide the specified test requirements. Test coupons shall be processed with the same element production lot.

TABLE D-IV. SAW element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883 method	Quantity (accept number)	Reference paragraph
	L	F				
1	X	X	RF electrical probe		100 percent	D.4.5.1
2	X	X	Visual inspection	2032	100 percent	D.4.5.2
3	X	X	Wire bond evaluation	2011	10 (0) wires or 20 (1) wires	D.4.5.3
4	X	X	Alternate element Evaluation		100 percent	D.4.7

D.4.6 Open architecture device (OA) element evaluation. OA elements shall be evaluated in accordance with table D-II, D-III, D-IV subgroup 4, and paragraphs D.4.6.1 and D.4.6.2.

D.4.6.1 Visual inspection. Each OA element shall be visually inspected to assure conformance with the requirements of method 2032 of MIL-STD-883.

D.4.6.2 Wire bond evaluation. From each inspection lot of OA elements, a randomly selected sample of at least two elements will be evaluated for bond pull strength.

a. A minimum of ten wires shall be bonded and destructively pull tested in accordance with method 2011 of MIL-STD-883.

b. The OA element metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample shall be selected and subjected to the test in accordance with D.4.6.2.a. If the second sample contains no failures, the bonding test results and the element lot are acceptable. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, the element lot shall be rejected.

c. The element inspection lot may be resubmitted to wire bond evaluation if the failure was not due to defective element metallization.

d. With acquiring activity approval, destructive bond pull tests may be performed on test coupons that provide the specified test requirements. Test coupons shall be processed with the same element production lot.

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D.4.7 Alternate element evaluation. Alternate element evaluation shall be used only in cases where full device performance cannot be adequately ascertained outside the actual end item (e.g., hybrid microcircuit RF component). The sample built into devices shall successfully complete evaluation prior to release of the balance of the incoming lot. In lieu of packaged element evaluation tests in accordance with D.4.3, D.4.4, and D.4.5, elements may be assembled into devices and tested. Acceptance of these elements shall be based on the ability of the device to meet all group A, subgroups 1, 2, and 3 (plus 4, 7, and 9 as applicable) electrical tests required for the device. A minimum of ten elements or 100 percent of the elements, whichever is less, (0 defects) shall be assembled into at least three devices. Devices assembled for the purpose of element evaluation are deliverable provided all of the provisions of this specification are met. Element wire bond evaluation for elements may be accomplished using a second or additional sample of elements wire bonded for that purpose only. When the device build option for evaluation is selected, the manufacturer shall establish and maintain a sample plan or procedure to identify the sample prior to electrical test. In case of lot failure when alternative element evaluation is used, all of the device samples and the inspection lot shall be rejected. When the manufacturer chooses to analyze the failed devices to isolate the cause of failure, and this analysis determines that the cause of failure is not related to the element being tested, and that the element has been correctly stressed during the required screening and testing, then the inspection lot may be accepted. If the element has not been correctly stressed, the failed device may be reworked or new sample replacement devices may be assembled.

D.4.8 Substrate evaluation. Substrates shall be evaluated in accordance with table D-V and D.4.8.1 through D.4.8.5.3.3.

NOTE: Substrates fabricated by the device manufacturer using a qualified process shall be exempt from this evaluation.

D.4.8.1 Definition. For the purpose of substrate evaluation, a substrate inspection lot shall consist of homogeneous substrates having the same number of layers, manufactured using the same facilities, processes, materials, and vacuum deposited, plated, or printed as one lot.

D.4.8.2 Electrical test parameters. Electrical test parameters, values, limits, and conditions will be as specified in the applicable device specification.

D.4.8.3 Subgroup 1, 100 percent electrical testing. Each substrate shall be electrically tested at +25°C, if and as specified in the applicable device specification.

D.4.8.4 Subgroup 2, 100 percent visual inspection. Each substrate shall be visually inspected to ensure conformance with the applicable requirements of method 2032 of MIL-STD-883, and the applicable device specification.

D.4.8.5 Subgroups 3, 4, and 5 general requirements. From each inspection lot of substrates, a randomly selected sample shall be evaluated. Destructive tests may be performed on test coupons which provide the required test data. The test coupons shall be made with the same materials that were used in the manufacturing of the inspection lot and processed at the same time as the inspection lot.

D.4.8.5.1 Subgroup 3. A minimum of five samples shall be submitted to subgroup 3 testing.

D.4.8.5.1.1 Physical dimension. Inspect in accordance with method 2016 of MIL-STD-883, and the applicable device specification.

D.4.8.5.1.2 Visual inspection. Inspect in accordance with method 2032 of MIL-STD-883, and the applicable device specification.

D.4.8.5.1.3 Electrical. Substrates shall be electrically tested at +25°C for the following characteristics (minimum). Requirements shall be as specified in the applicable device specification.

a. Resistors: DC resistance.

b. Capacitors: Capacitance. As specified in the applicable device specification, test for dielectric withstanding voltage, insulation resistance, and dissipation factor.

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c. For multilayered substrates, continuity and isolation testing shall be performed to verify the interconnection of conductors as specified in the applicable device specification.

D.4.8.5.2 Subgroup 4. A minimum of three samples that have been subjected to, and passed, subgroup 3 testing shall be submitted to subgroup 4 testing.

D.4.8.5.2.1 Conductor thickness. Measure conductor thickness in accordance with the applicable device specification. Conductor thickness shall meet the requirements specified in the applicable device specification.

D.4.8.5.2.2 Conductor resistivity. Measure conductor resistivity in accordance with the applicable device specification. Conductor resistivity shall meet the requirements specified in the applicable device specification.

D.4.8.5.2.3 Film adhesion. Perform film adhesion testing in accordance with acceptable industry standards. The substrate and tape shall show no evidence of peeling or flaking of metallization.

D.4.8.5.2.4 Solderability. For solderable substrates only, perform solderability testing if specified in the applicable device specification.

D.4.8.5.3 Subgroup 5. A minimum of two samples that have been subjected to, and passed, subgroup 3 testing shall be submitted to subgroup 5 testing.

D.4.8.5.3.1 Temperature coefficient of resistance (TCR): Perform TCR testing for resistors in accordance with method 304 of MIL-STD-202. TCR shall meet the requirements specified in the applicable device specification.

a. Thick film type: Test as a minimum, two resistors from each resistor paste sheet resistance value. One from the smallest and one from the largest area resistors at -55°C using a reference reading at +25°C, or temperatures as specified in the device specification.

b. Thin film type: Test as a minimum, the highest value resistor at +125°C using a reference reading at +25°C or temperatures as specified in the device specification.

c. If specified in the applicable device specification, TCR tracking testing shall be performed. TCR tracking shall meet the requirements specified in the applicable device specification.

D.4.8.5.3.2 Wire bond strength testing. For wire bondable substrates, perform wire bond strength testing in accordance with method 2011 of MIL-STD-883. The sample shall include at least two substrates and ten bond wires minimum. For gold metalized Class L substrates that at the device level are intended to contain aluminum wire bonds, aluminum wires shall be placed as specified in the device specification and these wire bond samples shall be baked for 1 hour at +300°C minimum in either an air or an inert atmosphere prior to the performance of wire bond strength testing.

a. At least ten wires, consisting of substrate to substrate bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample substrate.

b. The substrate metallization shall be acceptable if no failure occurs. If only one wire bond fails, a second sample of a minimum of ten wires shall be prepared using the same wire type/size and the same type equipment as the failed bond(s). If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the substrate inspection lot shall be rejected.

c. The substrate inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective substrate metallization.

D.4.8.5.3.3 Die shear strength testing. Perform shear strength testing in accordance with method 2019 of MIL-STD-883. At least two die for each substrate shall be attached and tested for each die attachment method, as specified in applicable device specification. If a failure occurs at less than the specified force and is not due to defective substrate materials, the lot shall be resubmitted to die shear evaluation and the failure mode documented.

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TABLE D-V. Substrate evaluation requirements.

Subgroup	Class		Test	MIL-STD-883 method	Quantity (accept number)	Reference paragraph
	L	F				
1	X	X	Electrical testing		100 percent	D.4.8.3
2	X	X	Visual inspection	2032	100 percent	D.4.8.4
3	X	X	Physical dimension	2016	5 (0)	D.4.8.5.1.1
	X	X	Visual inspection	2032		D.4.8.5.1.2
	X	X	Electrical			D.4.8.5.1.3
4	X	X	Conductor thickness or conductor resistivity		3 (0)	D.4.8.5.2.1 D.4.8.5.2.2
	X	X	Film adhesion test			D.4.8.5.2.3
	X	X	Solderability			D.4.8.5.2.4
5	X	X	TCR		2 (0)	D.4.8.5.3.1
	X	X	Wire bond evaluation	2011	10 (0) wires or 20 (1) wires	D.4.8.5.3.2
	X	X	Die shear evaluation	2019	2 (0)	D.4.8.5.3.3

D.4.9 Package evaluation. Package cases or covers shall be evaluated in accordance with table D-VI and D.4.9.1 through D.4.9.5. In addition, laser marked surfaces will be subjected to, and pass, subgroups 6 or table D-VI.

D.4.9.1 Definition. For the purpose of package evaluation, a package inspection lot shall consist of homogeneous cases or covers of the same type and outline dimensions (may differ only in lead length and lead count), manufactured using the same facilities and processes, and plated as one lot within a 6-month time frame (if plating is applicable).

D.4.9.2 General

a. From the package inspection lot, a randomly selected sample shall be subjected to package evaluation.

b. Subgroups 1, 2, and 3 of table D-VI shall be accomplished for each lot. Subgroup 4 (as applicable) of table D-VI shall be accomplished periodically at intervals not exceeding 6 months for additional package inspection lots, for metal packages. Subgroup 6 (as applicable to metal package or leads) shall be performed one time only for Class F and at 6 month intervals for Class L unless a change in material or plating is made.

c. Subgroups 2, 3, and 4 of table D-VI apply to cases only. A quantity (accept number) of 15 (0) shall apply to the number of terminals or leads to be tested or all leads (if less than five devices) shall be tested. The leads shall be randomly selected from three packages.

d. Covers require only subgroups 1 and 6 (as applicable) of table D-VI.

e. Laser marked metal plated surfaces shall be subjected to, and pass, subgroup 6.

D.4.9.3 Subgroup 1. Separately verify case and cover dimensional compliance with the element acquisition documents.

D.4.9.4 Subgroup 4. For metal cases with leads separated by an insulator, measure insulation resistance between the metal body of the case and the leads that are isolated from the case. This test does not apply to non-metallic cases. This test shall be performed at 6 month intervals unless a change in insulator material is made for Class F devices and on every incoming lot for Class L devices.

D.4.9.5 Subgroup 6. Separately verify case and cover for compliance with subgroup 6 (as applicable) of table D-VI. Both internal and external areas shall be inspected.

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TABLE D-VI. Package evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	L	F		Method	Condition		
1	X	X	Physical dimensions	2016		3 (0)	D.4.9.3
2	X	X	Solderability	2003	Soldering temperature +245°C ± 5°C	3 (0) 15 (0) leads	D.4.9.2
3	X	X	Lead integrity	2004 2028	B2 (lead fatigue) D (leadless chip carriers) B1 for rigid leads (pin grid array leads)	3 (0) 15 (0) leads	D.4.9.2
4	X	X	Metal package isolation	1003	600 V dc 100 nA maximum	3 (0) 15 (0)leads	D.4.9.2 D.4.9.4
5			Not used				
6	X	X	Salt atmosphere	1009	A	5 (0)	D.4.9.2 D.4.9.5

D.4.10 Integral substrate/package evaluation. Integral substrate/packages (ISP) shall be evaluated in accordance with table D-VII and D.4.10.1 through D.4.10 .8.

D.4.10.1 ISP inspection lot. For the purpose of ISP evaluation, an ISP inspection lot shall consist of ISP of the same type; manufactured using the same facilities, processes and materials, within 90 days.

*

D.4.10.2 General.

a. Section D.4.10 is intended to be used as an end-of-line ISP acceptance procedure performed at the completion of the ISP construction and prior to the construction of the device.

b. ISP elements fabricated by the hybrid device manufacturer using a MIL-PRF-38534 qualified process shall be exempt from this evaluation as long as D.4.8 and D.4.9 are used for the components of the ISP.

c. Subgroups 1, 2, 4, 5, and 6 of table D-VII shall be accomplished for each inspection lot.

d. For lead integrity and solderability testing, a quantity (accept number) of 15 (0) shall apply to the number of terminals or leads to be tested or all leads (if less than five devices) shall be tested. The leads shall be randomly selected from three packages.

e. The same samples may be used for subgroups 4, 5, and 6, of table D-VII.

D.4.10.3 Subgroup 1. Each element shall be electrically tested at +25°C as specified in the device specification. If none is stated, the device manufacturer shall use his standard procedure.
NOTE: This may be satisfied by performing a continuity/isolation test.

D.4.10.4 Subgroup 2. Each element shall be visually inspected to assure conformance to the applicable requirements of method 2009 and method 2032 of MIL-STD-883, and the applicable device specification. This inspection shall be limited to the features that are inspectable.

D.4.10.5 Subgroup 4. The physical dimensions shall be verified against the device specification.

D.4.10.6 Subgroup 5. Wire bond strength testing. For wire bondable devices, perform wire bond strength testing in accordance with method 2011 of MIL-STD-883. The sample size shall include at least two ISP devices and 10 bond wires minimum. For gold metallized Class L ISPs, that at the hybrid level are intended to contain aluminum wire bonds, aluminum wires shall be placed as specified in the device specification and these wire bond samples shall be baked for one hour at 300°C ±10°C in either air or an inert atmosphere prior to the performance of wire bond strength testing.

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a. At least ten wires, consisting of substrate to substrate bonds, shall be destructively pull tested. An equal number of bonds shall be tested on each sample ISP device.

b. The ISP metallization shall be acceptable if no failures occur. If only one wire bond fails, a second sample of a minimum of ten additional wires shall be prepared using the same wire type/size and the same type of equipment as the failed bond. If the second sample contains one or more failures, or if more than one failure occurs in the first sample, then the ISP lot shall be rejected.

c. The ISP inspection lot may be resubmitted to evaluation if the failure(s) was not due to defective ISP metallization.

D.4.10.7 Subgroup 7. Prior to solderability testing, the elements or leads only shall be submitted to a preconditioning temperature of +250°C ±10°C for a period of 6 ±0.5 hours, or equivalent. (See D.7.4.1.6 for examples of equivalent conditions).

D.4.10.8 Subgroup 8. Both internal and external areas shall be inspected. This test shall be performed one time only for the life of the program, or as needed to evaluate changes in the fabrication process.

TABLE D-VII. Integral substrate/package element evaluation requirements.

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	L	F		Method	Condition		
1	X	X	Electrical testing			100 percent	D.4.10.3
2	X	X	Visual inspection	2032 and 2009		100 percent	D.4.10.4
4	X	X	Physical dimensions	2016		3 (0)	D.4.10.5
5	X	X	Wire bond evaluation	2011		10 wires (0) 20 wires (1)	D.4.10.6
6	X	X	Lead integrity	2004	B_2	3 (0)	D.4.10.2.d
7	X	X	Solderability	2003	Solder temperature +245°C ±5°C	3 (0)	D.4.10.2.d D.4.10.7
8	X	X	Salt atmosphere	1009	A	3 (0)	D.4.10.8

D.4.11 Polymeric material evaluation. The polymeric materials (conductive and non-conductive attach materials) used in device applications shall be subjected to and pass the evaluation procedures detailed in method 5011 of MIL-STD-883. Evaluation is not required for encapsulations, seals, coatings, plastics, used in non-hermetic devices but shall be validated during PI/QML testing. The manufacturer should be aware of outgassing, ionic impurities, or other conditions that may result from the materials used in the non-hermetic devices.

D.5 PROCESS CONTROL AND IN-LINE PROCESS MONITOR

D.5.1 Description of process control. Process control and monitoring is a methodology used to detect defective processes prior to completion of assembly. The indicated processes shall be controlled in accordance with table D-VIII and D.5.2 through D.5.5 though process control may be applied to other areas of the design.

D.5.2 Wire bonding.

D.5.2.1 General. A process machine operator evaluation shall be performed:

a. When a machine is put into operation.

b. Periodically while in operation, not to exceed 4 hours (wire bond lot).

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c. When the operator is changed. Change of certified auto wire bond operators is allowed without machine re-evaluation if all other machine conditions for evaluation are maintained.

d. When any machine part has been changed.

e. When any machine adjustment of the process parameters has been made.

f. When the spool of wire is changed.

g. When a new device type is started (unless the machine was evaluated using test samples that also simulate the new device type, see D.5.2.2).

h. A wire bonding lot consists of devices that are consecutively bonded using the same setup and wire, by one machine/operator (operator changes are allowed for autobonders) during the same period not to exceed 4 hours.

D.5.2.2 Standard evaluation circuit (test coupon or test vehicle). Standard evaluation circuits (test coupons or test vehicles) that simulate the production device metal bonding system (e.g., thick film, thin film, aluminum bonding pads, plated gold) may be destructively evaluated in lieu of the product.

D.5.2.3 Process machines. Process machines not meeting the evaluation requirements shall not be used.

D.5.2.4 Corrective action of process machine. A process machine may be returned to operation only after appropriate corrective action has been implemented and the machine has been evaluated and passed testing in accordance with table D-VIII as required.

D.5.2.5 Data record. A data record shall be maintained and identifiable to each machine, operator, shift, and date of test.

D.5.2.6 Wire bond process setup.

D.5.2.6.1 Process machine/operator evaluation. Sample wires from three devices or a test sample shall be destructively pull tested in accordance with method 2011 of MIL-STD-883, and as follows:

a. Class F devices: A minimum of ten wires total consisting of wire bonds to elements metallization bonding systems (e.g., thick film, thin film, aluminum bonding pads, plated gold) typical of device assembly operation shall be tested.

b. Class L devices: A minimum of 15 wires total shall be tested. As a minimum, wires tested shall include one each from a typical transistor, diode, capacitor, resistor, three wires from each IC and five wires from the package to the substrate, as applicable.

c. Classes F and L: Evaluation results are acceptable if no failure occurs at less than the value given in method 2011 of MIL-STD-883. If any of the sample wires fail, the machine/operator shall be deactivated and corrective action taken. When a new sample has been prepared, tested, and has passed this procedure, the machine/operator has been certified or recertified, it may be returned to service.

D.5.2.6.2 Lot sample bond strength. From each wire bonding lot, a sample of at least two devices shall be nondestructively tested in accordance with method 2023 of MIL-STD-883. This requirement does not apply to devices that are 100 percent nondestructively tested. Alternately, destructive pull testing in accordance with method 2011 may be performed. Devices with known visual wire bonding rejects shall not be excluded from this sample.

a. In each sample device, at least 15 wires shall be tested, including one wire from each type of transistor, diode, capacitor, resistor, three wires from each type of integrated circuit, and five wires connecting package leads, as applicable. If there are less than 15 wires in the device, all wires shall be tested. Sample devices shall be inspected for lifted wires. Lifted wires resulting from bond pull testing shall be counted as nondestruct pull test failures.

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b. The wire bonding lot shall be acceptable if no failure occurs. If one wire bond fails, another sample of two devices shall be selected and 100 percent nondestructively tested. If the second sample contains no failures, the wire bonding lot is acceptable. If the second sample also contains failure(s), or more than one wire bond fails in the first sample, the bonding machine/operator shall be removed from the operation.

c. The failures shall be investigated and appropriate corrective action shall be implemented. The machine/operator shall be recertified in accordance with D.5.2.6.1 before being returned to operation. All devices bonded since the previous certification (lot sample bond strength test) that have not received 100 percent nondestruct bond pull shall be subjected to 100 percent nondestructive bond strength testing (Class F).

d. For RF/microwave devices, test sample circuits that simulate the production device may be destructively evaluated in lieu of the product (see D.5.2.2). When test sample circuits are used, the data from this test shall be used for SPC monitoring of the process/product.

D.5.3 Seal testing. Seal, as a process monitor, only applies to hermetically sealed areas of OA devices. All Class L devices shall receive fine leak testing, without pressurization (bomb) within one hour of removal from sealing atmosphere and prior to any other test. Class L devices may be sealed with any amount of helium tracer gas and shall pass the corresponding leak rate, or the helium leak rate may be calculated based on the helium tracer gas atmosphere.

37 percent Helium – 3.7×10^{-8} atm cc/sec He.
10 percent Helium – 1.0×10^{-8} atm cc/sec He.
5.0 percent Helium – 5.0×10^{-9} atm cc/sec He.
3.0 percent Helium – 3.0×10^{-9} atm cc/sec He.

Calculation:
He leak rate = 1×10^{-7} x He%/100%
If failure occurs, the lid seal rework requirements will be followed.

CAUTION NOTE: The use of helium fill for high voltage devices may lead to ionization of the helium and cause the parts to fail. The device manufacturer shall document the design accordingly if sealing in helium tracer gas or if other gas is damaging to the device."

D.5.4 Internal gas analysis process monitor. The manufacturer shall develop and document a system to utilize method 1018, of MIL-STD-883, as a guideline to monitor the sealing process. Levels of all gases reported, including moisture, shall be evaluated to the extent necessary to detect any variation in the sealing process, based upon the manufacturer's data. Reported gases shall be used to aid in identifying possible process deficiencies or evidence of out-of-control conditions.

D.5.5 Attach validation monitor. As a manufacturer option, the attached validation monitor for substrate or die attach may be monitored in-line using either one, or a combination of, die shear, radiography, and ultrasonic inspection. The attach process monitor shall apply to solder, eutectic, silver glass, conductive, or non-conductive adhesive attach materials as applicable to the design.

D.5.6 Testing for pure tin finishes. The manufacturer shall develop a test plan that will assure no parts used in the hybrid have a pure tin finish.

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TABLE D-VIII. In-line process monitor.

Class		Test	MIL-STD-883 method	Condition	Reference paragraph
L	F				
X	X	Wire bonding	2011 2023		D.5.2
1/	1/	Die shear	2019	100 percent die shear, one device every inspection lot	D.5.5
1/	1/	Radiography	2012	10 percent of every production/ inspection lot	D.5.5
1/	1/	Ultrasonic inspection	2030	10 percent of every production/ inspection lot	D.5.5

1/ Manufacturer's option.

D.6 DEVICE SCREENING

D.6.1 Description of device screening. Screening is a series of tests and inspections performed on each device in each lot in order to eliminate products which do not meet the performance requirements. Each device shall be subjected to and pass all of the applicable screening tests and inspections in accordance with table D-IX and D-X and as defined in D.6.2 through D.6.13.

D.6.2 General.

a. Additional tests and inspections may be performed where experience indicates justifiable concern for specific quality characteristics.

b. Electrical test parameters, values, limits (including deltas), and conditions shall be as specified on the device specification.

c. All devices that fail any test criterion in the screening sequence shall be removed from the lot at the time of observation, or immediately at the conclusion of the test, in which the failure was observed.

d. When PDA, pattern failure, or delta limits have been specified, or other conditions for lot acceptance have been imposed, the required data shall be recorded and maintained as a basis for lot acceptance.

e. Once rejected and verified as a device failure, rework and subsequent rescreening in accordance with the limitations of this specification may be performed.

b. Tests shall be performed in the order specified in table D-IX and D-X, except as specified in D.6.7, D.6.11 and D.6.12.

D.6.3 Nondestructive bond pull test for Class L devices. Nondestructive 100 percent bond pull test shall be performed for Class L devices. The total number of failed wires and the total number of devices failed shall be recorded. The lot shall have a PDA of 2 percent or one wire, whichever is greater based on the number of wires pulled in the wire bond lot or production lot. Failed lots may be resubmitted one time to 100 percent nondestructive bond pull test with a tightened PDA of 1.5 percent. The test shall be performed in accordance with method 2023 of MIL-STD-883. Devices from lots that have been subjected to the nondestructive 100 percent bond pull test and have failed the specified Class L PDA requirement shall not be delivered as Class F product.

D.6.4 Pre-seal burn-in test. Pre-seal burn-in shall be performed in accordance with method 1030 of MIL-STD-883.

D.6.5 Internal visual inspection. Devices awaiting internal visual inspection, and open non-hermetic devices awaiting further processing, shall be stored in a controlled environment as specified in method 2017 of MIL-STD-883.

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D.6.6 Visual inspection for damage. The manufacturer may inspect for damage after each thermal or mechanical screening step, or at any subsequent time in the screening sequence.

D.6.7 Particle impact noise detection (PIND) test. For cavity devices, PIND shall be performed in accordance with method 2020 of MIL-STD-883, condition A or B and shall be performed 100 percent anytime after centrifuge/mechanical shock but before X-ray and external visual. For Class L devices, condition A shall be used unless otherwise specified. For Class L screening, the lot may be accepted on any of the five runs if the percentage of defective devices is less than 1 percent (or one device, whichever is greater). All defective devices will be removed after each run. Lots which do not meet the 1 percent PDA on the fifth run, or exceed 25 percent defectives cumulative, will be rejected. PIND testing shall not apply to non-cavity or open non-hermetic devices.

D.6.8 Pre-burn-in electrical test.

a. Pre-burn-in electrical testing is optional except when delta limit measurements are required. However, devices may be tested to remove defects prior to further screening and to form a basis for application of PDA criteria.

b. This test need not include all device parameters, but shall include those measurements most sensitive to and effective in removing electrically defective devices.

c. When delta limits are specified in the device specification, the measurements shall be recorded, and traceability shall be maintained from the device to the corresponding electrical test data.

D.6.9 Burn-in. Burn-in shall be performed on each device in accordance with method 1030 of MIL-STD-883 for open devices and method 1015 of MIL-STD-883 for cavity/non-cavity devices in accordance with the device document.

D.6.9.1 General.

a. Pre-burn-in (interim burn-in for Class L) and post burn-in electrical parameters as specified in the device specification shall be measured.

b. Burn-in electrical conditions shall be as specified in the device specification.

c. Delta limits shall be defined in the device specification when required.

d. Delta measurements shall be made on parameters specified in the device specification.

e. The manufacturer shall determine and document, prior to beginning burn-in, the criteria for the formation of burn-in lots (e. g., devices submitted to burn-in at one time, a production lot, or an inspection lot). The burn-in lot shall be $\geq$41 devices or all devices submitted to burn-in during a 1 week period.

f. The manufacturer shall not conduct burn-in in addition to that specified.

g. Unless otherwise specified in the device specification, PDA, and pattern failure, analysis shall be applicable only to +25 °C static tests (group A, subgroup 1).

D.6.9.2 Burn-in period.

a. Class L devices shall be burned-in in accordance with the time-temperature regressions specified in method 1015 (method 1030 for open non-hermetic devices) of MIL-STD-883. When specified, the burn-in time shall be equally divided into two successive burn-ins. Interim electrical tests in accordance with the device specification will be performed after the first burn-in to determine acceptable devices for the second burn-in.

b. Class F devices shall be burned-in in accordance with the time-temperature regressions specified in method 1015 (method 1030 for open non-hermetic devices) of MIL-STD-883.

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D.6.9.3 Failure analysis of burn-in screen failures for Class L devices. Catastrophic failures (e.g., shorts or opens measurable or detectable at +25°C) after burn-in shall be analyzed. Analysis of catastrophic failures may be limited to a quantity and degree sufficient to establish failure mode and cause. Failure analysis results shall be documented and available to the Government representatives.

D.6.9.4 Lots resubmitted for burn-in. Burn-in lots that do not exceed twice the allowable PDA may be resubmitted for burn-in one time only (e.g., if the PDA limit is 10 percent, then the lot may be resubmitted if less than 20 percent). Failure analysis for other than Class L is not required. Resubmitted lots shall be kept separate from new lots and shall be inspected for all specified characteristics using a tightened inspection PDA equal to the next lower number in the PDA series. The number of pattern failures allowed shall be the same as required for the original burn-in.

D.6.9.5 Burn-in acceptance criteria. At the option of the manufacturer, burn-in acceptance shall be based on PDA or pattern failures. Either option, or both, may be applied to a burn-in lot as acceptance criteria (i.e., if a lot exceeds PDA requirements, then pattern failure analysis may be used to determine if the lot is acceptable without performing a resubmitted burn-in).

D.6.9.5.1 General. Pattern failures are multiple device failures within a device burn-in lot with the same root cause of failure. When the PDA or pattern failures applies to delta limits, the delta parameter values measured after burn-in (100 percent screening test) shall be compared with the delta parameter values measured prior to that burn-in.

D.6.9.5.2 PDA option.

D.6.9.5.2.1 PDA Class F. For Class F, the PDA shall be 10 percent or one device, whichever is greater, regardless of burn-in lot size.

D.6.9.5.2.2 PDA Class L. For Class L, the PDA shall be 2 percent or one device, whichever is greater, regardless of burn-in lot size. Class L PDA shall be calculated on failures occurring during the second half of burn-in only.

D.6.9.5.3 Pattern failure option.

D.6.9.5.3.1 Pattern failure option, Class F. For Class F devices, when acceptance is based on pattern failures, all multiple device static failures at +25°C shall be analyzed to determine root cause. Multiple device failures with the same root cause (three or more depending on lot size) shall be considered a “pattern failure”. If a “pattern failure” is established, the lot shall be rejected; otherwise, the lot shall be accepted regardless of PDA. In all cases, lots with device failures that do not exceed the PDA are acceptable and do not require pattern failure analysis. The number of device failures with the same root cause that establish a “pattern failure” shall be based on lot size, as follows:

Lot size (x)	Number of failures that establish a pattern
$x \leq 20$	3
$21 \leq x \leq 40$	4
$40 < x \leq 100$	5
$100 < x \leq 300$	6
$300 < x \leq 500$	11
$500 < x$	16

Example 1: Lot size is 25 with 4 device static failures at +25°C.

If all 4 device failures do not have the same root cause of failure (i.e., 3 or less failures with the same root cause), then no “pattern failure” exists and the passing 21 devices are acceptable.

If all 4 failures have the same root cause of failure, then a “pattern failure” exists and the lot shall be rejected.

Example 2: Lot size is 400 with 15 device static failures at +25°C.

The lot is acceptable (i.e., 10 percent PDA allows 40 device failures).

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Example 3: Lot size 400 with 41 device static failures at +25°C.

If ten or less of the device failures are due to the same root cause, then a “pattern failure” does not exist and the lot is acceptable.

If 11 or more of the device failures are due to the same root cause, then a “pattern failure” has been established and the lot is unacceptable.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, non-screenable defects, or non-reworkable, the device shall be rejected.

D.6.9.5.3.2 Pattern failure option, Class L. For Class L, when acceptance is based on pattern failures, all multiple device static failures at +25°C shall be analyzed to determine root cause. The lot shall be stopped and placed on hold if:

a. Any two device failures within the burn-in lot have the same root cause of failure (i.e., pattern failure established), or

b. The total number of device failures in the burn-in lot exceeds 5 percent.

The lots may be reworked and recovered if the failure is due to:

a. A defect that can be effectively removed by rescreening the entire burn-in lot or,

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, non-screenable defects, or non-reworkable, the lot shall be rejected.

D.6.10 Final electrical test.

a. Final electrical testing shall include all parameters, limits, and conditions of test which are specifically identified in the device specification as final electrical test requirements. As a minimum, final electrical testing shall include group A electrical tests in table D-XII, subgroups 1, 2, and 3 (plus subgroups 4, 7, and 9 as applicable).

b. Final electrical testing satisfies end-point electrical test requirements specified in the preceding screening test method (e.g. after temperature cycle, centrifuge) and need not be duplicated.

D.6.11 Seal (gross leak only with no type 1 detector fluid or pressurization bomb). Gross leak testing shall apply to non-hermetic cavity type devices only.

a. For Class L devices, the seal test may be performed in any sequence between the final electrical test and external visual, but it shall be performed after all shearing, forming, or solderability operations if there is an affect on the seal interface.

b. For Class F devices, the seal test may be performed in any sequence between the constant acceleration test and external visual, but it shall be performed after all shearing, forming, or solderability operations if there is an affect on the seal interface.

D.6.12 Seal (fine and gross leak for OA devices with hermetically sealed hybrid or multichip module(s)).

a. For class L devices, the seal test may be performed between the final electrical test and external visual, but it shall be performed after all shearing and forming operations on the terminals.

b. For class F devices, the seal test may be performed between the constant acceleration/mechanical shock test (or PIND, if applicable) and external visual, but it shall be performed after all shearing and forming operations on the terminals.

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c. For class L and F devices, all device lots (sublots) having any physical processing steps that may affect the seal (e.g., solder dipping to the glass seal) shall be retested for hermeticity and visual defects following seal or external visual This shall be accomplished by performing, and passing, as a minimum, a sample seal test (method 1014 of MIL-STD-883) using an acceptance criteria of a quantity (accept number) of 45 (0), and an external visual inspection (method 2009 of MIL-STD-883) on the entire inspection lot (sublot). For devices with leads that are not glass sealed, and that have a lead pitch less than or equal to .050 inch (1.27 mm), that sample seal test will be performed using a acceptance criteria of a quantity (accept number) of 15 (0). If the sample fails the acceptance criteria specified, all devices in the inspection lot represented by the sample shall be subjected to the fine and gross seal tests and all devices that fail shall be removed from the lot for final acceptance.

D.6.13 Radiography for Class L devices. Radiographic inspection in accordance with method 2012 of MIL-STD-883 shall be performed 100 percent any time after PIND but before external visual.

NOTE: Radiography shall only be deleted if the manufacturer and customer determine it to be not applicable or of limited value for a given design or technology.

D.6.14 External visual screen. The final external visual screen shall be conducted in accordance with method 2009 of MIL-STD-883, after all other 100 percent screens have been performed. The manufacturer shall inspect the devices 100 percent or on a sample basis using a quantity/accept number of 116(0). If one or more rejects occur in sample, the manufacturer may double the sample size with no additional failures allowed or inspect the remaining devices 100 percent for the failed criteria and remove the failed devices from the lot. If the doubled sample also fails, the manufacturer shall be required to 100 percent inspect the remaining devices in the lot for the failed criteria. Re-inspection magnification shall be no less than that used for the original inspection for the failed criteria.

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TABLE D-IX. Cavity, non-cavity non-hermetic, and OA device screening.

Class		Test	MIL-STD-883	Condition	Reference paragraph
L	F		Method		
X		Non-destructive bond pull	2023	100 percent	D.6.3
		Open burn-in	1030	Optional	D.6.4
X	X	Internal visual 1/	2017		D.6.5
X	X	Temperature cycle	1010	Condition B, 10 cycles – 55°C to 125°C	D.6.6
X	X	Constant acceleration 2/ or Mechanical shock 2/	2001 2002	3,000 G, Y1 direction Condition B, Y1 direction	D.6.6
X		PIND 3/	2020	Condition A shall be used for Class L, unless otherwise specified 4/	D.6.7
X		Pre-burn-in electrical		In accordance with device specification	D.6.8
X		Burn-in	1015	320 hrs at 125°C, PDA 2 percent after 2nd 160 hour BI	D.6.9
	X		1015	160 hours at 125°C PDA 10 percent	D.6.9
X	X	Final electrical		In accordance with device specification	D.6.10
X		Radiography	2012	Y1 only	D.6.13
X	X	Gross leak 5/	1014	Condition C - no bomb pressurization	D.6.12
X	X	Seal (fine and gross) 6/	1014	100 percent	D.6.12
X	X	External visual	2009	100 percent	D.6.14

See footnotes at end of table.

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TABLE D-IX. Cavity, non-cavity non-hermetic, and OA device screening - Continued.

1/ Devices are fully assembled after internal visual and before screening (temperature cycle) has commenced. Class L and F shall meet method 2017of MIL-STD-883, Class K and H respectively.
2/ Either constant acceleration or mechanical shock is required for cavity devices, neither test is required for non-cavity devices.
3/ Not required for non-cavity devices.
4/ Condition B may be used when specified in the applicable device specification.
5/ Gross leak seal test applies only to non-hermetic cavity devices. Not required for non-cavity devices.
6/ Seal test applies to hermetically sealed hybrids or multichip modules.

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TABLE D-X. Open non-hermetic device screening.

Class		Test	MIL-STD-883 method	Condition	Reference paragraph
L	F				
X		Non-destructive bond pull	2023	100 percent	D.6.3
		Open burn-in	1030	Optional	D.6.4
X	X	Internal visual 1/	2017		D.6.5
X	X	Temperature cycle	1010	10 cycles (Nit. Atm) –55°C to 125°C 2/	D.6.6
		Constant acceleration or 3/ or Mechanical shock 3/	2001 2002	3,000 G, Y1 direction Condition B, Y1 direction	D.6.6
X		Pre-burn-in electrical		In accordance with device specification	D.6.8
X		Burn-in	1030	320 hours at 125°C, PDA 2 percent after 2nd 160 hour BI	D.6.9
	X		1030	160 hours at 125° C, PDA 10 percent	
X	X	Final electrical		In accordance with device specification	D.6.10
X	X	Internal visual	2017	100 percent	D.6.5
X	X	External visual	2009	100 percent	D.6.14

1/ Devices are fully assembled after internal visual and before screening (temperature cycle) has commenced. Class L and F shall meet method 2017 of MIL-STD-883, Class K and H respectively.
2/ Nitrogen atmosphere shall be less than 100 ppm moisture at the supply point. If nitrogen atmosphere is not available, the open devices shall be protected from the temperature cycle environment and shall pass internal visual at the end of the screening process.
3/ Neither constant acceleration or mechanical shock is required, but may be performed at manufacturer's option.

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D.7 CONFORMANCE INSPECTION, AND PERIODIC INSPECTION.

D.7.1 Description of Conformance Inspection and Periodic Inspection. Conformance inspection (CI) and periodic inspection (PI) is a series of tests and inspections performed on samples of devices that have passed screening. These tests and inspections are used to further verify the performance requirements on a sample basis. Sample testing is necessary due to the fact that many of these tests are either destructive, expensive, or time consuming. Group A is considered CI, whereas groups B and C are considered PI/QML. CI and PI/QML shall consist of the tests and inspections specified herein. Devices shall not be accepted or approved for delivery until all applicable CI and PI/QML requirements have been met. The acquiring activity may approve delivery if groups A, B, C1, C4, and C5 testing have been completed and group C2, steady-state life test, has commenced. The manufacturer shall maintain traceability of all devices delivered to the acquiring activity prior to completion of CI and PI/QML testing for the purpose of notification/recall in case of test failure.

D.7.2 General. CI and PI for a given device type is determined by selection of a requirements option flow (see table D-XI). The requirements option flow selected shall determine the CI and PI/QML requirements for the specific device manufactured. Where applicable, inspection lot sampling shall be in accordance with Appendix F of this specification. Except where the use of final electrical test rejects or simulation samples (i.e., test coupons or test vehicles) are allowed, all devices shall have been previously screened and subjected to and passed all final electrical tests. Successful completion of CI and PI/QML for a given product assurance level shall satisfy qualification for either Class L or F. If a lot is withdrawn in a state of failing to meet requirements and is not resubmitted, it shall be considered a failed lot and reported as such.

D.7.2.1 Inspection lots. Inspection lots consist of a quantity of devices of a single device type (required for group A) or several different circuit types (allowed for group B) in a single package type and lead finish submitted at one time for final acceptance. All devices within each inspection lot shall be finally sealed in the same period not exceeding 13 weeks.

D.7.2.2 Inspection lot formation. Inspection lot formation is required if the inspection lot is to be formally accepted by the lot related CI and PI/QML testing of this specification. If the in-line process verification testing alternative is used, inspection lot formation is not required.

NOTE: The device manufacturer has the right to elect not to use any solution or solvent identified within this specification, or related specifications, that has also been identified by the American Congress of Government Industrial Hygienists as being a potential or suspect carcinogen. Where the device manufacturer elects not to use a material, they shall notify the acquiring or qualifying activities and the customer in writing in clear, unambiguous language not subject to misinterpretation that this right has been exercised.

TABLE D-XI. CI and PI/QML summary.

Requirement	Reference	Option 1 (in-line)	Option 2 (end-of-line)
General	Paragraph	D.7.2	D.7.2
Group A (CI)	Paragraph	D.7.3	D.7.3
	Table	D-XII	D-XII
Group B (PI)	Paragraph	D.7.4.1	D.7.4.2
	Table	N/A	D-XIV
Group C (PI/QML)	Paragraph	D.7.5 and D.8	D.7.5 and D.8
	Table	D-XV through D-XIX	D-XV through D-XIX

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D.7.2.3 Sample selection. The number of hybrid microcircuits to be tested shall be chosen (independent of lot size) by the manufacturer in accordance with the applicable requirements of options 1 or 2 of D-XI herein. Initial samples and resubmitted samples, when applicable, shall be randomly selected from the inspection lot. Lot acceptance is based on an accept number of zero. For group C inspection, limited sample quantities may be used to meet the requirements of D.7.1 for production start-up. When limited sampling is used for start-up, a subsequent full sample group C test shall be performed within 6 months of initial group C, or prior to exceeding the limited usage requirements of D.7.2.3.2, whichever comes first.

D.7.2.3.1 Non-functional samples. Electrically rejected devices from the same inspection lot may be used in all subgroups when end-point measurements are not required provided that the devices have been subjected to all device screening conditions through burn-in.

D.7.2.3.2 Limited usage samples: (For group C production start-up). A small lot sample shall be selected in accordance with table D-XV through D-XIX inclusive, when all three criteria listed below are met, otherwise the large lot sample shall be selected.

a. A maximum of 500 devices in a single order against a single drawing (device specification).

b. A maximum of 2,000 devices acquired against a single drawing on a given equipment-acquisition contract or program (device specification).

c. A maximum of 2,000 devices acquired against a single drawing during a 12 month period for a given device and manufacturer (device specification).

D.7.2.4 End-point electrical. End-point electrical shall be measured and recorded when applicable. The end-points shall be specified in the device document. If not specified, the end-point electrical shall be all tests at 25 °C.

D.7.2.5 Data. Test results shall be recorded by inspection lot identification code (date code), inspection lot, or serial number when applicable. For in-line group B inspections where inspection lots are not applicable, data records or logs will be maintained and available for review by the qualifying and acquiring activities. A summary of attributes results for all tests and measurements shall be part of the test report unless 100 percent recorded data is provided. Variable data shall be provided when required by the device specification.

D.7.3 Group A electrical testing. Group A electrical testing shall be performed in accordance with D.7.3.1 and the applicable device specification.

D.7.3.1 Group A general requirements. Group A subgroups shall as a minimum, include the final electrical testing of subgroups 1, 2, and 3 (plus 4, 7, and 9 as applicable) and any other subgroups required by the device specification. Each inspection lot or sub-lot shall be tested. A procedure for performing group A inspection in accordance with one or more of the following methods (see D.7.3.2, D.7.3.3 and D.7.3.4 herein) shall be available for review by the qualifying activity. Each of these three methods are equivalent, therefore, the manufacturer may choose to use any of the three.

NOTE: Sequence of test: Group A testing by subgroup shall be performed in any sequence after subgroup 1 (for PDA) or as specified in the device specification for other PDA purposes (e.g. all subgroups at 25°C).

D.7.3.2 End-of-line sample testing.

a. Sampling: The same sample may be used for all subgroup testing (e.g. for sample testing table D-XII quantity). Where the required size exceeds the lot size, 100 percent inspection shall be allowed.

b. Production performs all required final electrical screening tests.

c. Quality assurance or quality designate shall verify setup and randomly pull samples in accordance with table D-XII and production or quality assurance (QA) performs acceptance testing on the selected sample.

d. Group A failed lots shall be resubmitted in accordance with D.7.6.1.

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D.7.3.3 In-line sample testing. Test samples for each individual group A subgroup shall be randomly selected from the inspection lot after 100 percent screening of that subgroup (or subgroups, in the event that multiple subgroups are tested at the same temperature in sequence with the same test program). All devices in the inspection lot or sublot shall be available for selection as a test sample and a fully random sample shall be selected in accordance with table D-XII from the total population of devices. In addition, a different operator shall check the entire test setup and verify the use of the correct test program prior to testing the group sample. Group A failed lots shall be resubmitted in accordance with D.7.6.1.

TABLE D-XII. Group A electrical test.

Subgroup	Parameters	Quantity (accept number)
1	Static test at +25°C	116 (0)
2	Static tests at maximum rated operating temperature	76 (0)
3	Static tests at minimum rated operating temperature	45 (0)
4	Dynamic tests at +25°C	116 (0)
5	Dynamic tests at maximum rated operating temperature	76 (0)
6	Dynamic tests at minimum rated operating temperature	45 (0)
7	Functional tests at +25°C	116 (0)
8	Functional tests at maximum and minimum rated operating temperatures	76 (0)
9	Switching tests at +25°C	116 (0)
10	Switching tests at maximum rated operating temperature	76 (0)
11	Switching tests at minimum rated operating temperature	45 (0)

D.7.3.4 In-line verification testing. In-line verification testing, generally, is performed in conjunction with final electrical tests at screening which satisfy the requirements of group A testing and need not be repeated. Therefore, if the screening tests are performed with the verification defined here, the requirements of group A have been met.

a. For each test setup (and operator for manual testing) production shall test a correlation unit to assure that the accuracy requirements of MIL-STD-883 are being met.

b. Testing shall be performed using the verified setup.

c. At the completion of testing (or at least once each week) or following a change of operators for manual testing, a system shall be in place to verify production testing by:

(1) Visually inspecting to confirm that the correct test fixture, equipment, software, and procedures were used.

(2) Review actual testing or data of a controlled, known good, device of the device type being tested, utilizing the fixtures, equipment, software, and procedure(s) that were used by production. Variables data for all applicable group A tests at +25°C shall be read and recorded for the controlled unit. This data shall be maintained with the lot or traceable to the lot.

(3) Failure of the verification test will, as a minimum, require engineering to perform a review/analysis of hardware, software, setup, and parts to determine the root cause of the failure. The action taken shall be based on the analysis results. The entire group of devices being considered for acceptance after analysis may then be retested for the appropriate subgroup(s) acceptance one time only by repeating in-line verification testing. If the analysis does not specifically locate the problem, the lot may be reconsidered for acceptance one time only for 100 percent retesting of all of the devices to all of group A requirements and by repeating in-line verification testing.

D.7.4 Group B periodic inspection (PI). Group B inspection (PI) shall be satisfied by performing in-line inspection (D.7.4.1) sample monitoring or by performing end-of-line inspection (D.7.4.2) on screened devices.

D.7.4.1 Group B inspection, option 1 (in-line inspection). Group B will be satisfied by in-line inspections and tests in accordance with D.7.4.1.1 through D.7.4.1.8. Electrically rejected devices, or test vehicles or coupons, may be used in all subgroup tests in lieu of actual product.

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D.7.4.1.1 Physical dimensions. Randomly select devices from devices at final inspection so, as a minimum, two devices of each package type presented for inspection are inspected each month. Confirm that all critical dimensions affected by the assembly process (e.g., package length, width, height, pin length) meet the requirements of the device specification. Critical dimensions unaffected by assembly processes may be inspected at final visual inspection or as a part of incoming (receiving) inspection.

D.7.4.1.2 Resistance to solvents. Each inspection lot of marking ink shall be tested prior to acceptance in accordance with method 2015 of MIL-STD-883. This series of tests shall be performed on each type of surface which is used as the marking surface on completed devices (e.g., silver plate, abraded nickel plate, non-abraded nickel plate, plastic, ceramic). One piece of each applicable surface type shall be tested in each solvent. Each week one device or element (lid or package) representative of each of the marking surfaces of each device marked during the week shall be tested in accordance with method 2015 of MIL-STD-883, except that only "solvent D" is required.

D.7.4.1.3 Internal visual and mechanical. Internal visual and mechanical inspection shall be performed at pre-seal visual inspection in accordance with method 2014 of MIL-STD-883. As a minimum, one device of each device type received at pre-seal visual inspection each month shall be inspected.

D.7.4.1.4 Bond strength. Wire bond strength in-line inspection shall be performed as a part of wire bond certification and in accordance with method 2011 of MIL-STD-883. Each wire bond process (i.e., thermosonic gold, ultrasonic aluminum, thermal compressions gold) shall be tested weekly. Where more than one machine exists for a specific process, the test sample shall be rotated between machines so that all machines are tested at least once during each 13 week period when in operation. At the time of certification, an additional minimum ten wires total (15 wires for Class L) shall be bonded in the certification sample part(s). After completion of certification bond pulls, the parts with the additional ten wires (15 for class L) intact shall be preconditioned for 1 hour at +300°C minimum in either air or an inert atmosphere followed by destructive pull tests. An alternative preconditioned temperature of 140ºC for 3 hours shall be used for printed wiring boards. Bond strength requirements (i.e., minimum pull forces) shall be as specified in table D-XIII. No failures are allowed.

NOTE: As an option, it is allowable to wire bond coupon devices to certify each wire bond process using the conditions specified above.

D.7.4.1.5 Die shear. Die shear testing shall be performed on two devices as a part of group C inspection (i.e., first lot and after any major change affecting element attach). Die shear testing during group C shall be performed in accordance with method 2019 of MIL-STD-883.

D.7.4.1.6 Solderability. Solderability testing shall be performed as a part of incoming inspection (i.e., package evaluation) as follows:

Packages or leads only (package may melt under the following conditions, therefore leads may be removed from the package) shall be temperature aged to one of the following conditions prior to performing the steamage and solderability test in accordance with method 2003 of MIL-STD-883.

a. 6 ±0.5 hours at T_A = +250°C ±10°C

b. 22 ±1 hours at T_A = +200°C ±8°C

c. 160 ±8 hours at T_A = +150°C ±6°C

d. 192 ±8 hours at T_A = +125°C ±4°C

NOTE: When the device process flow includes an operation in which the package lead finish is changed prior to delivery of the device (e.g., a solder coating is applied), the solder coat operation shall be performed on the package evaluation sample packages subsequent to the temperature aging, steamage, and solderability test.

D.7.4.1.7 Seal. Seal tests (gross leak only with no type 1 detector fluid or pressurization bomb) shall be performed in accordance with method 1014 of MIL-STD-883. One-hundred percent testing shall be performed on all cavity devices between final electrical test and after all shearing, forming, or solderability operations if there is an effect on the seal interface.

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D.7.4.1.8 Seal (fine and gross leak for OA devices with hermetically sealed hybrid or multichip modules(s). For class L and F devices, the seal test may be performed between the constant acceleration/mechanical shock test (or PIND, if applicable) test and external visual, but it shall be performed after all shearing and forming operations on the terminals.

D.7.4.1.9 Non-conformance. If failures occur in any of the above in-line inspections, an analysis to determine cause shall be performed and corrective action, as necessary, shall be taken. The cause of failure, applicable corrective action, and disposition of product affected by the failure shall be documented. This documentation shall l be available for qualifying and acquiring activity review.

D.7.4.2 Group B inspection - option 2 (end-of-line inspection). Group B inspection shall be performed end-of-line on each inspection lot for each package type and lead finish in accordance with table D-XIV and D.7.4.2.1 through D.7.4.2.8. Electrically rejected devices, or test vehicles or coupons, may be used in all subgroup tests in lieu of actual product.

NOTE: If the manufacturer is not capable of performing the end-of-line test due to sensitive de-capsulation processing, the manufacture may perform physical dimension and resistance to solvents, and the balance of the group B tests shall be performed by an outside lab.

D.7.4.2.1 Physical dimensions. Randomly select devices from devices at final inspection so that, as a minimum, two devices of each package configuration presented for inspection are inspected. Confirm that all critical dimensions affected by the assembly process (e.g., package length, width, height, pin length.) meet the requirements of the device specification. Critical dimensions unaffected by assembly processes may be inspected at final visual inspection, or as a part of incoming (receiving) inspection.

D.7.4.2.2 Resistance to solvents. Each inspection lot of devices shall be tested in accordance with method 2015 of MIL-STD-883. To prevent solvents from damaging non-hermetic devices, an alternate method may be performed.

NOTE: Resistance to solvents may not apply to open non-hermetic devices.

D.7.4.2.3 Internal visual and mechanical. The criteria for internal visual and mechanical inspection shall be the general requirements for design and construction, the requirements of the device specification and confirmation that the actual device construction is in accordance with the design documentation on file.

D.7.4.2.4 Bond strength. Destructive wire bond pull tests shall be performed in accordance with method 2011 of MIL-STD-883 and as follows. Testing shall be accomplished in-line anytime after device wire bonding. Coupons which simulate actual production processes and materials may be used in lieu of actual product.

a. Two devices shall be preconditioned and tested.

b. Sample devices shall be preconditioned for one hour minimum at +300°C minimum in either air or an inert atmosphere. An alternative preconditioned temperature of 140ºC for 3 hours shall be used for printed wiring boards.

NOTE: If preconditioning cannot be performed due to device packaging (e.g. plastic package, encapsulated), then the device shall meet the post-seal bond strength requirements of method 2011 without the preconditioning.

c. Sampling criteria shall be based on the number of wires pull tested using a sample size (accept number) as follows:

(1) Class F: 22 (0) wires, 11 wires each device (or all wires if less).

(2) Class L: 44 (0) wires, 22 wires each device (or all wires if less).

d. Sample wire locations shall include wires from the following device locations as applicable:

(1) One wire from each type transistor, diode, capacitor, and resistor chip/die.

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(2) Three wires from each type integrated circuit.

(3) Five wires connecting to package leads.

e. The minimum allowable bond strength shall be in accordance with table D-XIII.

TABLE D-XIII. Bond strength requirements.

Gold or aluminum wire diameter, X (inches)	Minimum bond strength (grams)
X < 0.001	0.5
X = 0.001	1.0
0.001 < X ≤ 0.003	(Method 2011 of MIL-STD-883, table I, post-seal requirement) minus 1 gram
0.003 < X	(Method 2011 of MIL-STD-883, figure 2011-1, post-seal requirement) minus 10 percent

D.7.4.2.5 Die shear strength. The element (die/chip) shear test shall be performed to a quantity (accept number) of 22 (0) of the elements in the devices, or all elements in the two sample devices, whichever is less. The shear sample shall be uniformly divided among all element types (or all elements, if less) in the device and shall be performed in a minimum of two devices. The sample shall include typical resistor, capacitor, integrated circuit, and discrete semi-conductor elements. Alternative element shear may be conducted in accordance with D.8.6.4.14.1.

D.7.4.2.6 Solderability. At least 15 leads (or all leads, if less) shall be randomly selected, identified, and tested in accordance with method 2003 of MIL-STD-883. To prevent steamage damage to the non-hermetic device, the leads may be removed from the package and tested individually.

D.7.4.2.7 Seal (gross leak only with no type 1 detector fluid or pressurization bomb). For cavity devices, seal test (gross leak only with no type 1 detector fluid or pressurization bomb) shall be performed in accordance with method 1014 of MIL-STD-883. This test is not required if the 100 percent seal test screening is performed between final test and external visual.

D.7.4.2.8 Seal (fine and gross leak for OA devices with hermetically sealed hybrid or multichip modules). For Class L and Class F devices, the seal test may be performed between the constant acceleration/mechanical shock test (or PIND, if applicable) test and external visual, but it shall be performed after all shearing and forming operations on the terminals.

D.7.4.2.9 Non-conformance. If failures occur in any of the above end-of-line inspections, an analysis to determine cause shall be performed and corrective action, as necessary, shall be taken. The cause of failure, applicable corrective action, and disposition of product affected by the failure shall be documented. Resubmission shall be performed in accordance with D.7.6.1. This documentation shall be available for qualifying and acquiring activity review.

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TABLE D-XIV. Group B testing (option 2, end-of-line only).

Subgroup	Class		Test	MIL-STD-883		Quantity (accept number)	Reference paragraph
	L	F		Method	Condition		
1	X	X	Physical dimension	2016		2 (0)	D.7.4.2.1
2			Not used				
3	X	X	Resistance to solvents 1/	2015		3 (0)	D.7.4.2.2
4	X	X	Internal visual and mechanical	2014		1 (0)	D.7.4.2.3
5	X	X	Bond strength: a. Thermocompression b. Ultrasonic or wedge c. Flip-chip d. Beam lead	2011	 C or D C or D F H	2 (0)	D.7.4.2.4
6	X	X	Die shear strength	2019		2 (0)	D.7.4.2.5
7	X	X	Solderability	2003	Solder temperature +245°C ±5°C	1 (0) 15 (0) leads	D.7.4.2.6
8	X	X	Seal (gross only no bomb pressurization) 2/	1014	C or D	15 (0)	D.7.4.2.7
9	X	X	Seal (fine and gross) 3/	1014			D.7.4.2.8

1/ Optional for open non-hermetic devices.
2/ Seal test applies to cavity devices intended to pass un-bombed gross leak.
3/ Seal test applies to hermetically sealed hybrids or multichip modules.

D.7.5 Group C inspection (PI/QML). Group C inspection (PI/QML) shall be performed only on the first inspection lot submitted for inspection, as required to evaluate or qualify major changes and as required for periodic process monitoring (D.3.3). Group C inspection shall be performed in accordance with D.7.7 and D.8 herein; table D-XV, D-XVI, and D-XVII for cavity and non-cavity non-hermetic, OA devices, and D.7.8 and D.8 herein, tables D-XVIII and D-XIX for open non-hermetic devices. This testing satisfies qualification (QML) specified in D.8 for the applicable class.

NOTE: The qualifying activity may approve alternate test plans for small lots of devices for group C inspection.

D.7.6 Non-conformance. Lots which fail subgroup requirements of groups A, B, and C may be resubmitted in accordance with the provisions of D.7.6.1. A failed lot which is reworked or is re-screened (re-submittal to inadvertently missed process steps is not considered a re-screen) shall not be resubmitted to the failed subgroups (and shall be counted as a failure) for periodic groups B, C, and PI/QML coverage. The lot may be resubmitted only to the failed subgroup to determine its' own acceptance. If a lot is not resubmitted or fails the resubmission, the lot shall not be shipped and the compliant marking and all references to this document shall be removed.

D.7.6.1 Resubmission of failed lots. Resubmitted lots shall be kept separate from new lots and shall be clearly identified as resubmitted lots. When any initial lot submitted for CI or PI fails, any subgroup requirement of groups A, B, and C tests, it may be resubmitted once for that particular subgroup at double the sample size or 100 percent tested with zero failures allowed. A second resubmission using double the initial sample size with zero failures allowed is permitted only if failure analysis is performed to determine the mechanism of failure for each failed device from the prior submissions and it is determined that failure is due to:

a. A defect that can be effectively removed by re-screening the entire lot, or

b. Random type defects which do not reflect poor basic device design or poor basic processing procedures.

NOTE: In all instances where analysis of the failed devices indicates that the failure mechanism is due to poor basic processing procedures, a basic design fault, or non-screenable defects, the lot shall not be resubmitted.

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D.7.7 Group C cavity and non-cavity non-hermetic, and OA PI/QML testing. Preconditioning shall be performed in accordance with D.8.6.4.1 and is considered a destruct test.

TABLE D-XV. Preconditioning.

Class		Test	MIL-STD-883	JEDEC	Condition	Quantity	Reference paragraph
L	F		Method	Method		(Accept number) 1/	
X	X	External visual	2009			10 (0) or 44 (0)	D.8.6.4.11
X	X	Ultrasonic inspection 2/ 3/	2030	J-STD-035	Record results	10 (0) or 44 (0)	D.8.6.4.18
X	X	Moisture/reflow sensitivity classification for non-hermetic devices 2/ End-point electrical Visual Temperature cycle Bake out Heat Soak 4/ Reflow		Reference J-STD-020 and JESD22-A113	 In accordance with device specification Document results -40 to 60°C, 5 cycles 24 hrs. 125°C 192 hrs, 30°C, 60% RH 3 Cycles	10 (0) or 44 (0)	D.8.6.4.1
X	X	End-point electrical			In accordance with device specification	10 (0) or 44 (0)	D.8.6.4.12
X	X	Ultrasonic inspection 3/	2030	J-STD-035	Compare with initial results	10 (0) or 44 (0)	D.8.6.4.18
X	X	External visual	2009			10 (0) or 44 (0)	D.8.6.4.11

1/ Ten to 44 devices minimum required at end of precondition to perform subgroup C1 (table D-XVI) and group C2 (table D-XVII).
2/ Required to establish moisture sensitivity limits in accordance with J-STD-020.
3/ Ultrasonic Inspection may not apply due to the construction of the device (e.g. open cavity in a non-cavity device).
4/ Heat soak condition may be selected based on moisture sensitivity of the end item application (Reference J-STD-020). The condition specified is a moisture sensitivity level 3. Level 1 or 2 may be performed to meet the level 3 minimum level.

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* TABLE D-XVI. Group C cavity, non-cavity non-hermetic, and OA PI/QML testing.

CLASS L	CLASS F	Test	MIL-STD-883 Method	JEDEC Method	Condition	Quantity (Accept number)	Reference paragraph
		Subgroup C1					
X	X	External visual	2009			5 (0) or 22 (0)	D.8.6.4.11
X	X	Ultrasonic inspection 1/	2030	J-STD-035		5 0) or 22 (0)	D.8.6.4.18
X	X	PIND 2/ 3/	2020		A or B, 5 passes	5 (0) or 22 (0)	D.8.6.4.2
X	X	Autoclave		JESD22-A102	96 hours –0, +5 hours Temp 121 ±2°C (dry bulb) 100 percent humidity 29.7 psia vapor pressure	5 (0) or 22 (0)	D.8.6.4.4
		or			or		
X	X	Steady-state temperature humidity bias life test (85/85)		JESD22-A101	1,000 hours –24, +168 hours, 85 ±2°C (dry bulb) 85 ±5 percent humidity 49.1 kPa vapor pressure		
		or			or		
X	X	Highly accelerated temperature and humidity stress test (HAST)		JESD22-A110	96 hours -0, +2 hours Temp 130°C ±2°C (dry bulb) 85 percent ±5 percent humidity 33.3psia vapor pressure		
X	X	Temperature cycling	1010		100 cycles, –55°C to +125°C	5 0) or 22 (0)	D.8.6.4.3
X		Autoclave		JESD22-A102	96 hours –0, +5hours 121 ±2°C (dry bulb) 100 percent humidity 29.7psia vapor pressure	5 (0) or 22 (0)	D.8.6.4.4
		or			or		
X		Steady-state temperature humidity bias life test (85/85)		JESD22-A101	1,000 hours –24, +168 hours, 85 ±2°C (dry bulb) 85 ±5 percent humidity 49.1 kPa vapor pressure		
		or			or		
X		Highly accelerated temperature and humidity stress test (HAST)		JESD22-A110	96 hours -0, +2 hours Temp 130°C ±2°C (dry bulb) 85 percent ±5 percent humidity 33.3psia vapor pressure		
X	X	Constant acceleration or 2/ 4/	2001		3,000 G, Y1 direction	5 (0) or 22 (0)	D.8.6.4.5

See footnotes at end of table.

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TABLE D-XVI. Group C cavity, non-cavity non-hermetic and OA PI/QML testing – Continued.

CLASS L	CLASS F	Test	MIL-STD-883 Method	JEDEC Method	Condition	Quantity (Accept number)	Reference Paragraph
		Subgroup C1					
X	X	Random vibration 2/ 3/ 4/	2026		Condition F	5 (0) or 22 (0)	D.8.6.4.6
X	X	Mechanical shock 2/ 4/	2002		Condition B, Y1 direction	5 (0) or 22 (0)	D.8.6.4.7
X	X	PIND 2/	2020		A or B, 1 pass	5 (0) or 22 (0)	D.8.6.4.2
X	X	End-point electrical			In accordance with device specification	5 (0) or 22 (0)	D.8.6.4.13
X	X	Gross leak 2/ 5/	1014			5 (0) or 22 (0)	D.8.6.4.8
X	X	Seal (fine and gross) 7/	1014				D.8.6.4.9
		Subgroup C3					
X	X	Internal gas analysis 7/	1018			3 (0) or 8/	D.8.6.4.10
		Subgroup C4 6/					
X	X	External visual	2009			2 (0)	D.8.6.4.11
X	X	Ultrasonic inspection	2030	J-STD-035	Compare with initial results	2 (0)	D.8.6.4.18
X	X	Internal visual and mechanical	2014			2 (0)	D.8.6.4.14
X	X	Bond strength	2011		44 wires, or all if less	2 (0)	D.8.6.4.15
X	X	Die shear	2019		Five elements from each attach process.	2(0)	D.8.6.4.16
		Subgroup C5					
X	X	ESD	3015		a. Electrical parameters Gp A-1 b. ESDS c. Electrical parameters Gp A-1	3 (0)	D.8.5

1/ Ultrasonic inspection is not required if the test was performed during preconditioning.
2/ Required for cavity devices only.
3 Manufactures option.
4/ Optional based on design for non-cavity devices (e.g. soft encapsulation device may require constant acceleration or shock).
5/ For cavity devices intended to pass un-bombed gross leak.
6/ Outside lab may perform subgroup C4 testing (reference D.8.6.4.15 herein).
7/ Seal and IGA test applies to hermetically sealed hybrids or multichip modules.
8/ Subgroups 3 and 4 samples will have received subgroup 1 environmental exposure. Subgroup 3 samples may be used to perform subgroup 4 tests.

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TABLE D-XVII. Group C2 – cavity and non-cavity non-hermetic PI/QML testing.

Class		Test	MIL-STD-883	Condition	Quantity (Accept number)	Reference paragraph
L	F		method			
X	X	End-point electrical		In accordance with device specification	5 (0) or 22 (0)	D.8.6.4.12
X	X	Steady-state life test	1005	1,000 hours at +125°C or equivalent	5 (0) or 22 (0)	D.8.6.4.13
X	X	End-point electrical		In accordance with device spec	5 (0) or 22 (0)	D.8.6.4.12

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D.7.8 Open non-hermetic device PI/QML testing. Group C testing shall be performed in accordance with D-XVIII.

TABLE D-XVIII. Group C for open non-hermetic PI/QML testing.

Class L	Test F	Test	MIL-STD-883 method	Condition	Quantity (Accept number)	Reference paragraph
		Subgroup C1				
X	X	External visual	2009		5 (0) or 22 (0)	D.8.6.4.11
X	X	Internal visual and mechanical	2014		5 (0) or 22 (0)	D.8.6.4.14
X	X	Temperature cycle	1010	100 cycles (nit atm) -55°C to +125°C 1/	5(0) or 22 (0)	D.8.6.4.3
X	X	Constant acceleration or 2/	2001	3,000G, Y1 direction	5 (0) or 22 (0)	D.8.6.4.5
X	X	Mechanical shock or 2/	2002	B, Y1 direction	5(0) or 22(0)	D.8.6.4.7
X	X	Random vibration 2/	2026	Condition F	5(0) or 22(0)	D.8.6.4.6
X	X	End-point electrical		In accordance with device specification	5(0) or 22(0)	D.8.6.4.12
X	X	External visual	2009		5(0) or 22(0)	D.8.6.4.11
		Subgroup C4				
X	X	Internal visual and mechanical	2014		2 (0)	D.8.6.4.14
X	X	Bond strength	2011	44 wires, or all if less	2 (0)	D.8.6.4.15
X	X	Die shear	2019	Five elements from each attach process	2 (0)	D.8.6.4.16
		Subgroup C5				
X	X	ESD	3015	a. Electrical parameters b. ESDS c. Electrical parameters	3 (0)	D.8.5

1/ Nitrogen atmosphere shall be less than 100 ppm moisture at the supply point. If nitrogen atmosphere is not available, the open devices shall be protected from the temperature cycle environment and shall pass internal visual during the subgroup C4 internal visual and mechanical process.
2/ Optional based on design

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TABLE D-XIX. Group C2 – Life test for open non-hermetic QML testing.

Class		Test	MIL-STD-883	Condition	Quantity (Accept number)	Reference paragraph
L	F		method			
X	X	End-point electrical		In accordance with device specification	5(0) or 22(0)	D.8.6.4.12
X	X	Steady-state life test	1005 using TM1030	1,000 hrs at 125°C (nit atm) or equivalent 1/	5(0) or 22(0)	D.8.6.4.13
X	X	End-point electrical		In accordance with device specification	5(0) or 22(0)	D.8.6.4.12

1/ Nitrogen atmosphere shall be less than 100 ppm moisture at the supply point.

D.8 QUALIFICATION

D.8.1 Description of qualification. The following criteria have traditionally been used to qualify all processes and materials used in the manufacture of chip and wire devices. It may not, however, be adequate for all, or new, technologies, in which case it shall be used as a starting point for developing a qualification program. These criteria are intended to be used to characterize all process and materials used in the manufacture of the device. These criteria shall be used to determine the acceptability of the processes and materials. All parts built using processes and materials that have successfully completed characterization and have been verified by the qualifying activity are considered qualified.

D.8.2 Rework qualification. Devices containing any unqualified rework shall not be shipped until the rework has been successfully qualified. The rework and repair provisions shall apply.

D.8.2.1 Qualification of rework. If any rework is to be qualified, and unless otherwise allowed, the manufacturer shall build a qualification lot of reworked devices in which certified rework processes are performed. Standard evaluation circuits may be used. Qualification of rework by this method may require qualifying activity approval of the test plan and authorization to test (ATT) prior to assembly of the lot. Rework qualification without approval is at manufacturer's risk.

D.8.2.2 Delid/relid rework qualification procedures. Delid/relid rework shall require qualifying activity approval of the test plan and ATT prior to assembly of the lot.

D.8.2.3 Alternate qualification procedures for die/wire bond rework. The manufacturer may elect to review the initial production lot(s) from which qualification samples are selected for the occurrence of certified rework processes. The devices containing the rework to be qualified shall be among those selected for qualification. If the amount of rework that was performed does not meet the sample size requirements, then additional die/bond rework shall be performed on the selected rework samples, or more rework samples shall be selected to meet the minimum sample size requirements. If the initial qualification does not cover all certified rework, then subsequent production lot(s) shall be reviewed for the occurrence of the unqualified rework until all certified rework is qualified.

D.8.3 Qualified manufacturers list (QML) qualification lot. The manufacturer may elect to perform the QML qualification in accordance with D.8.6 on an inspection lot of shippable product; or the manufacturer may choose to build a lot of devices specifically for QML qualification and test them in accordance with D.8.6. Devices specifically built for QML qualification may either be actual product or standard evaluation circuits. Actual products from the qualification lot testing are shippable as a compliant product after successful completion of qualification and applicable PI testing.

D.8.4 Qualification test requirements. QML qualification shall be accomplished by successful performance of group C (PI/QML) testing as specified in D.7.5 herein.

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D.8.5 Qualification to electrostatic discharge sensitivity (ESDS) classes. Initial qualification to an ESD class or re-qualification after a major change shall consist of determining the ESD level in accordance with any one of the four following options.

(1) Testing the devices to Subgroup C5 of Table D-XVI for cavity and non-cavity non-hermetic devices, or Table D-XVIII for open non-hermetic devices using method 3015 of MIL-STD-883 to determine the actual ESD classification designators in accordance with 3.9.5.8.2.

(2) Testing the devices to Subgroup 5 of Table D-XVI for cavity and non-cavity non-hermetic devices, or Table D-XVIII for open non-hermetic devices using method 3015 of MIL-STD-883 using alternate testing method to test once at 250 V to determine ESD classification designator 0 or 1A IAW 3.9.5.8.2.

NOTE: If any device(s) fail at 250 V, it is classified as Class 0. If all devices pass at 250 V, it is classified as Class 1A.

(3) Classifying the hybrid to the lowest electrostatic voltage class level of the active devices ESDS listied in accordance with MIL-PRF-38535 that are accessible to leads of the device by analysis. Support data (from device testing or IC manufacturer's ESD results) shall be retained by the hybrid manufacturer for all device types compliant with this specification.

(4) Classify the hybrid device as Class 0 (see 3.9.5.8.2 herein) without performing the ESD testing.

D.8.6 QML-38534 qualification. All tests, test methods, test conditions, and limits shall be in accordance with MIL-STD-883 and as specified herein. If a qualification lot is withdrawn due to (1) failing to meet qualification requirements or (2) lack of failure analysis or corrective action, and (3) no retesting is performed, the certification of the process or material (or both) to be covered by that qualification shall be removed by the qualifying activity.

NOTE: The device manufacturer has the right to select not to use any solution or solvent identified within this specification, or related specifications, that has also been identified by the American Congress of Government Industrial Hygienists as being a potential or suspect carcinogen. Where the device manufacturer elects not to use a material, they shall notify the acquiring or qualifying activities and the customer in writing in clear, unambiguous language not subject to misinterpretation that this right has been exercised.

D.8.6.1 Qualification eligibility. All processes to be qualified and which are to be included on QML-38534 shall have been certified by the qualifying activity in accordance with 4.5.1.2 herein.

D.8.6.2 Test samples. Devices used for qualification shall have been assembled using certified process (or as allowed by the qualifying activity) and screened in accordance with the applicable sections of D.6 herein. Qualification tests shall be performed at facilities which have a laboratory suitability granted by the qualifying activity or approved by the manufacturer's TRB. DLA Land and Maritime Form VQH-42H, "Device Product Baseline", or its equivalent shall be used to baseline the specific processes and materials used in the qualification device.

D.8.6.2.1 Standard evaluation circuits. The manufacturer may elect to design and build a functional standard evaluation circuit (device) in lieu of utilizing actual product. If qualification is to be performed on a lot of devices built specifically for QML qualification, the device shall be representative of the physical complexity of the product that shall be covered by its testing. Standard evaluation circuits shall not be used for group C2 (life test) product qualifications.

D.8.6.2.2 Sample selection. The sample size shall be selected in accordance with D.7.2.3 herein and the corresponding subgroups of the group C, table D-XV through D-XIX, as applicable. Except for designated rework and nonfunctional devices (D.7.2.3.1), test samples shall be randomly selected from the inspection lot. The manufacturer shall retain a sufficient number of test devices from the lot to designate reserve samples.

D.8.6.2.3 Rework samples. For approval of rework qualification, the rework sample shall be prepared in accordance with the manufacturer's baselined rework procedure. Three out of five devices tested in group C, subgroup 1 shall have undergone the rework to be qualified. The die and wire sample size requirements of D.8.6.4.13 and D.8.6.4.14 shall be applied to reworked wire bonds and replaced die. Each rework method shall be considered a different process.

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D.8.6.2.4 Non-functional samples. Electrical rejects from final electrical testing in screening can be used in any subgroup of qualification tests where electrical testing is not required (e.g., for subgroup C4, the rejects shall be subjected to subgroup C1 prior to testing to subgroup C4).

D.8.6.2.5 Disposition of samples. Samples destructively tested during qualification testing shall be submitted to the qualifying activity with the qualification test report. Other devices in the qualification inspection lot shall be properly disposed of.

D.8.6.3 Test failures.

D.8.6.3.1 Resubmission of failed samples or lots (or both). Unless otherwise specified, resubmission of failed samples, or additional samples from the same production lot, are not allowed unless such failures are due to equipment or operator errors in accordance with Appendix A. Notification of the qualifying activity is required.

D.8.6.3.2 Failures. All test failures shall be reported to the qualifying activity, along with (if applicable) the resulting failure analysis and corrective actions needed to assess qualification status or alternatives.

D.8.6.4 Technology capability verifications. Tables D-XV, XVI, and D-XVIII (as applicable) detail the testing requirements for qualification (PI/QML) for either Class F or Class L devices.

D.8.6.4.1 Preconditioning. Preconditioning shall apply to cavity, non-cavity non-hermetic, and OA devices if soldering with flux and cleaning of the flux is required for the device. If the non-hermetic device is not exposed to solder reflow conditions, then preconditioning in accordance with table D-XV is not required to be performed. If the non-hermetic device is exposed to hand solder conditions, then an alternate preconditioning method shall be approved.

D.8.6.4.2 PIND. For cavity, and OA devices, the devices shall show no evidence of loose particles. Any device showing loose particles when tested as specified herein shall be analyzed. Failure of PIND shall not jeopardize qualification provided the manufacturer demonstrates that the loose particle control is established and random samples, from product fabricated using the baselined process, are PIND tested after corrective action implementation. These random samples shall have been screened (see D.6). The retest requirements shall be determined based on the nature of the changes made as a result of the corrective action. Compliant Class F shall receive 100 percent PIND screening until the manufacturer demonstrates to the qualifying activity that these requirements are met.

D.8.6.4.2.1 Loose particle recovery. The loose particles that caused the failures shall be recovered and analyzed for the cause and source. If the analysis fails to locate the particles causing failure, the device shall be carefully delidded and examined in an attempt to locate the particles. Captured particles shall be evaluated at 30X minimum and the offending portion of the process shall be identified and corrected.

D.8.6.4.3 Temperature cycling. Temperature cycling shall be performed in accordance with method 1010 of MIL-STD-883.

D.8.6.4.4 Aging tests. Autoclave, steady-state, temperature humidity bias life test, or highly accelerated temperature and humidity stress test (HAST) shall be performed in accordance with JESD22 methods.

D.8.6.4.5 Constant acceleration. For cavity, and OA devices, constant acceleration shall be performed in accordance with method 2001 of MIL-STD-883. A stiffener plate (e.g., .125 inch (3.18 mm)) aluminum) may be attached to the base of the package to prevent damage due to "oil canning" of the package.

NOTE: Constant acceleration is optional based on design for non-cavity devices (e.g. soft encapsulation may require constant acceleration).

D.8.6.4.6 Random vibration. For cavity, and OA devices, random vibration shall be performed in accordance with method 2026 of MIL-STD-883.

NOTE: Optional based on design for non-cavity devices (e.g. soft encapsulation may require random vibration).

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D.8.6.4.7 Mechanical shock. For cavity, and OA devices, mechanical shock shall be performed in accordance with method 2002 of MIL-STD-883. Constant acceleration is not an option in place of mechanical shock. Both tests are required for qualification.

NOTE: Optional based on design for non-cavity devices (e.g. soft encapsulation may require shock).

D.8.6.4.8 Seal (gross leak only with no type 1 detector fluid or pressurization bomb). For cavity devices, seal test (gross leak only with no type 1 detector fluid or pressurization bomb) shall be performed in accordance with method 1014 of MIL-STD-883.

D.8.6.4.9 Seal (fine and gross leak for OA devices with hermetically sealed hybrid or multichip module(s)). For Class L and F devices, the seal test may be performed between the constant acceleration/mechanical shock test (or PIND test, if applicable) and external visual, but it shall be performed after all shearing and forming operations on the terminals.

D.8.6.4.10 IGA for OA devices only. An internal gas content sample of three devices (zero failures) will be selected from the subgroup 1 sample. The use of screened electrical rejects, or representative mechanical samples, is permissible provided these samples have seen, as a minimum, the environmental exposures required in subgroup 1 (e.g. temperature cycle or thermal shock, mechanical shock of constant acceleration, and seal tests as applicable). The internal gas analysis shall meet the requirements of method 1018 of MIL-STD-883.

D.8.6.4.11 External visual. The external visual shall be in accordance with method 2009 of MIL-STD-883.

D.8.6.4.12 End-point electrical requirements. End-point electricals shall be measured (and recorded when required) before starting and after completion of all tests in subgroups 1 and 2 of group C and preconditioning tests. Data from group A, or final electrical test, may be used as the initial end-point electrical before starting preconditioning, subgroup 1 and 2. Electrical end-point limits, life test conditions, and intermediate measurement requirements shall be specified as required by the applicable device specification. Test samples which require variable data shall be serialized prior to tests.

D.8.6.4.13 Steady-state life test. Steady-state life testing shall be performed on each initial lot of each device type. If group C, subgroup 2 testing is being performed for PI/QML qualification only, the sample size shall be five with zero failures allowed. In addition, if group C2 testing is being performed for PI/QML qualification only and life test has previously been completed, a 1,000-hour bake at +150°C followed by end-point electrical testing may be performed in lieu of steady-state life testing.

D.8.6.4.14 Internal visual and mechanical. The criteria of method 2014 of MIL-STD-883 shall verify that no damage has occurred to, and no contamination is present on, the elements and substrate. Non-cavity devices that are de-capsulated shall be performed with care to prevent damage during the process. Inspection shall ignore residue encapsulation from the de-capsulation process.

D.8.6.4.15 Wire bond strength for QML qualification. Two devices minimum shall be tested to assure the post-seal bond strength requirements of method 2011 of MIL-STD-883. The bond strength test shall be performed on a sample size (accept number) of 44 (0) bond wires, or all wires in the device for each wirebond process and material (wire metallization) present in the device can be qualified by that sample. As a minimum, wires tested shall include one each from a typical transistor, diode, capacitor, and resistor die, three wires from each IC and five wires from the package to the substrate, as applicable. Each rework process shall be performed on a sample size of 5 (0) or all wires reworked in each device For wire rework, the test wires shall be predesignated. No failures shall be allowed.

NOTE: A minimum of two devices, or all five QML devices, may be tested for wire bond strength qualification. The number of wires tested may be less than the minimum required if the five samples do not meet the minimum amount of bonds required.

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D.8.6.4.16 Element shear for QML qualification. Two devices minimum shall be tested to assure the die shear strength requirements of method 2019 of MIL-STD-883. The die shear test shall be performed to a quantity (accept number) of 5 (0) elements for each element attach process (including element rework as a separate process) and material present in the device. The materials considered shall include the attach medium, element backing, and element attach area surface. Each five piece sample of elements shall contain an even distribution of all element sizes that can be qualified by that sample. No failures shall be allowed. Additional devices will be added, if necessary, to meet the required element sample size. For element rework, the elements shall be pre-designated.

D.8.6.4.16.1 Alternative to element shear testing. The manufacturer may utilize method 2027 of MIL-STD-883, to test the strength of organic and solder/alloy attachments on selected elements, except that the accept/reject criteria shall be based on an acceleration on the element of 50,000 g's in the Y1 direction (i.e., the minimum acceptable pull strength shall be 50,000 times the weight of the element).

NOTE: This alternative test is only appropriate for elements whose element thickness, or mass, is small in proportion to the area of attach (e.g., 10 mil thick GaAs die). The acceptance level is more severe than die shear testing for many element types. In cases where the element is relatively massive compared to the attachment area (e.g., tantalum capacitors), this method shall give a false indication of die attach strength, pass or fail.

D.8.6.4.17 Outside lab testing. For cavity, OA, or non-cavity devices, de-capsulation, internal visual mechanical, bond strength, and die shear may be performed by an outside lab.

D.8.6.4.18 Ultrasonic inspection. Ultrasonic inspection is used to detect cracking and delamination during preconditioning and during the PI/QML test process. Ultrasonic inspection is a tool to assist in determining potential failure modes during the process and is not used for accept/reject criteria.

D.9 NOTES

D.9.1 Intended use. Non-hermetic and OA devices conforming to this specification are intended in use for microcircuit applications and logistic purposes. For maximum cost effectiveness while maintaining essential quality and reliability requirements, it is recommended that, for initial acquisitions for original equipment complements, the device class appropriate to the need of the application be acquired. For acquisition of spare parts for logistic support, it is recommended that, unless otherwise specified, all devices be acquired to Class F requirements.

D.9.2 Acquisition requirements. Acquisition documents should specify the following:

a. Title, number, and date of this specification.

b. Packaging requirements (see 5.1 herein).

c. PIN.

d. Title, number, and date of applicable device specification and identification of the originating design activity.

e. Device finishes.

f. Product assurance level (see D.1.3).

g. Change notification (i.e., point of contact).

D.9.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the acquisition documents.

a. Requirements for failure analysis.

b. Special requirements. (i.e., outside lab report, report documentation, data).

c. Disposition of samples.

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d. Requirement for conformance inspection (CI) and periodic inspection (PI) or Qualified Manufacturer's List (QML) plan.

e. Requirement for periodic process monitoring.

D.9.2.2 End item applications. The non-hermetic device application should address the end item application. The following concerns should be considered:

a. Solvent effect on the non-hermetic construction and materials.

b. Integrity of device after exposure to environments (temperature, mechanical, atmospheric pressure, moisture).

c. Permeation of moisture and contaminants through the package and seals and effects on interfaces and elements.

d. Subsequent processing effects on reliability.

e. Life cycle environments in the next higher assembly.

f. Interconnection to the next assembly level.

g. Special cleaning processes required at manufacture and customer.

h. Customer awareness of handling requirements.

i. Special handling and contamination controls in assembly, transportation, storage, unit packaging.

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APPENDIX D

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APPENDIX E

GENERIC DESIGN AND CONSTRUCTION CRITERIA

E.1 SCOPE

E.1.1 Scope. This appendix is intended to present the generic design and construction criteria which will be addressed by the manufacturer. The criteria of this appendix may be modified as described in this specification. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance. Manufacturers may demonstrate a design and construction system that achieves as least the same level of quality as could be achieved by complying with this appendix.

E.1.2 Description of appendix E. This appendix will describe the generic design and construction criteria of this technology and is presented as requirements for conformance.

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E.2 APPLICABLE DOCUMENTS

E.2.1 General. The documents listed in this section are specified in sections E3, E4, or E5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections E3, E4, or E5 of this specification, whether or not they are listed.

E.2.2 Government documents.

* E.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil).

E.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

E.3 REWORK LIMITATIONS

E.3.1 Description of the rework limitations. This section describes a typical rework program, including limitations and testing required to ensure that reworked devices are capable of meeting the performance requirements of this specification.

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E.3.2 Rework and repair provisions. All rework and repair permitted on devices will be accomplished in accordance with procedures and safeguards documented in accordance with Appendix A. This documentation will reflect the processes, procedures, and materials to be used including verification or test data. Each process or procedure will be designated as rework or repair. This documentation will indicate that a decision to rework is made solely by the manufacturer while a repair decision will be made with the concurrence of the customer, except for repairs permitted by this specification. A typical example of rework is the removal of a defective element and replacement with a new element. An example of repair is the use of an organically attached molytab to replace a previously alloy attached semiconductor element.

E.3.2.1 General rework and repair provisions.

a. All temperature excursions during any rework or repair will not exceed the baselined rework or repair limitations. Time and temperature limits will be specified.

b. Replate of package sealing surface on delidded packages is not permitted.

c. The minimum distance between the glass-to-metal seals and the package sealing surface will be at least .040 inch (1.02 mm) after final seal to prevent damage to lead seals by welding adjacent to them. (Applies to seam welding only.)

d. For Class H devices, any device that is reworked or repaired after pre-seal visual inspection will be subjected to full screening or rescreening as applicable. If a device has not been subjected to a given required screen prior to rework or repair, then that device will be subjected to that screen after rework or repair. If a device has been subjected to a given screen prior to rework or repair, then rescreening applies as follows:

    (1) Pre-seal visual inspection. Inspect for general damage (low magnification in accordance with method 2017 and method 2032 of MIL-STD-883) which might have been caused by the rework or repair and perform a complete method 2017 or method 2032 inspection of the reworked or repaired element or area (e.g., replaced die, wire bonds).

    (2) Temperature cycle or shock, mechanical shock or centrifuge, seal, and external visual. Rescreen all rework or repair devices 100 percent.

    (3) Burn-in. Devices delidded to rework package seal failures do not require burn-in rescreen. Devices which have had elements reworked, have been wire bonded or rewire bonded, or have been active trimmed/tuned require 100 percent burn-in rescreen.

e. Class K devices that are reworked or repaired prior to sealed burn-in shall be (re)screened as follows:

    (1) If no active elements or wire bonds affecting them have been replaced, full (re)screening shall apply with the following allowances:

        (a) Only the replacement wires need be non-destructively pull tested.

        (b) Pre-seal burn-in need not be repeated.

        (c) Post-seal burn-in may be reduced to 240 hours at 125°C, or at the time temperature equivalent, provided total burn-in (pre-seal and post-seal) on active devices is 320 hours or at the time temperature equivalent.

    (2) If active elements or wire bonds affecting them have been replaced, full (re)screening shall apply with the following allowances:

        (a) Only the replacement wires need be non-destructively pull tested.

        (b) Pre-seal burn-in need not be repeated.

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(c) Total burn-in (pre-seal plus post-seal) shall be 320 hours at 125°C, or at the time temperature equivalent.

f. Class K devices that are reworked or repaired after sealed burn-in.

(1) If no active elements or wire bonds affecting them have been replaced, full (re)screening shall apply with the following allowances:

(a) Only the replacement wires need be non-destructively pull tested.

(b) Pre-seal burn-in need not be repeated.

(c) Sealed burn-in may be reduced to 240 hours at 125°C, or at the time temperature equivalent if burn-in was previously performed.

(2) If active elements or wire bonds affecting them have been replaced, full (re)screening shall apply as follows:

(a) Only the replacement wires need be non-destructively pull tested.

(b) Pre-seal burn-in need not be repeated.

(c) Burn-in (pre-seal plus post-seal) shall be 320 hours at 125°C, or at the time temperature equivalent.

g. When flux is required for rework or repair, the specific flux and detailed procedures for its use and subsequent special cleaning operations will be documented and approved in accordance with Appendix A.

h. Replacement elements will not be bonded onto the chip element they are to replace.

E.3.2.2 Element wire rebonding. Wire rebonding of elements other than substrates, thick film elements, capacitors, and package posts will be permitted with the following limitations:

a. No scratched, voided, or discontinuous paths or conductor patterns on an element will be repaired by bridging with, or addition of, bonding wire or ribbon.

b. All rebonds will be placed on at least 50 percent undisturbed metal (excluding probe marks that do not expose underlying oxide). No more than one rebond attempt at any design bond location will be permitted. No rebonds will touch an area of exposed oxide caused by lifted or blistered metal. Bond-offs required to clear the bonder after an unsuccessful bond attempt need not be visible, will not be cause for reject and will not be counted as a rebond. For Class K, the total number of rebond attempts (exclusive of element replacement or tuning wire replacement) will be limited to a maximum of 10 percent of the total number of bonds in the device. The 10 percent limit on rebond attempts may be rounded to the nearest whole number to the 10 percent value.

E.3.2.3 Substrate, thick film elements, capacitors, and package post wire rebonding or repair. Wire rebonding on substrates and package posts will be permitted with the following limitations:

a. Scratched, open, or discontinuous substrate metallization paths or conductor pattern on a substrate, not caused by poor adhesion, may be repaired by bridging with, or by addition of, bonded conductors having current carrying capacity at least three and one-half times the maximum calculated operating load current for the conductor or three and one-half times the current capacity of the wire bond connection terminating on the damaged conductor path. The quantity of repairs will be limited to one for each one-half square inch, or fraction thereof, of substrate area. This repair is not applicable to thick film elements, capacitors, or package posts.

b. No rebonds will be made over intended bonding areas in which the top layer metallization has lifted, peeled, or has been damaged such that underlying metallization or substrate is exposed at the immediate bond site.

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E.3.2.4 Compound bonding. Compound bonding is permitted only as follows:

a. When required for design, rework, or repair, gold compound bonds will be limited to one bond over the original bond, wire, or ribbon.

b. Only monometallic compound bonds of the same size wire or ribbon are permitted (i.e., the original bond wire and that used for compound bonding shall be the same material).

c. For rework or repair, the maximum number of compound bonds will not exceed 10 percent of the total number of wires.

d. For rework or repair, a corrective action system shall be utilized in order to reduce the number of compound bonds.

e. For rework or repair, all compound bonds will be 100 percent non-destructive pull tested in accordance with method 2023 of MIL-STD-883.

f. A compound bond will not be used to connect two wires.

g. All compound bonds will meet the visual criteria in method 2017 of MIL-STD-883.

E.3.2.5 Element replacement. Element replacement will be permitted with the following limitations:

a. Any polymer attached element may be replaced two times at a given location on any device. Any element attached with polymer to metal, other than substrate metallization (e.g., pedestals, ribs, carriers) may be replaced four times at a given location. The number of polymer attached tuning element replacements will be defined in the manufacturers' baseline documentation, and approved by the qualifying activity.

b. Any metallic attached element may be replaced one time at a given location.

c. Any metallic attached element onto a plated tab, where the tab is attached to a substrate with a higher temperature metallic attach process, may be replaced two times.

d. Substrates may be removed, replaced, or put into a new package one time. This restriction does not apply to substrates attached into a package using mechanical fasteners.

E.3.2.6 Seal rework. The use of polymers to affect, improve, or repair any hermetic package seal will not be permitted.

E.3.2.6.1 Lid seal rework. It will be permissible to perform seal rework without delidding on devices that fail fine leak testing one time, only if tracer gas is included during the original sealing operation and under all of the following conditions:

a. Fine leak testing, without pressurization (bomb), shall be performed immediately after sealing prior to any other test.

b. Devices will be stored in a nitrogen environment for a maximum of 4 hours between initial seal and reseal without replacing the cover.

c. Devices will be submitted to a predetermined vacuum bake prior to reseal.

d. Solder sealed packages may not be reworked in accordance with this procedure.

NOTE: The above leak testing will not be used as a substitute for the fine leak testing.

E.3.2.6.2 Other seal rework. It will be permissible to rework other seals (e.g., feed-throughs, connectors, seal plugs, or windows) at metal-to-metal interfaces on unlidded devices.

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E.3.2.7 Delidding of devices. Devices may be delidded and relidded for rework or repair provided the delid-relid procedures, controls, and resulting data are baselined. The number of delid-relid cycles allowed will be in accordance with E.3.2.7.1 or E.3.2.7.2. Delid-relid history (i.e., traceability by lot number or serial numbers) will be maintained by the device manufacturer.

E.3.2.7.1 Solder sealed devices. Class H solder sealed devices may be delidded-relidded one time. Class K solder sealed devices may not be delidded-relidded.

E.3.2.7.2 Welded devices. Only seam sealed, overlapping pulse welded, or laser welded packages designed for delid-relid may be delidded-relidded. Devices may be delidded-relidded N times, with N = 2 maximum for Class K.

E.4 DESIGN AND CONSTRUCTION

E.4.1 Description of design and construction. This section describes a typical design and construction program used to ensure that these devices will be capable of meeting of the performance requirements of this specification.

E.4.2 Design and construction. Device design and construction will be in accordance with the requirements specified herein and the device specification. The design will be capable of passing all applicable tests and screens (see Appendix C).

E.4.2.1 Package. Devices will be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. The following provisions apply to package construction and sealing:

a. No adhesive or polymeric materials will be used for package lid, or feedthrough, attach (or seal) or rework/repair.

b. Polymer impregnations or secondary seal (backfill, coating, other uses or organic or, polymeric materials to effect, improve, or rework/repair the seal) on the device package will not be permitted.

c. Flux will not be used in the final sealing process.

d. In the case of final lid seal using a welding process, sufficient distance will be maintained between the lid seal and any glass-to-metal seal so as to preclude damage or degradation of the glass-to-metal seal.

e. Package materials will be selected such that thermal expansion rate mismatches between different materials do not compromise package integrity or hermeticity during applicable temperature excursions.

E.4.2.2 Polymeric materials. The cure temperature of polymeric materials will not be exceeded after completion of final seal. Polymeric materials will meet the requirements of method 5011 of MIL-STD-883. For materials outside the scope of method 5011, the manufacturer will develop an alternative plan.

E.4.2.3 External metals. External metal surfaces, other than seal weld areas, will meet the applicable corrosion resistance requirements, or will be plated to do so.

E.4.2.4 Other external materials. External parts, elements, or coatings, including markings, will be non-nutrient to fungus and will not blister, crack, flow, or exhibit defects that adversely affect storage, operation, or environmental capabilities of the device under the specified test and operating conditions.

E.4.2.5 Design and manufacturing documentation. Design, topography, schematic circuit information, manufacturing flowcharts, and process control documents for all devices will be available for review by the acquiring activity and the qualifying activity. This documentation will depict the physical and electrical construction of the device. Each device will be traceable to a specific part, drawing, or type number, and to the production lot and inspection lot codes under which devices are manufactured and tested (so that revisions can be identified).

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E.4.2.5.1 Schematic diagrams. The device schematic diagram, logic diagram, or combination thereof, will be available with sufficient detail to represent all electrical elements functionally designed into the device together with their values (when applicable). For complex devices, or those with redundant detail, the overall device may be represented by a logic diagram in combination with schematic details.

E.4.2.6 Internal conductors. Internal thin film conductors on elements (e.g. metallization stripes, contact areas, bonding interfaces) and internal wires (e.g. wires, ribbons) will be designed such that no properly fabricated conductor will experience current in excess of the maximum value calculated by the manufacturer to preclude damage or degradation to the conductors, except by design (e.g., internal fuses). The following conditions will be considered when calculating the maximum current:

a. Calculate the current density at the point of maximum current density (i.e., greatest current in accordance with unit cross section) for the specified device type.

b. Use a current value equal to the maximum continuous current (at full fan-out for digitals or at maximum load for linears) or equal to the simple time-averaged current obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point of maximum current density. This current value will be determined at the maximum recommended supply voltage and with the current assumed to be uniform over the entire conductor cross-sectional area.

c. Use the minimum allowed metal thickness in accordance with manufacturing specifications and controls including appropriate allowance for thinning experienced in the metallization step (via). The thinning factor over a metallization step is not required unless the point of maximum current density is located at the step.

d. Use the minimum allowable actual conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

e. Do not include areas of barrier metals and non-conducting material in the calculation of conductor cross-section.

E.4.2.7 Device finishes. Tin is prohibited as a final finish and as an undercoat. The use of tin-lead finish is acceptable provided that the lead content is a minimum of 3 percent by weight.

E.4.2.7.1 Internal element finishes. Finishes on interior elements (e.g., bonding pads, posts, tabs, element backing, element leads, and attach material) shall be such that they meet lead and element bonding requirements and any applicable design and construction requirements. The use of pure tin on interior elements is prohibited. Tin lead alloy with a minimum of 3 percent lead is acceptable on interior elements. Tin alloys other than lead used on interior elements or as an attach material require that the tin content be less than or equal to 97 percent and require approval of the qualifying activity and notification of the acquiring activity.

E.4.2.7.2 External element finishes. Finishes of all external leads, or terminals, and all external metallic package/lid elements will meet the applicable corrosion resistance requirements.

E.4.2.7.3 External lead finish. Lead finish thickness measurements will be taken halfway between the seating plane and the tip of the lead. The finish system on all external leads or terminals will conform to one of the following:

a. Hot solder dip. The hot solder dip will be homogeneous with a minimum thickness of 60 microinches (1.52 μm) for round leads and, for other shapes, a minimum thickness at the crest of the major flats of 200 microinches (5.08 μm) solder (SN60 or SN63). For leadless chip carrier devices, the solder will cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch (except the index feature if not connected to the castellation). Terminal area intended for device mounting will be completely covered. The hot solder dip on leads is applicable to either E.4.2.7.3.a.(1) or E.4.2.7.3.a.(2) as follows:

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(1) All outlines with hot solder dip over a finish with c or d as follows. The hot solder dip shall extend beyond the effective seating plane. If the seating plane is not defined, the hot solder dip shall extend to within .040 inch (1.02 mm) of the lead/package interface and is bound by the lead/package interface. For dual inline type termination forms (through hole and surface mount), the plane of the two longest lead/package interfaces will define this bound. For leadless chip carrier devices, the hot solder dip shall cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch, except the index feature if not connected to the castellation. Terminal area intended for device mounting shall be completely covered.

(2) All outlines with hot solder dip over base metal or noncompliant coating. The solder shall extend to the glass seal or point of emergence of the metallized contact or lead through the package wall. If solder is applied up to the seal, a hermeticity test and external visual in accordance with C.5.11.c shall subsequently be performed and passed. For leadless chip carrier devices, the hot solder dip shall completely cover the metallized side castellation or notch and metallized areas above and below the notch, except the index feature if not connected to the castellation

b. Tin-lead plate. Tin-lead plate will have in the plated deposit 3 percent to 50 percent by weight lead (balance nominally tin) co-deposited. As plated tin-lead will be a minimum of 300 microinches thick and will contain no more than 0.05 percent by weight co-deposited organic material (measured as elemental carbon). Tin-lead plating may be fused by heating above its liquidus temperature. Fused tin-lead will be a minimum of 200 microinches thick. Tin-lead plate is applicable:

(1) Over a finish in accordance with entry c as follows, or

(2) Over the basis metal.

c. Nickel plate or undercoating. Electroplated nickel, or electroless nickel phosphorous nickel undercoating, or finishes, will be 50 to 350 microinches (1.27 μm to 8.89 μm) thick measured on major flats or diameters. Electroless nickel will not be used as the undercoating on flexible or semiflexible leads and will be permitted only on rigid leads or package elements other than leads (see method 2004 of MIL-STD-883 for definitions of flexible and semiflexible leads).

Combinations of pre-plate electroplate or electroless nickel and final electroplate nickel finishing shall not exceed 700 microinches/17.78 micrometers total. Combinations of pre-plate electroplate nickel and final electroless nickel plate finishing shall not exceed 600 microinches total.

d. Gold plate. Gold plating will be a minimum of 99.7 percent gold, and only cobalt will be used as the hardener. Gold plating will be a minimum of 50 microinches (1.27 μm) and a maximum of 225 microinches (5.72 μm) thick. Gold plating will be permitted only over nickel plate or undercoating in accordance with c above.

E.4.2.8 Thermal design. Thermal design analysis will be performed and will establish, as a minimum, that functional device elements are operating within their design temperature ratings when the device is operated at the specified maximum operating case temperature. Finite element analysis is an acceptable thermal design analysis technique. All active and passive elements will be derated.

E.4.2.9 Electrical circuit design. Circuit design analysis shall be performed in accordance with the manufacturer's internal procedure and shall include the following evaluations as a minimum (applicable to the design):

a. Electrical element stress over the specified operating temperature range will be within the specified derating criteria under worst case temperature (Tc, Ta or Tj) conditions.

b. Evaluated to meet the Group A CI test limits at worse case operating temperature (Tc, Ta or Tj) conditions, as applicable.

E.4.2.10 Assembly process induced environments. When the next level assembly environment (e.g. solder attach to a board assembly) is specified, the design and construction shall be considered.

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E.5 MAJOR CHANGES

E.5.1 Description of major changes. This section describes how to handle major changes to devices or processes.

E.5.1.1 Manufacturer controls. The manufacturer is responsible for controlling all materials and processes (see A.3.2.3) involved in the production of devices compliant to this specification. Any change to the supplier, materials, or processes which may impact the reliability and performance of the final device, will be controlled and evaluated by the manufacturer. This may include documentation of all changes, additional testing of devices, and/or notification of customers and the qualifying activity. This includes obsolescence and availability issues.

E.5.2 Class I, major changes. A thorough description of the proposed change, acceptable engineering data, and a suggested test plan designed to demonstrate that the changed product will continue to meet the acquisition document requirements including performance, quality, reliability, radiation hardness assurance (when specified), or interchangeability will be generated and provided to the qualifying activity for review and approval. The manufacturer will proceed with the change after approval of the test plan. To minimize the need for additional tests due to insufficient details or data regarding the proposed changes, it is recommended that the test plan be discussed with the acquiring or qualifying activity prior to commencing the test program. Test guidelines for each major change listed herein are provided in table E-I for product design changes (column CI and PI) and baselined process changes (column QML). The subgroup designations in table E-I correspond with the subgroups designated in tables C-Xa, C-Xb, C-Xc, and C-Xd of Appendix C. Tests will be performed on samples of the first devices or subassemblies manufactured incorporating the changes. Upon completion of the prescribed test program, the results will be recorded and available for review. At the manufacturer's option, devices incorporating the change may be manufactured and tested prior to approval; however, all shipments of these changed devices will be withheld until formal documented approval is granted by the acquiring activity or qualifying activity. Changes representative of those which are subject to the requirement are:

a. Change of substrate material (e.g., alumina versus BeO).

b. Change of materials or inks deposited on the substrate (e.g., (1) Conductor: Gold versus copper; (2) Resistor: Ruthenium base versus carbon) or deposit method (e.g., thin film versus thick film).

c. Cumulative change of nominal process time of deposited materials exceeding 25 percent or nominal process temperature exceeding +50°C or 10 percent, whichever is greater, since the last qualification or major change notification.

d. Cumulative changes to substrate mask design that reduce nominal design dimensions, spacing, or isolation more than ±25 percent, or changes to electrical parameters of the deposited elements beyond the design limits since the last qualification or major change notification.

e. Change of trimming method (e.g., abrasive versus laser).

f. Increase in substrate fabrication multi-layer conductor levels more than one conductor level from the QML listing.

g. Change of attach material (e.g., epoxy A versus epoxy B) or of attachment method (e.g., epoxy versus eutectic) for device elements.

h. Change in the baselined attach process temperature for element or substrate attachment which exceeds +25°C or 10 percent, whichever is greater.

i. Change of die type (e.g., 2N2484 versus 2N2905) or other element types (e.g., tantalum versus ceramic capacitors or thin film versus thick film resistors) mounted on the substrate.

j. Change in element attach area of more than 50 percent, or a change in the distribution of the component mass relative to the area of attachment of more than 25 percent, on devices that contain magnetics, stacked elements, insulated wires, flex circuit, or high profile elements from the original QML listing.

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k. Change of baselined wire bond method (e.g., ultrasonic versus thermal compression) or wire size changes greater than 1.0 mil.

l. Any change in specified material composition or purity of the wire.

m. Increase in substrate attach perimeter more than 50 percent of the QML listing.

n. Change of package configuration (e.g., platform versus bathtub), lid or covers (e.g., step lid versus drawn cover) or plating material.

o. Change of package or lid base material (e.g., nickel versus stainless steel).

p. Changes to finished device dimensions exceeding the acquisition document, or SMD envelope tolerances.

q. Change of seal method (e.g., seam weld versus laser weld), or seal material (e.g., SnAg versus AuSn).

r. Change in the baselined seal process time, temperature, or vacuum of more than 10 percent, or sealing atmosphere, except for the addition of helium.

s. Increase in package seal perimeter more than 50 percent from the QML listing.

t. Increase in lead count for QML listing in accordance with package type.

u. Changes to the baselined product flowchart in which element evaluation, screening, CI and PI options, and any operations are added or deleted, except for additional inspections and SPC operations.

v. Addition of new processes or materials to the QML.

w. Assembly operation or test facility move.

x. Class I and Class II changes for Class K.

y. Change of die manufacturer for class K devices, all Class I and Class II changes since the original baseline qualification (CI, PI, QML).

z. For radiation hardened devices, all Class I and class II as defined in Appendix G changes since the original baseline qualification (CI, PI, QML).

aa. Change of element backside or topside finish (e.g. palladium termination to gold, gold plated lead to nickel) from QML listing.

bb. Change affecting ESD level (e.g. 2N2484 versus 2N2905).

NOTE: Same element part number from a different manufacturer is not considered a major change, except for Class K. Change of die manufacturer is a major change for Class K as stated in item y. of this paragraph

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TABLE E-I. Testing guidelines for major product/process changes. 1/ 2/ 3/ 4/ 5/ 6/ 7/ 8/ 9/

NOTE: Table E-I provides examples for PI and QML tests to be performed for major changes. Consideration to increase or decrease the testing shall be given depending on existing data and on the particular circumstance. Manufacturers shall evaluate the impact of the change, determine any necessary testing, and notify the qualifying activity, acquiring activity or TRB.

Changes that may result in increased T_J of components shall be reviewed and, as necessary, justified through data on similar devices, or applications, or repeat life testing to demonstrate performance at the increased T_J. C2 need not be repeated where data exists to justify the increased T_J.

Major changes	Recommended test subgroups of table C-Xc, (unless otherwise specified)		Variable data required (subgroups)		Explanation for recommended test guideline
	PI	QML	PI	QML	
a. Change of substrate material	C1, C2, C3, C4	C1, C2, C3, C4	C2, C3, C4	C2, C3, C4	C1 then C4 will demonstrate mechanical integrity via electrical test, visual inspection (adhesion, cracking, delamination), bond strength, and die shear of the elements on the substrate. C2 will demonstrate electrical performance differences and long term reliability of substrate material change. C3 will validate outgas properties of substrate material.
b. Change of material deposited on substrate (1) conductor (2) resistor (3) dielectric (4) deposit method	 C1, C2, C4 C2 C2 C1, C4, C2	 C1 ,C2, C4 C1, C2 C1, C2 C1, C2, C4	 C2, C4 C2 C2 C2, C4	 C2, C4 C2 C2 C2, C4	C2 will demonstrate electrical performance differences and long term reliability of deposited materials. C1 then C4 will demonstrate mechanical integrity via electrical test, visual inspection (adhesion, cracking, delamination), bond strength, and die shear of the elements on the substrate material.
c. Process/time/ temperature changes	Notify qualifying activity with recommendation	Notify qualifying activity with recommendation	N/A	N/A	

See footnotes at end of table.

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TABLE E-I. Testing guidelines for major product/process changes – Continued.

Major changes	Recommended test subgroups of Table C-Xc (unless otherwise specified)		Variable data required (subgroups)		Explanation for recommended test guideline
	PI	QML	PI	QML	
d. Substrate mask design	Pre-cap, C2	N/A	C2	N/A	In-line pre cap inspection will validate the internal inspection and mechanical requirements. C2 will demonstrate electrical performance differences from Group A and long term reliability of the mask change.
e. Change of trim method	C2	C1, C2, C4	C2	C2, C4	C1 then C4 will demonstrate active trim integrity via electrical test; visual inspection, bond strength, and die shear will provide supporting data on the affects of the active trim. Group C2 will demonstrate electrical performance differences from Group A and long term reliability of trim method.
f. Increase in multi-layer conductor levels, more than one level	C1, C2, C4	C1, C2, C4	C2, C4	C2, C4	C1 then C4 will demonstrate mechanical integrity via electrical test; visual inspection (adhesion, cracking, delamination), bond strength, and die shear will verify the multilayer increase. C2 will demonstrate electrical differences from Group A and long term reliability.
g., h. Change of attach material or attach process temperature	C1 C3, C2 , C4 (no wire bond pull)	C1 C2, C3, C4 (no wire bond pull)	C2, C3, C4 (no wire bond pull)	C2, C3, C4 (no wire bond pull)	C1 will demonstrate mechanical integrity via electrical test. C3 will validate the process temperatures (cure time/temp, vacuum bake, etc). C4 (no wire pull) will demonstrate mechanical integrity via visual inspection (adhesion, cracking, delamination) and die shear of the elements on the substrate C2 will demonstrate electrical differences from Group A and long term reliability.

See footnotes at end of table.

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TABLE E-I. Testing guidelines for major product/process changes – Continued.

Major changes	Recommended test subgroups of table C-Xc, (unless otherwise specified)		Variable data required (subgroups)		Explanation for recommended test guideline
	PI	QML	PI	QML	
i. Change of die type 7/	C2	C2	C2	C2	C2 will demonstrate electrical differences from Group A and long term reliability.
j. Change in element attach area, or a change in the distribution of the component mass, relative to the area of attachment.	N/A	C1, C4 (no wire bond pull)	N/A	C4 (no wire bond pull)	This affects the attach interface. C1 then C4 (no wire bond) will demonstrate mechanical integrity via electrical test, visual inspection (adhesion, cracking, delamination), and die shear of the elements on the substrate.
k1. Change of baselined wire bond method	N/A	C1, C4 (no die shear)	N/A	C4 (no die shear)	C1 then C4 (no die shear) will demonstrate mechanical integrity via electrical test, visual inspection, and bond strength.
k2. Wire size change	C1, C4 (no die shear)	C1, C4 (no die shear)	C4 (no die shear)	C4 (no die shear)	C1 then C4 (no die shear) will demonstrate mechanical integrity via electrical test, visual inspection, and bond strength.
l. Change of wire bond material	C1, C4 (no die shear)	C1, C4 (no die shear)	C4 (no die shear)	C4 (no die shear)	C1 then C4 (no die shear) will demonstrate mechanical integrity via electrical test, visual inspection, and bond strength.
m. Increase in substrate perimeter from QML listing	N/A	C1, C3, C4 (no die shear, wire bond pull)	N/A	C3 C4 (no die shear wire bond pull)	C1 then C4 will demonstrate mechanical integrity via electrical test and visual inspection (adhesion, cracking, delamination). C3 will validate outgas of larger substrate.
n. Change of package or lid configuration, etc.	C1, C3	C1, C3	C3	C3	C1 will demonstrate mechanical integrity via electrical test. C3 will validate the integrity of the new package configuration.

See footnotes at end of table.

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TABLE E-I. Testing guidelines for major product/process changes – Continued.

Major changes	Recommended test subgroups of table C-Xc (unless otherwise specified)		Variable data required (subgroups)		Explanation for recommended test guideline
	PI	QML	PI	QML	
o. Change of package, lid base material	C1, C3	C1, C3	C3	C3	C1 will demonstrate mechanical integrity via electrical test. C3 will validate the integrity of the new package configuration.
p. Change to finished device dimensions	Notify acquiring activity	N/A	N/A	N/A	Notify acquiring activity.
q., r. Change of seal method, profile or seal material	C1, C3	C1, C3	C3	C3	C1 will demonstrate the package mechanical integrity and electrical test will validate the process changes. C3 will validate the new seal process.
s. Increase in package seal perimeter from QML listing	N/A	C1, C3	N/A	C3	C1 will demonstrate mechanical integrity via electrical test. C3 will validate the new package increase in package volume, processes related to the increased seal perimeter.
t. Increase in lead count for each package type from QML listing	N/A	C1 C3	N/A	C3	C1 then C3 will demonstrate the package mechanical integrity and electrical test will validate the package/process. Not required for ceramic packages.
u. Change to baselined product flowchart	N/A	Notify qualifying activity	N/A	N/A	Notify qualifying activity.
v. Addition of new process or material	N/A	Notify qualifying activity	N/A	N/A	Notify qualifying activity.
w. Assembly operation or test facility move	N/A	Notify qualifying activity	N/A	N/A	Notify qualifying activity.
x. Class I and Class II changes for Class K	Notify acquiring activity	N/A	N/A	N/A	

See footnotes at end of table.

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TABLE E-I. Testing guidelines for major product/process changes – Continued.

Major changes	Recommended test subgroups of Table C-Xc (unless otherwise specified)		Variable data required (subgroups)		Explanation for recommended test guideline
	PI	QML	PI	QML	
y. Change of die manufacturer for Class K devices	Notify the acquiring activity	N/A	N/A	N/A	Notify acquiring activity to determine the applicable re-qualification requirements for change of die manufacturer for Class K devices.
z. For radiation hardened devices, any changes that affects the radiation response of the device.	See Appendix G	See Appendix G	N/A	N/A	See paragraphs G.4.2 and G.4.3.2 in Appendix G.
aa. Change of element backside or topside finish material from QML listing	N/A	C1, C4	N/A	C4	This affects the attach interface. C1 then C4 will demonstrate mechanical integrity via electrical test, visual inspection will validate attach (inspect for cracks, fissures), and die shear will validate the attach strength to the new finish material.
bb. Change affecting ESD level	C5	C5	N/A	N/A	

1/ Sampling will be in accordance with Table C-Xc, of this specification.
2/ All electrical parameter testing will be in accordance with the device specification, drawing, or SMD.
3/ Data histograms providing a parametric data summary may be submitted in place of variables data.
4/ The acquiring or qualifying activity (or both) may add or reduce testing as warranted by device specification requirements, unique design, or process circumstances, after notification by the manufacturer.
5/ The acquiring activity will determine testing requirements for design changes affecting Class K devices.
6/ Notification is required at the time of acceptance of new order; or delivery on existing order, when changes are made to devices acquired to Specification Control Drawings.
7/ Review and determine if worst case circuit analysis or thermal analysis is required based upon the change.
8/ If QML is covered, then PI is not required to be performed.
9/ Group A testing is expected to be completed prior to any table E-I test.

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APPENDIX F

STATISTICAL SAMPLING

F.1 SCOPE

F.1.1 Scope. This appendix contains statistical sampling qualification procedures and general test and inspection procedures used throughout this specification. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

F.1.2 Description of Appendix F. This appendix contains general information and guidance to be used by manufacturers when testing and inspecting devices.

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F.3 GENERAL STATISTICAL SAMPLING	151
F.4 STATISTICAL SAMPLING PROCEDURES AND TABLE	152

F.2 APPLICABLE DOCUMENTS

F.2.1 General. The documents listed in this section are specified in sections F3, F4, or F5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections F3, F4, or F5 of this specification, whether or not they are listed.

F.2.2 Government documents.

* F.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.

(Copies of these documents are available online at https://quicksearch.dla.mil).

F.2.3 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

F.3 GENERAL STATISTICAL SAMPLING

F.3.1 Definitions. The following definitions will apply for all statistical sampling procedures:

a. Percent defective allowable (PDA) series: The PDA series is defined as the following decreasing series of PDA values: 50, 30, 20, 15, 10, 7, 5, 3, 2, 1.5, 1, 0.7, 0.5, 0.3, 0.2, 0.15, 0.1.

b. Tightened PDA inspection: Tightened PDA inspection is defined as inspection performed using the next PDA value in the PDA series which is lower than that specified.

c. Acceptance number (c): The acceptance number is defined as zero.

d. Rejection number (r): Rejection number is defined as one or more.

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F.3.2 Symbols. The following symbols will apply for all statistical sampling procedures:

a. c: Acceptance number.

b. r: Rejection number.

F.4 STATISTICAL SAMPLING PROCEDURES AND TABLE

F.4.1 General. Statistical sampling will be conducted using a sample size (accept number) method as specified in table F-I herein. The procedures specified herein are suitable for all quality conformance requirements.

F.4.1.1 Selection of samples. Samples will be randomly selected from the inspection lot or inspection sublots. For continuous production, the manufacturer, at their option, may select the sample in a regular periodic manner during manufacture provided the lot meets the formation of lots requirement.

F.4.1.2 Failures. Failure of a unit for one or more tests of a subgroup will be charged as a single failure.

F.4.2 Single-lot sampling method. CI and PI information (sample sizes and number of observed defectives) will be accumulated from a single inspection lot to demonstrate conformance to the individual subgroup criteria.

F.4.2.1 Sample size. The sample size for each subgroup will be determined from table F-I and will meet the specified sample size (accept number).

F.4.2.2 Acceptance procedure. If zero failures are found in the initial sample of the required sample size, the lot will be accepted. If the observed number of defectives from the initial sample is greater than zero, a second sample of double the initial sample size may be selected from the original sub(lot). The sub(lot) may be accepted if zero defectives are observed in this double-size sample.

F.4.2.3 One-hundred percent inspection. Inspection of 100 percent of the lot will be allowed, at the option of the manufacturer, for any or all subgroups other than those which are called "destructive". If the observed percent defective for the inspection lot exceeds the specified PDA series value for the sample size specified, the lot will be considered to have failed the appropriate subgroup. One-hundred percent sampling is required where lot size is smaller than the required sample size with zero defectives allowed. Resubmission of lots tested on a 100 percent inspection basis will also be on a 100 percent inspection basis and in accordance with the tightened PDA inspection criteria.

TABLE F-I. Sample size (accept number) sampling plan. 1/ 2/ 3/

PDA series	50	30	20	15	10	7	5	3	2
	Minimum sample size (accept number)								
Accept number c = 0, r ≥ 1	5(0)	8(0)	11(0)	15(0)	22(0)	32(0)	45(0)	76(0)	116(0)

PDA series	1.5	1	0.7	0.5	0.3	0.2	0.15	0.1
	Minimum sample size (accept number)							
Accept number c = 0, r ≥ 1	153(0)	231(0)	328(0)	461(0)	767(0)	1152(0)	1534(0)	2303(0)

1/ Sample sizes are based upon the Poisson exponential binomial limit.
2/ In this specification lot tolerance percent defective (LTPD) has been replaced with sample size (accept number) where the accept number is zero. Where reference is made by unrevised test methods of MIL-STD-883 to an LTPD value, that value will be found in the PDA series and the sample size will be the value immediately below the PDA series value. The accept number will always be zero.
3/ Minimum size of sample to be tested to assure, with a 90 percent confidence, that a lot having percent defective equal to the specified sample size (accept number) will not be accepted (single sample).

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APPENDIX G

RADIATION HARDNESS ASSURANCE (RHA) REQUIREMENTS FOR HYBRID MICROCIRCUITS AND MULTICHIP MODULES

G.1 SCOPE

G.1.1 Scope. This appendix provides the requirements to be used by MIL-PRF-38534 device manufacturers supplying hybrid microcircuits and multichip modules (MCM's) with radiation hardness assurance. This appendix is a mandatory part of the specification. Compliance with this appendix is required for Standard Microcircuit Drawing (SMD) product with the radiation hardness assurance designator per Table G-1. Non-SMD product (Source Control Drawing (SCD) or data sheet devices) may be identified as compliant to this appendix only if all the requirements of this appendix and the specified quality level are met.

NOTES:

1. When a customer SCD specifies compliance with any class level of MIL-PRF-38534, and specifies radiation requirements in accordance with this appendix, then the device shall be marked compliant (i.e. CKL).

2. For SCD product that is compliant to the indicated class, but not compliant to this appendix, then the product shall be marked with the QML compliance indicator (i.e. CK), but not the RHA designator.

3. Full compliance with MIL-PRF-38534 and radiation compliance to this appendix may not be required for build to print, build to specification (SCD) or joint effort between the procuring activity and the manufacturer. In this case, where devices are manufactured using MIL-PRF-38534 and this appendix as a guideline, devices shall not be marked compliant (i.e. no CK or CKL).

G.1.2 Description of Appendix G. This appendix contains the performance requirements for parts to be designated as QML-38534 RHA. The methods of assuring radiation hardness addressed in this appendix include design, hybrid device level and active element level radiation qualification, and radiation lot acceptance for active elements.

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G.1.3 Implementation of this appendix. All devices offered and shipped in compliance with this appendix shall meet the performance requirements specified in the procurement document, this appendix, and the applicable quality level (i.e., Class H, K, etc.). The manufacturer shall be in compliance to this appendix by the qualifying activity.

G.2 APPLICABLE DOCUMENTS

G.2.1 General. The documents listed in this section are specified in sections G.3 and G.4 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections G.3 and G.4 of this specification, whether or not they are listed.

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G.2.2 Government documents.

* G.2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this specification to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits (Microcircuits) Manufacturing, General Specification For
MIL-PRF-19500 - Semiconductor Devices, General Specification For.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-750 - Test Method Standard for Semiconductor Devices
MIL-STD-883 - Test Method Standard Microcircuits

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-814 - Ionizing Dose and Neutron Hardness Assurance Guidelines for Microcircuits and Semiconductor Devices.
MIL-HDBK-815 - Dose-Rate Hardness Assurance Guidelines.

(Copies of these documents are available online at https://quicksearch.dla.mil).

G.2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.
ASTM F1892 - Standard Guide for Ionizing Radiation (Total Dose) Effects Testing of Semiconductor Devices.

(Copies of these documents are available online at https://www.astm.org/).

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

JEP 133 - Guide for the Production and Acquisition of Radiation Hardness Assured Multichip Modules and Hybrid Microcircuits.
JESD57 - Test Procedures for the Measurement of Single-Event Effects in Semiconductor Devices from Heavy Ion Irradiation.
JESD89 - Measurement and Reporting of Alpha Particles and Terrestrial Cosmic Ray-Induced Soft Errors in Semiconductor Devices.

(Copies of these documents are available online at https://www.jedec.org/).

G.2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained

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APPENDIX G

G.3 REQUIREMENTS

G.3.1 General. Hybrid microcircuits supplied to this document shall be manufactured and tested in accordance with approved baseline manufacturing flow and the requirements herein. RHA qualified manufacturer listing (QML) manufacturers shall meet all the requirements of MIL-PRF-38534 and the additional requirements specified herein. If the manufacturer has a Technology Review Board (TRB), then the TRB shall not make major changes to the baseline design rules, processes, procedures, or testing without notifying the qualifying activity prior to implementation of the change.

G.3.2 Technology review board (TRB). The TRB authority to implement changes and test optimizations does not apply to RHA devices unless otherwise approved by the qualifying activity.

G.3.3 Radiation Program Plan (RPP). The RPP shall be based on the quality management plan requirement specified in paragraph A.3, and the requirements of this appendix. The RPP may refer to the manufacturer's Quality Management Plan document and address only those issues that are different or in addition for radiation hardness assurance.

G.3.3.1 Conversion of customer requirements. In addition to the conversion of customer requirements specified in Appendix A, the manufacturer shall include the process for reviewing the radiation requirements for each hybrid device and establishing the procedures used to verify that the RHA requirements are met.

G.3.3.2 Change control procedures. In addition to the change control procedures specified in Appendix A, manufacturers of RHA hybrid devices shall have in place a procedure to notify their customers of any change in design, materials, processes, active elements (i.e. microcircuits, transistors), active element manufacturers, or test and analysis methods that affect the radiation response or performance characteristics of the hybrid device. All changes affecting the RPP shall be considered a major change (See table E-1) requiring qualifying activity approval prior to implementation.

G.3.3.3 Approval of sources of radiation test data. The hybrid device manufacturer is responsible to ensure that all testing is in compliance with the specified test methods, test plans and procurement documents. The manufacturer's RPP shall identify what test methods and facilities are used and how these are approved.

a. The hybrid device manufacturer shall have laboratory suitability from the qualifying activity or use a laboratory that has qualifying activity laboratory suitability.

b. The hybrid device manufacturer may use data attained from the active element manufacturer after determining that the element manufacturer's testing methods and facilities are in compliance with the specified test procedures and procurement documents.

NOTE: Evaluation of test methods and facilities are not required for QML elements (i.e., purchased from a QML listed manufacturer to the relevant detail data sheet and general specification) for the radiation hardness conditions or documented in the Standard Microcircuit Drawing (SMD) or MIL-M-38510 specification sheet in accordance with MIL-PRF-38535, or specification sheet in accordance with MIL-PRF-19500.

c. The hybrid device manufacturer shall be responsible for evaluating and verifying that testing done by other facilities, such as procuring activity labs, is in accordance with specified test methods, test plans, and procurement documents.

G.3.3.4 Analysis of data. The hybrid device manufacturer shall have procedures in place for review and approval of radiation test data including statistical analysis. Procedures should address vendor supplied wafer lot data as well as hybrid device and active element test data gained from testing by, or for, the hybrid device manufacturer.

G.3.4 RHA marking. In addition to the marking requirements specified in paragraph 3.9.5, the RHA designator in Table G-1 shall be used in the SMD part number. For QML compliant SCDs or data sheet products, the RHA level shall follow the certification mark (i.e. CKL indicates a compliant Class K device rated at 50Krad). Non-compliant QML product shall not be marked with the RHA level.

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TABLE G-I. RHA levels.

RHA level designator	Radiation total ionizing dose level (krad(Si))
- (dash)	No RHA
M	3
D	10
P	30
L	50
R	100
F	300
G	500
H	1000

G.3.5 Procurement documents and test plan.

G.3.5.1 Hybrids devices. - Each hybrid device or family of hybrid devices shall be documented in a procurement document and manufacturer's test plan under document revision level control. The SMD is the preferred procurement document although other procurement documents may include SCDs, detail data sheets or web data sheets. Details not defined in the procurement document shall be included in the test plan.

* G.3.5.1.1 Procurement document requirements. The procurement document (e.g. SMD, SCD or data sheet) shall contain tables similar to G-II and G-III that includes applicable technologies and tests. Analysis and testing data shall be in the procurement document to notify the customer of the capability of the device. As a minimum, the procurement document shall contain a summary table containing the information provided in tables G-II and G-III, and the following applicable items.

a. If active elements are tested independently or in the hybrid device.

b. The applicable design analysis performed.

c. Hybrid packaging mechanical outline and physical characteristics.

d. Hybrid device radiation limits.

e. Hybrid device electrical test limits (pre and post radiation) hybrid level data.

f. Electrical test limits over temperature post final radiation step (if applicable).

g. Statistical probability level (e.g. 99/90 or 99/99) applied to hybrid device (if applicable).

h. Total Ionizing Dose (TID) testing, performed in accordance with Method 1019 of MIL-STD-883.

Each Item below as it applies to hybrid and element level testing.

1. Sample size, bias or unbiased, frequency of testing (i.e., each wafer lot), over-test (if applicable), and anneal (if applicable).

2. Total dose for High Dose Rate (HDR): Method 1019 of MIL-STD-883 condition A, B or C, for device TID HDR level.

3. Total dose for Low Dose Rate (LDR) (if applicable): Method 1019 of MIL-STD-883 condition C, D, E, for device TID LDR level.

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4. Evaluation of Enhanced Low Dose Rate Effects (ELDRS) (if applicable) in accordance with paragraph 3.13.1 of method 1019 of MIL-STD-883.

NOTE: If ELDRS evaluation or LDR testing is not performed, the hybrid device procurement document (see G.3.5.1) shall state that the technology may be susceptible to ELDRS and that ELDRS characterization has not been performed. This statement must be included in the procurement document to alert the procuring activity to the potential risk that the active elements or hybrid device have not been characterized or tested for ELDRS or LDR tested.

i. Neutron irradiation testing (also referred to as displacement damage) (if applicable) performed in accordance with method 1017 of MIL-STD-883. Each Item below as it applies to hybrid and element level testing.

1. Sample size, frequency of testing (i.e., each wafer lot).

2. Device hardness level to non-ionizing energy loss degradation.

Note: If neutron testing is not performed, the hybrid device procurement document (see G.3.5.1) for devices containing bipolar technology shall state that the technology is susceptible to displacement damage, and that characterization or testing has not been performed. This statement is required to alert the customer of the risk that the active elements may be susceptible to displacement damage and are not tested.

j. Single Event Phenomena testing (if applicable):

Each Item below as it applies to hybrid and element level testing.

1. Single Event Testing: Temperature, vacuum, energy (ions/nucleus) beam angle, fluence, flux, particle range, voltages, load, capacitive filters/loads, events (anticipated and tested for), cross section of events, magnitude and duration of transient voltages.

Note: Some examples of documents that may provide further guidance related to radiation hardness assurance are MIL-HDBK- 814, MIL-HDBK-815, MIL-STD-883 methods 1017, 1019, 1020, 1021, 1022, 1023 and 1032, JESD 57, JEP 133, ASTM F 1892, and ASTM F 1192.

G.3.5.1.2 Test plan criteria. The items listed must be under document revision level control by the manufacturer.

a. Burn-in circuit, burn-in time and temperature.

b. Approved test facilities for each RHA test.

c. For Active Elements (Pre and Post radiation electrical test limits, radiation limits, statistical probability of survival, package element is tested in, burn-in circuit, burn-in time and temperature).

G.3.5.2 Active elements. Each active element shall be documented in a procurement document under document revision level control. SMDs and MIL-M-38510 specification sheets for microcircuits and MIL-PRF-19500 specification sheets for semiconductors are the preferred procurement documents. Element SCDs or manufacturer detail data sheets are acceptable as procurement documents. The procurement document shall include the applicable requirements listed in paragraph G.3.5.1.1.

NOTE: This information may be included an alternate controlled document such as a test plan.

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TABLE G-II. Radiation hardness assurance methods table.

RHA Method Employed	Active elements tested only as part of the hybrid 1/	Testing at rated total dose of (X krad)		Worst Case Analysis Performed						End point electrical tests after final total dose		Statistical Analysis Probability of survival and confidence	
		Element level	Hybrid device level 1/	Hybrid device level	Includes temperature effects	Combines temperature and radiation effects	Combines total dose and displacement effects	End-of-life	Hydrogen affects	Element Level	Hybrid device level	Element Level	Hybrid device level
	Yes or No	Tested at some multiple of the rated TID. 1X as a minimum	Tested at some multiple of the rated TID. 1X as a minimum	Yes or No	Yes or No	Yes or No	Yes or No	Yes or No	Yes or No	Test temperature(s)	Test temperature(s)	State confidence level (Pxx/yy) or NA	State confidence level (Pxx/yy) or NA

1/ See paragraph G.4.3.4 alternate radiation testing procedure.

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TABLE G-III. Hybrid level and element level test table.

Radiation Test		Total Dose			Neutron		Heavy Ion	
		Low Dose Rate (LDR)	High Dose Rate (HDR)	ELDRS Characterization	SEE (upset)	Displacement Damage (DD)	SEU (upset)	SEL (latch-up)
Hybrid Level Testing		Tested or Not Tested	Tested or Not Tested	Performed or Not performed	Tested or Not tested	Tested or Not tested	Tested or Not tested	Tested or Not tested
Element Level Testing	Technology CMOS Semiconductor (Power MOSFET)	Tested or Not Tested	Tested or Not Tested	Performed or Not performed	Tested or Not tested	Tested or Not tested	Tested or Not tested	Tested or Not tested
	Technology Bipolar Semiconductor	Tested or Not Tested	Tested or Not Tested	Performed or Not performed	Tested or Not tested	Tested (or Not tested	Tested or Not tested	Tested or Not tested
	Technology Bipolar Linear or Mixed Signal	Tested or Not Tested	Tested or Not Tested	Performed or Not performed	Tested or Not tested	Tested or Not tested	Tested or Not tested	Tested or Not tested

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G.3.6 Design Analysis.

G.3.6.1 Worst case analysis (WCA). Worst case analysis shall be performed for each hybrid or family of hybrids that are determined to be similar as defined in 6.4.43 or are of the same core design to the worst case circuit design requirements of E.4.2.9 herein. Additional worst case analysis shall be performed as applicable to the procuring activity requirements. Desired post-irradiation Group A performance shall be documented based on circuit analysis, expected active element performance, or actual hybrid device performance. WCA shall be performed for total ionizing dose, neutron irradiation, and single event phenomena testing as applicable.

G.3.6.1.1 Additional RHA effects. If neutron irradiation testing is required to be performed, then the combined effect of total ionizing dose and displacement damage should be taken into account in the worst case analysis. If additional testing such as heavy ion or proton irradiation is specified in the procurement document, then these effects should also be included in the worst case analysis.

G.3.6.2 Temperature effects WCA. If temperature effects testing is required, the analysis should take into account temperature and total dose effects as a minimum.

G.3.6.3 Life cycle. As a minimum, Group A performance shall be established at beginning of life. If life cycle is required, end-of-life calculations shall be based on 15 years of continuous operation at minimum and maximum operating temperature unless otherwise specified in the procurement document.

G.3.6.4 Performance requirements. Performance requirements shall be verified by either design margin or over test.

a. Design Margin: Active element parameter requirements may be determined during the design process and verified by active element level RHA testing. Hybrid device parameter requirements may be determined during the design process and verified by hybrid level RHA testing using over test.

b. Hybrid level over-test: When testing at the hybrid level, devices with more than one active element shall be tested at 1.5X the rated total ionizing dose. See paragraph G.4.3.4

G.3.6.5 Hydrogen effects analysis. Hydrogen contributed to the internal cavity of the package has been known to increase the degradation of electrical parameters when exposed to total ionizing dose. Efforts should be made to determine the level of hydrogen in the device package when total ionizing dose testing is performed. If the electrical test results meet the limits specified in the procurement document after total dose, then the hydrogen level can be used as a baseline as a known acceptable level for this device, in the tested package. All sources of hydrogen data such as the internal gas analysis monitor in Group C3 of table C-Xc. shall be compared to the baseline. Any hydrogen level more than 1000ppm greater than the baseline may be cause for retesting or calculating a greater parametric degradation based on the increased hydrogen.

G.3.6.6 Element analysis. Any type of active element that the manufacturer determines does not need to be radiation tested (i.e. based on the active element technology) shall be identified in the design analysis. If the manufacturer determines that the active element type is radiation hardened beyond any need to do characterization or lot acceptance testing, then the justification (i.e., data or scientific explanation) for the decision must be documented and identified in the design analysis. If the manufacturer has element characterization data and has determined, by design analysis, that there is adequate design margin such that radiation lot acceptance testing is not needed, then the margin shall be identified in the design analysis.

G.3.6.7 Design analysis documentation. The design analysis performed shall be documented in the design analysis documentation in accordance with table G-II. Actual testing performed shall be documentation in accordance with table G-III.

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G.4 TESTING

G.4.1 Minimum RHA testing:

G.4.1.2 RHA testing: The minimum RHA failure mechanism/evaluations that must be addressed initially and for major changes in order to meet this appendix are addressed as follows:

G.4.1.2.1 Total Ionizing Dose. Total dose shall be performed per MIL-STD-883 test method 1019.

G.4.1.2.1.1 General test conditions. The hybrid device or elements that are to be tested shall be tested at either High Dose Rate (HDR) or Low Dose Rate (LDR), or both, initially and after major changes to establish the RHA indicator to be marked (See Table G-1). When both high dose rate testing and low dose rate testing are performed, the same parameters shall be tested at low dose rate that were tested at high dose rate.

G.4.1.2.1.2 Major change requirements. The hybrid device shall be LDR tested or evaluated for Enhanced Low Dose-Rate Effects (ELDRS), initially and after major changes unless:

a. The active element characterization has been performed and no ELDRS was observed.

b. The hybrid device procurement document (G.3.5.1) states that the technology (except for CMOS) is susceptible, and the characterization has not been performed. This statement shall be included in the procurement document to alert customers to the potential risk that the active elements may be susceptible to ELDRS irradiation, and have not been tested.

G.4.1.2.2 Neutron irradiation. Neutron irradiation displacement evaluation shall be performed initially and after major changes on either the hybrid device or the active elements (applicable to bipolar devices as a minimum) unless the hybrid device procurement document (G.3.5.1) states that the technology is susceptible, and the characterization has not been performed. This statement is required to alert the customer of the potential risk that the active elements may be susceptible to displacement damage and are not tested.

G.4.2 Hybrid device qualification testing.

G.4.2.1 General. Hybrid device-level RHA qualification testing shall be performed initially and after major changes in accordance with G.3.3.2. Hybrid device-level qualification testing shall, as a minimum, meet the RPP (G.3.3), procurement document/test plan (G.3.5.1), and Table G-IV. Minimum required testing is specified in Table G-IV. Testing a hybrid device may be omitted if data exists for a similar device as defined in 6.4.43 or it is the same core design. If this option is used, the group of devices considered “similar” shall be documented and approved by the qualifying activity. The hybrid devices in the grouping, and which part was actually tested, shall be documented in the procurement document. Radiation testing of hybrid devices shall be performed on devices that have passed burn-in (160 hrs minimum) and Group A testing requirements as a minimum. If hydrogen levels within the hybrid device are a concern, then seal testing, in accordance with method 1014 of MIL-STD-883, shall be performed prior to performing radiation testing.

G.4.2.2 Total ionizing dose. Hybrid devices shall be tested for total ionizing dose, per MIL-STD-883 Test Method 1019 (See paragraph G.4.1). The testing shall be performed on the final hybrid package so that effects from hydrogen contributed from internal materials (e.g. package materials and processing) will be included in the radiation report. If hydrogen levels were not verified during design analysis, then it is advisable to perform Internal Gas Analysis (IGA), in accordance with method 1018 or MIL-STD-1018, on a sample radiation device to establish the baseline hydrogen level with the radiation test results.

G.4.2.3 Neutron irradiation. When neutron irradiation testing is performed at the hybrid-device level (See G.4.1), the samples shall be electrically tested before and after exposure. RHA exposure shall be in accordance with MIL-STD-883 test Method 1017.

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TABLE G-IV. Hybrid device RHA qualification testing.

REQUIRED	TEST	Method	Condition	Quantity (accept number)		38534 Paragraph
Subgroup 1						
X	Burn-in	MIL-STD-883 TM 1015	160 Hrs minimum, Tc or Ta = 125°C unless otherwise specified	Required as precondition to other subgroups		G.4.2.1
X	End point electrical	Procurement Document	1/	Required as precondition to other subgroups		
Subgroup 2	2/					
G.4.1.2.2	Neutron irradiation	MIL-STD-883 TM1017	25°C	5(0)		G.4.3.4
	End point electrical	Procurement Document	1/ 3/			
Subgroup 3	2/			Qualification Method		
				Design Margin	Alternate G.3.6.4	
X	Total ionizing radiation dose	MIL-STD-883 TM1019	A, B, C, D or E	4(0)	8(0)	G.4.2.2
X	End point electrical	Procurement Document	1/ 4/ 3/	4(0)	8(0)	

See footnotes at end of table.

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TABLE G-IV. Hybrid device RHA qualification testing – Continued.

REQUIRED	TEST	Method	Condition	Quantity (accept number)	38534 Paragraph
Subgroup 4	1/ 2/ 3/				
G.4.1.2.1.2	ELDRS characterization	MIL-STD-883 TM1019	Paragraph 3.13.1.1	10(0) Condition A, C or 10(0) Condition D 1 control	G.4.2.2
	End point electrical	Procurement Document	1/ 4/ 5/	21(0)	

1/ Group A subgroups as specified in procurement document and/or test plan.
2/ Subgroup 1 precondition required.
3/ Test results are analyzed to meet a probably of survival and confidence of xx/yy (example: 99/90) as specified in the procurement (if applicable).
4/ After each dose has been completed, perform subgroups A1, A4, A7 and A9 as specified in the procurement document. After total dose has been completed, perform subgroups A1, A2, A3 and A4 or as specified in the procurement document.

Note: 99/90 is required for Alternate Verification Procedure G.4.3.4.

5/ Data analysis is required for ELDRS evaluation per paragraph 3.13.1.1 of TM 1019 MIL-STD- 883.

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G.4.3 Active element testing.

G.4.3.1 RHA active element testing. RHA active element testing (See table G-V) shall as a minimum, meet the RPP (G.3.3), active element procurement document/test plan (G.3.5.2), paragraph 4.1, and the electrical limits established in the worst case circuit analysis (G.3.6.1). Supplier active element data shall be accepted in lieu of testing as long as the testing methods and conditions, radiation levels, and electrical performance, pre and post irradiation, are verified to meet the active element procurement document/test plan (G.3.5.2). Prior to any active element radiation testing, active elements shall be subjected to test method 1015 of MIL-STD-883 or the applicable test method of MIL-STD-750 for 160 hours at 125°C. Burn-in is not required if previous testing has shown that burn-in produces negligible changes in the device radiation response or if the results of testing after radiation are corrected for the changes in radiation response which would have been caused by burn-in. If hydrogen levels are a concern, then seal testing, in accordance with method 1014 of MIL-STD-883, shall be performed prior to performing radiation testing.

G.4.3.2 Active element RHA qualification. Active Element RHA qualification testing shall be required initially and to qualify major changes that may affect RHA response.

G.4.3.2.1 Total dose testing.

G.4.3.2.1.1 Test conditions. Each active element shall be total dose tested per test method 1019 of MIL-STD-883 or MIL-STD-750 as applicable, for either High Dose Rate (HDR) or Low Dose Rate (LDR). If TID testing has not been performed at the hybrid device level, then the active element-level testing should be performed in the final hybrid package or one with a hydrogen level and volume known to be relatable to the hybrid package. When both HDR and LDR testing are performed, the same parameters shall be tested at LDR that were tested at HDR.

G.4.3.2.1.2 Major change requirements. Each active element shall be HDR tested, LDR tested, or evaluated for Enhanced Low Dose-Rate Effects (ELDRS), initially and after major changes unless the hybrid device procurement document (G.3.5.1.1) states that the technology is susceptible, and the characterization has not been performed. This statement shall be included in the procurement document to alert customers to the potential risk that the active elements may be susceptible to ELDRS and have not been tested for.

G.4.3.2.2 Neutron irradiation displacement element testing. When active elements are evaluated for neutron displacement damage (see paragraph G.4.1) the samples shall be electrically tested before and after exposure. RHA exposure shall be in accordance with MIL-STD-883 or MIL-STD-750 Method 1017.

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TABLE G-V Active element RHA qualification and radiation lot acceptance testing.

REQUIRED		TEST	Method	Condition	Quantity	38534 Paragraph
RHA Qualification G.4.3.2	Radiation lot Acceptance Testing G.4.3.3				(accept number)	
Subgroup 1						
X	X	Burn-in	MIL-STD-883 TM 1015 or MIL-STD-750 TM 1038, 1039, or 1040	160 Hrs minimum, Tc or Ta = 125°C unless otherwise specified	Required as precondition to other subgroups	
X	X	End point electrical	Design requirements		Required as precondition to other subgroups	
Subgroup 2		1/				
G.4.3.2.2	G.4.3.2.2	Neutron irradiation	MIL-STD-883 TM 1017 or MIL-STD-750 TM 1017	25°C	5(0)	G.4.3.2.2
		End point electrical	Design requirements	2/ 3/		

See footnotes at end of table.

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* Table G-V. Active element RHA qualification and radiation lot acceptance testing – Continued.

REQUIRED					Quantity	38534 Paragraph
RHA Qualification G.4.3.2	Radiation lot Acceptance Testing G.4.3.3	TEST	Method	Condition	(accept number)	
Subgroup 3		1/				
G.4.3.2.1	G.4.3.3.1	Total ionizing radiation dose	MIL-STD-883 or MIL-STD-750 TM 1019	A or C or D or E	8(0)	G.4.3.2.1 G.4.3.3.1
X	X	End point electrical	Design Requirements	2/ 3/	8(0)	
G.4.3.2.1.2	NA	ELDRS characterization	MIL-STD-883 TM 1019	Paragraph 3.13.1.1	10(0) Condition A, C or 10(0) Condition D 1 control unit	G.4.3.2.1.2
		End point electrical	Design Requirements	2/ 4/	Condition A or C and D. 10(0) HDR, 10(0) LDR and 1 control unit.	

1/ Subgroup 1 precondition required.
2/ After each dose has been completed, perform subgroups A1, A4, A7 and A9 as specified in the procurement document. After total dose has been completed, perform subgroups A1, A2, A3 and A4 or as specified in the procurement document
3/ A probably of survival and confidence (example 99/90) as specified in the procurement document shall be applied to the post-rad electrical test limits.
4/ Data analysis is required per paragraph 3.13.1.1 of TM 1019 MIL-STD 883.

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G.4.3.3 Radiation Lot Acceptance Testing (RLAT).

G.4.3.3.1 Total dose testing. Samples shall be selected from every wafer lot of active elements. Elements shall be total ionizing dose tested per test method 1019 of MIL-STD-883 or MIL-STD-750, as applicable, for either High Dose Rate (HDR) or Low Dose Rate (LDR) as determined by the active element RHA qualification paragraph G.4.3.2.1.and hybrid device RHA qualification paragraph G.4.2.2.

G.4.3.4 Alternate RHA testing procedure. Active element testing may be performed at the hybrid device level testing only if all of the following are met.

a. Samples from every wafer lot are assembled into hybrid devices that are then tested to 1.5X the rated total ionizing dose.

   Note: Hybrid devices with one active element may be tested to 1.0X the rated total ionizing dose.

b. All post 1.5X radiation data must be within the post radiation limits specified in the procurement document and demonstrate a statistical probability of survival and confidence of 99/90.

c. Production devices may only be made with combinations of wafer lots that have been tested together.

d. The hybrid device procurement document (G.3.5.1.1) clearly states that design analysis and element level testing are not performed. (See Table G-II.)

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APPENDIX G

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