

The documentation and process conversion measures necessary to comply with this document shall be completed by 2 June 2020.

METRIC

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## PERFORMANCE SPECIFICATION SHEET

PRINTED WIRING BOARD, RIGID, SINGLE AND DOUBLE LAYER,  
THERMOSETTING RESIN BASE MATERIAL, WITH OR WITHOUT  
PLATED-THROUGH HOLES, FOR SOLDERED PART MOUNTING

This specification is approved for use by all Departments  
and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist  
of this specification sheet and [MIL-PRF-31032](#).

### 1. SCOPE

1.1 Scope. This specification covers the generic performance requirements for rigid, single and double sided (1 or 2 conductor layers) printed wiring boards (hereafter designated printed board) with or without plated holes that will use soldering for component/part mounting (see [6.1.1](#)).

1.2 Classification. Printed boards are classified as rigid, type 1 (single sided), or type 2 (double sided), as specified (see [6.2](#)).

### 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections [3](#) and [4](#) of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections [3](#) and [4](#) of this specification, whether or not they are listed.

2.2 Government documents. The following specification forms a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

[MIL-PRF-31032](#) - Printed Circuit Board/Printed Wiring Board, General Specification for.

(Copies of this document are available online at <https://quicksearch.dla.mil>.)

Comments, suggestions, or questions on this document should be addressed to DLA Land and Maritime, ATTN: VAC, P.O. Box 3990, Columbus, OH 43218-3990, or emailed to [5998.Documents@dla.mil](mailto:5998.Documents@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

AMSC N/A



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2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

## ASTM INTERNATIONAL (ASTM)

- ASTM B567 - Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
- ASTM B568 - Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.

(Copies of these documents are available online at <https://www.astm.org>.)

## IPC - ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

- IPC-2221 - Generic Standard on Printed Board Design.
- IPC-2222 - Sectional Design Standard for Rigid Organic Printed Boards.
- IPC-A-600 - Acceptability of Printed Boards.
- [IPC-TM-650](#) - Test Methods Manual.
- IPC-9252 - Requirements for Electrical Testing of Unpopulated Printed Boards.

(Copies of these documents are available online at <https://www.ipc.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. Unless otherwise noted herein or in contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

## 3. REQUIREMENTS

3.1 Printed board detail requirements. Printed boards delivered under this specification shall be in accordance with the requirements as specified herein, and documented in the printed board procurement documentation.

3.1.1 Conflicting requirements. The order of precedence of conflicting requirements shall be in accordance with [MIL-PRF-31032](#).

3.1.2 Reference to printed board procurement documentation. For the purposes of this specification, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable printed board procurement documentation.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in [MIL-PRF-31032](#).

3.2 Qualification. Printed boards furnished under this specification shall be technologies that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

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### 3.3 Design and dimensional requirements.

3.3.1 Design (see 3.1 and 6.2). Printed boards shall be of the design specified. Unless otherwise noted herein, if individual design parameters are not specified in the printed board procurement documentation, then the baseline design parameters shall be as specified as follows:

- a. Overall printed board design baseline shall be in accordance with [IPC-2222](#) and [IPC-2222](#), type 1 or type 2, performance class 3.
- b. Test coupon design, quantity, placement, and usage shall be in accordance with [IPC-2221](#), performance class 3. Test coupons shall be as specified in the applicable design standard and shall reflect worst case design conditions of the printed boards that they represent. Test coupon selection and usage shall be determined by the manufacturer in order to meet the in-process, LCI, PCI and CVI inspection requirements herein.

3.3.2 Dimensional (interface and physical dimension) requirements. The completed printed board shall meet the interface and physical dimensions requirements specified. The dimensional requirements include items such as the conductor pattern including component lands and terminals, cutouts, overall board thickness, periphery, and other design features as specified. In the event that a dimensional characteristic is not specified, the applicable class 3 of [IPC-2221](#) or [IPC-2222](#) design default for that characteristic shall apply.

3.3.2.1 Conductor pattern feature accuracy. Conductor pattern feature accuracy shall be as specified.

3.3.2.2 Edge board contacts edge condition. The end or beveled edge of edge board contacts shall be smooth with no burrs, roughness, or lifted plating. There shall be no separation of the edge board contacts from the base material or any loose reinforcement fibers on the beveled edge. Exposed copper on the end or beveled edge of the edge board contact shall be acceptable. Conductor finish plating or coating shall comply with the requirements of [3.5.2.2](#).

3.3.2.3 Hole pattern accuracy. The location of the hole pattern in the printed board shall be as specified.

3.3.2.4 Hole size. The hole size and tolerance shall be as specified. Unless otherwise specified, hole size tolerance shall be applied after plating. Nodules or rough plating in plated-through holes shall not reduce the hole diameter below the minimum limits specified.

3.3.2.5 Conductor thickness (non-destructive). The conductor thickness on printed boards shall be as specified. Unless otherwise specified, the minimum final conductor thickness (metal foil) shall not be reduced by more than 10 percent from the starting metal foil nominal thickness as converted from the area weight of the foil.

3.3.2.6 Conductor width and spacing.

3.3.2.6.1 Conductor spacing. Conductor spacing, including tolerance, shall be as specified.

3.3.2.6.2 Conductor width. Conductor width shall be as specified. Unless otherwise specified, allowable reduction in the conductor width due to isolated defects or misregistration shall be in accordance with [3.5.2.3](#).

3.3.2.6.3 Edge spacing. The minimum edge spacing shall be as specified.

### 3.4 Materials.

3.4.1 Printed board materials. All materials used in the construction of compliant printed boards shall comply with the applicable specifications referenced in the printed board procurement documentation. If materials used in the production of printed boards are not specified, then it is the manufacturer's responsibility to use materials which will meet the performance requirements of this specification sheet. Acceptance or approval of any printed board material shall not be construed as a guarantee of the acceptance of the completed printed board.

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3.4.2 Prohibited materials (see 6.5). Unless otherwise specified, electroplated or immersion tin shall not be used as a finish either externally, internally, or as an undercoat. Electroplated or immersion tin is any tin or tin alloy containing more than 97 percent tin. If used as a finish, tin shall be alloyed with a minimum of three percent lead. The use of tin-lead (Sn-Pb) finishes is acceptable provided that the minimum lead content is three percent.

3.5 External visual acceptability requirements. Printed board test specimens (the finished printed boards or supporting test coupons, as applicable) shall conform to the acceptability requirements specified in 3.5.1 through 3.5.5.3 as applicable. Scratches, dents, and tool marks shall not bridge or expose signal conductors, expose base metal, expose or disrupt reinforcement fibers, reduce dielectric properties, and reduce spacing below the minimum requirements herein. The figures, illustrations, and photographs contained in [IPC-A-600](#) can aid in the visualization of externally observable accept/reject conditions of printed boards or test specimens.

3.5.1 Base material.

3.5.1.1 Edges of base material. Base material edges include the external edge of the printed board, the edges of cutouts, and the edges of non-plated-through holes. Defects such as burrs, chips, delaminations, nicks, haloing, and other penetrations along the base material edges of completed printed boards shall be acceptable provided the defect does not reduce the edge spacing specified by more than 50 percent or 2.5 mm (.098 inch), whichever is smaller. If no edge spacing requirement is specified, any base material edge defect shall not exceed 2.5 mm (.0984 inch). Loose metallic burrs shall not be acceptable.

3.5.1.2 Surface imperfections. Imperfections in the surface of the base material such as blistering, burrs, cuts, dents, exposed reinforcement material fibers, foreign materials, gouges, nicks, pits, resin scorched areas, resin starved areas, scratches, tool marks, variations in color such as white spots or black spots, or other visual defects detrimental to the performance of the base material shall be acceptable in localized concentrations providing the following conditions are met:

- a. The imperfections do not bridge between conductors.
- b. The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimum conductor spacing requirements.

3.5.1.2.1 Exposed or disrupted fibers. Exposed or disrupted reinforcement fibers on the horizontal surface of the printed board shall not bridge conductors and shall not reduce the conductor spacing below the minimum conductor spacing requirements. Unless otherwise specified, weave texture (reinforcement texture) or weave exposure (exposed reinforcement material fibers) by mechanical fabrication operations shall be acceptable provided they meet the exposed or disrupted reinforcement fiber requirements.

3.5.1.2.2 Surface pits and voids. Surface pits and voids in the base material shall be acceptable providing the following conditions are met:

- a. Surface pits or voids are no bigger than 0.8 mm (.031 inch) in the longest dimension.
- b. The surface pits or voids do not bridge conductors.
- c. The total area of all surface pits or voids does not exceed five percent of the total printed board area.
- d. The surface pit or void does not affect the performance of the base material.

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3.5.1.3 Subsurface imperfections. Subsurface imperfections (such as blistering, delamination, foreign inclusions, and haloing) shall be acceptable providing the following conditions are met:

- a. The imperfections do not bridge more than 25 percent of the distance between conductors or plated-through holes. No more than two percent of the printed board area on each side shall be affected.
- b. The imperfections do not reduce conductor or dielectric spacing below the specified minimum requirements (see 3.3).
- c. The imperfections do not propagate as a result of testing (such as rework simulation, resistance to soldering heat, or thermal shock).
- d. The longest dimension of any single imperfection is no greater than 0.80 mm (.031 inch). In non-circuitry areas, the maximum size shall not be greater than 2.00 mm (.079 inch) in the longest dimension or 0.01 percent of the printed board area, maximum.

3.5.1.4 Measling and crazing. Unless otherwise specified, measling and crazing shall comply with the class 3 acceptable conditions of [IPC-A-600](#).

### 3.5.2 Conductor pattern.

3.5.2.1 Bonding of conductor to base material and lifted lands. There shall be no peeling or lifting of any land or conductor patterns from the base material. The completed printed board shall not exhibit any lifted land. (NOTE: See 3.6.2.4 for allowances for the acceptable lifting of lands, i.e. lifted lands, following the resistance to soldering heat, rework simulation, and thermal shock testing.)

3.5.2.2 Conductor finish. The conductor finish shall be as specified. A conductor finish plating or coating material shall be used that enables the printed wiring board to meet all of the performance requirements of this specification. Unless otherwise specified (see 3.3), the following conductor finish conditions shall apply.

3.5.2.2.1 Coverage. The conductor finish shall completely cover the exposed horizontal portion of the conductor pattern. Voids in the conductor finish coverage of plated-through hole walls shall comply with the requirements herein (see 3.5.2.2.2). Complete coverage does not apply to the vertical conductor edges.

3.5.2.2.1.1 Metallic coatings or platings. The conductor finish plating or coating shall cover the basis metal of the conductive pattern. There shall be no evidence of any flaking, lifting, or separation of conductor finish coating or plating from the surface of the conductive pattern.

3.5.2.2.1.2 Tin alloys, reflowed tin-lead, or solder coated surfaces. For design requiring unfused tin-lead plating as a final conductor finish coverage, the thickness shall be as specified. The conductor finish shall cover the exposed horizontal portion of the conductor pattern. Coverage of a conductor by solder does not apply to the vertical conductor edges. The following conditions shall apply:

3.5.2.2.1.2.1 Dewetting. For tin alloys, reflowed tin-lead, or solder coated surfaces, a maximum of five percent of dewetting is permitted on any conductive surface where a solder connection will be required. Dewetting on conductors, ground, or voltage planes not used for solder connections shall meet the requirements of appendix J of [MIL-PRF-31032](#).

3.5.2.2.1.2.2 Nonwetting. For tin alloys, reflowed tin-lead, solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. Absence of solder on the vertical sides of lands shall be acceptable.

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3.5.2.2.2 Conductor finish plating and coating voids in plated-through holes. The conductor finish plating and coating shall not have voids that exceed the following limits:

- a. No more than one final finish void in any plated-through hole.
- b. Not more than five percent of the plated-through holes shall have final finish voids.
- c. Any final finish void present is not more than five percent of the plated-through holes length.
- d. Any final finish void present is less than 90 degrees of the circumference of the plated-through hole.

3.5.2.2.3 Plating junctions. Unless otherwise specified, the following requirements apply to all junctions of different plating or coating materials:

- a. There shall be no exposed copper in the junction of metallic platings or coatings.
- b. An overlap of metallic platings or coatings shall be acceptable if it is no greater than 0.8 mm (.031 inch) in length.
- c. When both solder coating and gold plating are present at a plating junction, a discolored or gray-black area at that plating overlap zone shall be acceptable.

3.5.2.2.4 Thickness (non-destructive). The plating or coating thickness of the conductor finish shall be as specified.

3.5.2.2.5 Whiskers. There shall be no whiskers of solder or other platings on the surface of the conductor pattern.

3.5.2.3 Conductor pattern imperfections. The conductor pattern shall contain no cracks, splits, or tears. Imperfections in conductor patterns shall be acceptable provided they do not exceed the defect requirements specified herein.

3.5.2.3.1 Assorted imperfections. Unless otherwise specified, any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce each conductor width by more than 20 percent of its minimum specified width. There shall be no occurrence of the 20 percent width reductions greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.3.2 Cuts and scratches. A scratch of any length or width is permissible on ground or voltage planes, provided the dielectric is not exposed. Scratches on non-critical conductors may be of any length, but no deeper than 20 percent of the total conductor thickness.

3.5.2.3.3 Dents. A dent of any length or width on ground planes shall be acceptable provided the clad surface is not torn. Dents on conductive patterns may be of any length, but no deeper than 0.013 mm (.0005 inch).

3.5.2.3.4 Pinholes. Pinholes in ground or voltage planes in non-critical areas shall be acceptable provided they have no single diameter greater than 0.5 mm (.0197 inch) and do not exceed three for each 25 mm (.984 inch) diameter. A pinhole in a conductive pattern shall be acceptable, provided it does not reduce the width of a conductive pattern by 10 percent. Pinholes shall be limited to no more than one for each 25 mm (.984 inch) of conductive length.

3.5.2.3.5 Pits. Pits in ground or voltage planes shall be acceptable provided they do not exceed 25 percent of the surface area. Any pit in the conductive pattern is acceptable provided the outline dimension does not exceed 10 percent of the conductor width, and there is no more than one pit for each 25 mm (.984 inch) of the conductor length.

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3.5.2.3.6 Superfluous metal. Unless otherwise specified, small particles of metal such as extraneous copper or subsequent plating after etching, which remain affixed to areas that are intended to be free of conductive material, shall be acceptable providing the following conditions are met:

- a. The superfluous metal is no closer than 6.4 mm (.25 inch) to any conductor.
- b. The superfluous metal is smaller than 0.13 mm (.005 inch) at its greatest diameter.

3.5.2.4 Lands for component mounting. The lands to be used for component mounting shall be as specified. Imperfections on component hole lands, surface mount lands, or wire bond pads shall be acceptable provided they do not exceed the defect allowance requirements specified herein.

3.5.2.4.1 Component hole lands. The external annular ring shall be as specified. Unless otherwise specified, the external annular ring for component hole lands may have in isolated areas a 20 percent reduction of the specified minimum external annular ring due to defects such as dents, pinholes, pits, or nicks. No more than 20 percent of the annular ring circumference (72 degrees) may be affected.

3.5.2.4.2 Rectangular surface mount lands (see figure 1). The size of the rectangular surface mount land shall be as specified. The pristine area of the land is defined as the area within the 80 percent of the land width by 80 percent of the land length as shown on figure 1. Unless otherwise specified, defects such as nicks, dents, and pin holes along the external edge of the land shall not exceed 20 percent of either the length or width of the land and shall not encroach the pristine area. Defects internal to the land shall not exceed 10 percent of the length or width of the land and shall remain outside of the pristine area of the surface mount land. One electrical test probe "witness" mark shall be acceptable within the pristine area.

3.5.2.4.3 Round surface mount lands (ball grid array [BGA] lands) (see figure 2). The size of the round surface mount land shall be as specified. Unless otherwise specified, defects such as nicks, dents, and pin holes along the edge of the land shall not radially extend towards the center of the land by more than 10 percent of the diameter of the land and shall not extend more than 20 percent around the circumference of the land as shown on figure 2. There shall be no defects within the pristine area which is defined by the central 80 percent of the land diameter. One electrical test probe "witness" mark shall be acceptable within the pristine area.

3.5.2.4.4 Wire bond lands. Unless otherwise specified, the maximum conductor finish roughness (surface roughness) for pads or areas designated for wire bonding shall be no greater than 0.8 micrometers (31 micro inches). Unless otherwise specified, the wire bond land bonding area shall be defined as the pristine area as shown on figure 1 for rectangular pads or on figure 2 for round pads. There shall be no pits, nodules, scratches, electrical test probe "witness" marks, or other defects in the pristine area that exceed the surface roughness limits.

3.5.3 Holes for layer-to-layer connections. The external annular ring of holes used for layer-to-layer connections shall be as specified. Unless otherwise specified, the external annular ring may have in isolated areas a 20 percent reduction of the specified minimum external annular ring due to defects such as dents, pinholes, pits, or nicks.

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3.5.4 Solder mask (when applicable). The cured solder mask shall not exhibit any chalking, crazing, peeling, skipping or skip coverage, softening, swelling, wicking, or wrinkles in excess of the limits specified herein. Unless otherwise specified, the solder mask conditions below shall apply.

3.5.4.1 Coverage. Solder mask coverage imperfections (such as blisters, delaminations, pits, skips, wrinkles, and voids) shall be acceptable providing the imperfection meets all of the following:

- a. The solder mask imperfection shall not expose two adjacent conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.
- b. In areas containing parallel conductors, the solder mask imperfection shall not expose two isolated conductors whose spacing is less than 0.50 mm (.020 inch) unless one of the conductors is a test point or other feature area which is purposely left uncoated for subsequent operations.
- c. The exposed conductor shall not be bare copper.
- d. The solder mask imperfection does not expose tented via holes.
- e. Blister, pits or voids in non-conductor areas shall be acceptable if they have adherent edges and do not exhibit blistering or lifting in excess of that allowed in 3.7.4.3.
- f. For designs using solder mask over bare conductors, it shall be acceptable to have up to 0.25 mm (.010 inch) of exposed base metal at the interface between the solder mask and the basis metal conductor finish.

3.5.4.2 Discoloration. Discoloration of metallic surfaces under the cured solder mask is acceptable.

3.5.4.3 Registration. The solder mask shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified. If no requirements are specified, the following apply:

- a. Unless otherwise specified, solder mask shall not encroach onto surface mount lands.
- b. Solder mask misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements.
- c. Solder mask shall not encroach into plated-through hole barrels or onto other surface features (such as connector fingers or lands of unsupported holes) to which solder connections will be made.
- d. Solder mask is permitted in plated-through holes or vias in which no lead is to be soldered.
- e. Test points which are intended for assembly testing shall be free of solder mask unless a partial coverage allowance is specified.

3.5.4.4 Thickness. Solder mask thickness shall be as specified.

3.5.4.5 Solder mask cure. The cured solder mask coating shall not exhibit tackiness, blistering, or delamination in excess of that allowed in 3.5.4.1.

3.5.4.6 Soda straw voids. There shall be no visible soda straw voids between the solder mask and the printed board base material surface and the edges of the conductor patterns.



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### 3.5.5 Via protection.

3.5.5.1 Filled via, resin, cap plating (see figure 3). When the design requires the copper cap plating of filled vias (see 3.1), all vias required to be protected by cap plating shall be completely covered by the cap plating. The plated copper surface shall be planar with no indication of the filled via underneath. Visually discernable protrusions (bumps) and depressions (dimples) in the copper plating over filled vias shall be acceptable providing they meet the requirements of 3.6.5. Voids in the copper cap plating over the filled portion of the via shall not be acceptable.

3.5.5.2 Solder mask plugging. When the design requires that through vias be plugged by solder mask, the percentage of plugging shall be as specified. Voids in the solder mask within the plugged hole shall be as specified.

3.5.5.3 Unfilled via, solder mask tenting (see figure 4). When the design requires the tenting of solder mask over unfilled vias (see 3.1), all vias required to be protected shall be completely covered by solder mask. Voids in the solder mask over the via exposing the hole shall not be acceptable.

3.6 Microsection requirements (double sided with plated holes only). When plated hole structures are examined in cross-section, the microsectioned printed board test specimens (production printed boards or test coupons) shall meet the requirements in 3.6.1 through 3.6.5.2, as applicable. If not specified on the applicable printed board procurement documentation or herein, the requirements of 3.3.1 shall be met. Barrel cracks, butt plating joints, circumferential separations, corner cracks, and cracked copper plating shall not be acceptable. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of microsectioned test specimens. If a condition is not addressed herein, or specified on the printed board procurement documentation, it shall comply with the class 3 criteria of IPC-A-600.

3.6.1 Base material. Unless otherwise specified, the following base material acceptance criteria shall apply.

3.6.1.1 Dielectric layer thickness. The minimum dielectric thickness between conductor layers shall be as specified.

3.6.1.2 Laminate voids (see figure 5). Laminate voids with the longest dimension of 0.08 mm (.003 inch) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, horizontally or vertically, as specified. For type 2 designs, after undergoing rework simulation (see 3.7.4.5), resistance to soldering heat (see 3.7.6.2), or thermal shock (see 3.7.6.3), laminate voids are not evaluated in zone A.

3.6.2 Conductor pattern.

3.6.2.1 Conductor finish. The conductor finish shall be as specified. Unless otherwise specified, the following conductor finish conditions specified shall apply.

3.6.2.1.1 Conductor finishes of tin alloys, reflowed tin-lead, or solder coating.

3.6.2.1.1.1 Dewetting. For conductor finishes using tin alloys, reflowed tin-lead, or solder coated surfaces, a maximum of five percent of dewetting is permitted on any conductive surface where a solder connection will be required. Dewetting on conductors, ground, or voltage planes not used for solder connections shall meet the requirements of appendix J of MIL-PRF-31032.

3.6.2.1.1.2 Nonwetting. For tin alloys, reflowed tin-lead, solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. Absence of solder on the vertical sides of lands shall be acceptable.

3.6.2.1.2 Thickness (plating or coating). The plating or coating thickness of the conductor finish shall be as specified.

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3.6.2.2 Conductor thickness (double sided with plating). The conductor thickness on printed boards shall be as specified. When a conductor thickness is specified, the external conductor thickness (copper foil and copper plating) shall be equal to, or greater than, the specified thickness. When a conductor thickness with tolerance is specified, the external conductor thickness shall be within the specified tolerance for the specified thickness. If only a starting metal foil weight is specified, the limits for external conductors with plating defined in the "external conductor thickness after plating" table of [IPC-2221](#) shall apply.

3.6.2.3 Conductor width. The conductor width shall be as specified. Unless otherwise specified, allowable reduction in the conductor width due to isolated defects shall be in accordance with [3.5.2.3](#).

3.6.2.4 Lifted lands (after rework simulation, resistance to soldering heat or thermal shock) (see [figure 5](#)). After undergoing rework simulation (see [3.7.4.5](#)), resistance to soldering heat (see [3.7.6.2](#)), or thermal shock (see [3.7.6.3](#)), the maximum allowed lifted land distance from the printed board surface plane to the outer lower edge of the land shall be the thickness (height) of the terminal area or land. The completed, non-stressed printed board shall not exhibit any lifted lands.

3.6.3 Treatments to sensitize the hole prior to copper plating (when applicable). Conductive coatings applied to the hole wall shall be sufficient for subsequent hole wall copper plating processes. Conductive coatings may be either electroless copper, direct metallization copper, nonmetallic conductive coatings, or vacuum deposited copper, as applicable.

3.6.4 Plated-through hole plating. Unless otherwise specified, copper plating thickness applies to the hole wall, the hole knee, and the surface land of the plated-through hole.

3.6.4.1 Copper plating defects. Nodules, plating folds, plating inclusions, or plated reinforcement material protrusions that project into the plated-through hole shall be acceptable provided that the hole diameter and the copper thickness are not reduced below their specified limits.

3.6.4.2 Copper plating thickness. Unless otherwise specified, the copper plating thickness shall be in accordance with the applicable design standard. Any copper plating thickness less than 80 percent of the specified thickness shall be treated as a void.

3.6.4.2.1 Copper plating voids. The copper plating in the plated-through hole shall not exhibit any void in excess of the following:

- a. There shall be no more than one plating void for each panel, regardless of length or size.
- b. There shall be no plating void longer than five percent of the total printed board thickness.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated-through hole exhibiting this condition shall be counted as having one void for panel acceptance purposes.

3.6.4.2.2 Wrap copper plating. Unless otherwise specified, the wrap plating (plated-through hole surface and knee continuous copper plating) thickness shall be as specified. Reduction of surface copper wrap plating by processing (sanding, etching, planarization, etc.) resulting in insufficient wrap plating shall not be acceptable. Via cap plating shall not be included in the wrap copper measurement.

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3.6.4.3 Conductive interface separations. Except for along the vertical edge of the external copper foil, there shall be no separations or contamination between the hole wall conductive interfaces. Conductive interface separations along the vertical edge of the external copper foil shall be acceptable. Anomalies resulting from this separation shall not be cause for rejection.

NOTE: The term conductive interfaces shall be used to describe the junction between the hole wall plating or coating and the surfaces of internal and external layers of copper or metal foil. The interface between platings and coating (electroless copper, direct metallization copper, non-metallic conductive coatings, or vacuum deposited copper, as applicable, and electrolytic copper, whether panel or pattern plated), shall also be considered a conductive interface.

3.6.4.4 Metallic cracks. There shall be no cracks in the platings or coatings. For terminal or land areas plated with copper, cracks are permissible in the external layer (outer) copper foil provided they do not extend or propagate into the plated copper.

3.6.4.5 Wicking. Wicking of copper plating extending 0.08 mm (.003 inch) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified.

### 3.6.5 Via cap plating.

3.6.5.1 Thickness. For designs that specify copper plating for via protection, the minimum via cap plating thickness over filled vias shall be as specified. If not specified, the minimum via cap copper plating thickness over filled vias shall be in accordance with the minimum wrap copper plating thickness specified.

3.6.5.2 Cap plating imperfections. When cap plating of a filled via is specified (see 3.1), voids in the plating over the via fill shall not be acceptable. Separation of the via cap plating to non-conductive via fill material shall be acceptable. Separation of the via cap plating to underlying plating shall not be acceptable. Depressions (dimples) below the surface of the land shall be no greater than 0.08 mm (.003 inch). Protrusions (bumps) of the cap plating above the surface of the land shall be no greater than 0.05 mm (.002 inch).

3.7 Performance requirements. The performance requirements specified in 3.7.1 through 3.7.6.3 shall be verified by the test methods detailed in 4.7. Unless otherwise specified by the Technical Review Board (TRB), test optimization in accordance with MIL-PRF-31032 may be used, but the printed boards shall meet all of the performance requirements specified and herein, regardless of the verification method used.

### 3.7.1 External visual and dimensional inspection (of printed boards).

3.7.1.1 External visual inspection. When examined as specified in 4.7.1, the printed boards shall be in accordance with the acceptance requirements specified in 3.5 (external visual acceptability, 3.8 (marking), and 3.9 (workmanship).

3.7.1.2 Design and dimensional inspection. When examined as specified in 4.7.1, the printed boards shall conform to the acceptance requirements specified in 3.3 (design and dimensional requirements) and 3.4 (material), inclusive.

3.7.2 Destructive physical analysis (DPA) by microsectioning and evaluation of printed board test specimens. When printed board test specimens (completed printed boards, supporting test coupons, or qualification test specimens) are cross-sectioned and examined as specified in 4.7.2, the requirements specified in 3.1, 3.3, and 3.6 shall be met. Microsections of non-stressed printed board test specimens shall be evaluated when the microsection examination of the stressed printed board test specimens suggest that a failure condition may exist in the completed boards (prior to being subjected to resistance to soldering heat testing).

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### 3.7.3 Chemical requirements.

3.7.3.1 Ionic contamination (cleanliness). When printed board test specimens are tested in accordance with [4.7.3.1](#), the levels of ionic contamination shall be in accordance with the requirements of 3.7.3.1.1 or 3.7.3.1.2, as applicable.

3.7.3.1.1 Prior to the application of solder mask. Unless otherwise specified, prior to the application of solder mask, the level of ionic contamination shall not exceed 1.56 micrograms/square centimeter (10.06 micrograms/square inch).

3.7.3.1.2 Completed printed boards (when specified, see [3.1](#) and [6.2.1.a](#)). The levels of cleanliness for completed printed boards shall be as specified.

### 3.7.3.2 Copper plating characteristics.

3.7.3.2.1 Elongation. When copper plating is tested in accordance with [4.7.3.2](#), the elongation shall be 12 percent minimum.

3.7.3.2.2 Tensile strength. When copper plating is tested in accordance with [4.7.3.3](#), the tensile strength shall be 248 MPa (36,000 psi) minimum.

3.7.3.2.3 Purity of copper. When copper plating is tested in accordance with [4.7.3.4](#), the purity of the copper shall be as specified. When no value for copper purity is specified, it shall not be less than 99.5 percent.

### 3.7.4 Physical requirements.

3.7.4.1 Adhesion, marking. After marking is tested in accordance with [4.7.4.1](#), any specified markings which are missing in whole or in part, faded, shifted (dislodged), or smeared to the extent that it cannot be readily identified or is not legible shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

3.7.4.2 Adhesion, plating. When tested as specified in [4.7.4.2](#), there shall be no part of the conductor pattern or copper plating protective finish (coating or plating) removed from the printed board test specimen except for those related to outgrowth, overhang, or slivers.

3.7.4.3 Adhesion, solder mask (when applicable). When tested as specified in [4.7.4.3](#), the maximum percentage of cured solder mask lifted from the surface of the base material, conductors, and lands of the coated printed board test specimen shall not exceed the following limits:

- a. Bare copper or base material: Zero percent.
- b. Non-melting metals (e.g., gold or nickel plating): Five percent.
- c. Melting metals (e.g., tin-lead plating, solder coating, indium, bismuth, and others): Ten percent.

3.7.4.4 Bow and twist. When printed boards are tested as specified in [4.7.4.4](#), the maximum limit for bow and twist shall be as specified.

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### 3.7.4.5 Rework simulation.

3.7.4.5.1 Unsupported holes. After undergoing the test specified in 4.7.4.5.1, the printed board test specimens with unsupported holes shall withstand 2.27 Kg (5 pounds) pull or 3.45 MPa (500 pounds per square inch), whichever is less.

3.7.4.5.2 Plated holes. After undergoing the test specified in 4.7.4.5.2, the printed board test specimens shall be microsectioned and inspected in accordance with 4.7.2 and the requirements specified in 3.6 shall be met.

3.7.4.6 Solderability (see 6.2.1.b). Printed board designs that do not require soldering to attach components (as in the case where press-fit components or wire bonding are used) do not require solderability testing. Printed boards that require soldering during assembly processes require solderability testing. Printed boards using only surface mount component do not require hole solderability testing. When required by the procurement documentation, accelerated conditioning for coating durability shall be in accordance with appendix J of MIL-PRF-31032.

3.7.4.6.1 Hole solderability. After undergoing the test specified in 4.7.4.6, the printed board test specimen shall conform to the requirements of appendix J of MIL-PRF-31032.

3.7.4.6.2 Surface solderability. After undergoing the test specified in 4.7.4.6, the printed board test specimen shall conform to the requirements of appendix J of MIL-PRF-31032.

3.7.5 Electrical requirements. If specified (see 3.1), the use of indirect testing by signature comparison for continuity and isolation may be used for production screening.

3.7.5.1 Continuity (when specified, see 6.2.1.d). When tested in accordance with 4.7.5.1, the resistance between the endpoints of conductor patterns within a network of conductors shall be as specified. If no resistance limit is specified, there shall be no circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum for each 25.0 mm (.98 inch) of circuit length shall apply. Conductor patterns that consist of long runs of narrow conductors or short runs of very wide conductors may increase or decrease the resistance. The acceptability of these type of circuit patterns, of controlled impedance nets, or of embedded resistive patterns shall be as specified.

3.7.5.2 Isolation (when specified, see 6.2.1.d). When tested as specified in 4.7.5.2, the insulation resistance between mutually isolated conductors shall be specified. Unless otherwise specified, for production printed boards, the insulation resistance shall be greater than 2 megohms.

### 3.7.6 Environmental requirements.

3.7.6.1 Moisture and insulation resistance. When tested as specified in 4.7.6.1, the printed board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed board test specimen shall not exhibit blistering, measling, or delamination in excess of that allowed in 3.5.1.

### 3.7.6.2 Resistance to soldering heat.

#### 3.7.6.2.1 Solder float thermal stress.

3.7.6.2.1.1 Unsupported holes. After undergoing the test specified in 4.7.6.2.1, the printed board test specimen shall be inspected in accordance with 4.7.1 and not exhibit any cracking or separation of plating or conductors, terminals or lands shall not lift in excess of that allowed in 3.6.2.4, and blistering or delamination shall not exceed the limits in 3.5.

3.7.6.2.1.2 Plated holes. After undergoing the test specified in 4.7.6.2.1, the printed board test specimen shall be inspected in accordance with 4.7.1 and blistering or delamination shall not exceed the limits in 3.5. The printed board test specimen shall then be microsectioned and inspected in accordance with 4.7.2 and shall meet the requirements of 3.1, 3.3, and 3.6.

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3.7.6.2.2 Solder reflow thermal stress. After undergoing the test specified in 4.7.6.2.2, the printed board test specimen shall be inspected in accordance with 4.7.2 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.6.3 Thermal shock. After undergoing the test specified in 4.7.6.3, the printed board test specimens shall meet the following requirements:

- a. Visual inspection: When inspected as specified in 4.7.1, there shall be no evidence of plating cracks, blistering, crazing, or delamination in excess of that allowed in 3.5.
- b. Resistance change: The change in resistance between the first high temperature cycle and the last high temperature cycle shall not be more than 10 percent.
- c. DPA by microsection (double side with plated hole only): The printed board test specimen shall be vertically cross sectioned and inspected in accordance with 4.7.2 and the requirements specified in 3.1, 3.3, and 3.6 shall be met.

3.7.6.4 Temperature cycling.

3.7.6.4.1 Direct current induced. After undergoing the test specified in 4.7.6.4.1, the printed board test specimens shall meet the requirements of 3.5. For capability verification inspection testing, the following conditions shall apply:

- a. Number of samples: Six.
- b. Test temperature: 150 degrees Celsius.
- c. Resistance change: Ten percent.
- d. Maximum number of cycles: 250 for each 24 hour period.
- e. Data collection frequency: Ten cycles.
- f. Cooling ratio: 0.66.
- g. Table selection: System.

3.8 Marking.

3.8.1 Product identification and traceability. Product identification and traceability marking shall be in accordance with MIL-PRF-31032.

3.8.2 Marking legibility. After any, or all tests, marking that is either etched, screened, or ink stamped shall comply with the class 3, acceptable conditions detailed in IPC-A-600.

3.9 Workmanship. Printed boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability, or appearance.

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## 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Conformance inspection (see 4.3 and [tables I and II](#)).
- c. Capability verification inspection (see 4.6).

4.1.1 Sampling and inspection. Sampling and inspection shall be in accordance with [MIL-PRF-31032](#), and as specified herein.

4.1.2 Standard test and inspection conditions. Unless otherwise specified by the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

4.2 Qualification inspection. Unless otherwise specified by the TRB approved qualification test plan, qualification inspection shall be in accordance with [MIL-PRF-31032](#) and as specified herein.

4.2.1 Qualification test vehicles. The qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with the TRB approved qualification test plan and the applicable qualification test vehicle specification(s).

4.2.1.1 Sample. The number of qualification test vehicle(s) to be subjected to qualification inspection shall be in accordance with TRB approved qualification test plan.

4.2.2 Test routine. The qualification test vehicle(s) shall be subjected to the inspections and tests specified in [tables I and II](#) in addition to thermal shock in accordance with [3.7.6.3](#) and [4.7.6.3](#).

4.2.3 Qualification by similarity. A production lot may be considered qualified by similarity if the dimensional parameters are within twenty-five percent of those currently qualified and the processing steps used are a set or subset of those processes used for a previous qualified technology. When producing printed board designs that are within the 25 percent dimensional parameter region of a qualified process but exceed the currently qualified process limits, the TRB shall review and approve the new process limits.

4.3 Conformance inspection. Conformance inspection shall be in accordance with [MIL-PRF-31032](#) and shall consist of lot conformance inspection (see 4.4) and periodic conformance inspection (see 4.5).

4.4 Lot conformance inspection. Lot conformance inspection shall be in accordance with [MIL-PRF-31032](#) and [table I](#) herein. Panels, pallets, and printed boards to be delivered in accordance with this specification shall have been subjected to and passed all applicable inspections and tests of [table I](#) prior to delivery of product. Lot conformance inspection testing by subgroup or within a subgroup may be performed in any sequence.

4.4.1 Panel acceptance (subgroup 1 of [table I](#)) inspections. The panel acceptance inspections shall be in accordance with [MIL-PRF-31032](#), and as specified in [table I](#), subgroup 1.

4.4.2 100 percent (subgroup 2 of [table I](#)) inspections. The subgroup 2 inspections shall be in accordance with [MIL-PRF-31032](#), and as specified in [table I](#), subgroup 2. The PDA limits for [table I](#), subgroup 2 inspections shall be 50 percent.

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4.4.3 Sample inspections. Panels and printed boards to be delivered in accordance with this specification shall have been subjected to and passed all the inspections of [table I](#), subgroups 1, 2, 3, 4, and 5.

4.4.3.1 Sampling. Samples shall be randomly selected from each inspection lot. The lot conformance inspection sample plan uses a two-character designator that identifies the inspection specimen (first letter) and the C=0 sample size series (second letter) in accordance with appendix E of [MIL-PRF-31032](#). The letter "B" is used as the first letter when pallets or production printed boards are to be sampled in their deliverable form. The letter "T" is used as the first letter when test vehicles (test coupons or partial or whole production panels) are to be sampled based on the number of panels in the lot. The second letter of the two-character designator uses the letters "H", "J", and "N" to identify the C=0 sample size series. The C=0 sample size series identifies the number to sample based on the lot size.

4.4.3.1.1 Panels and pallets. When a verification is performed when the printed boards are still on either a partial or whole production panel, the number to be sampled shall be the number of production panels in the lot, not the number of printed boards on the production panel. When the deliverable item is a pallet (or array) of printed boards, the number to be used for sampling is the number of pallets in the lot, not the number of printed boards on the pallet.

4.4.3.1.2 Test coupons. When using the "S" test coupon, the number of samples to be tested shall be based on a statistical sample of the inspection panels in the lot using plan TJ. When using the "A" test coupon, the number of samples to be tested shall be based on the same statistical sample as the "S" test coupon, but a multiple of 4 shall be applied to the resulting sample size. The "A" test coupons shall be selected in groups of 4, taken from the same inspection panel.

4.4.3.2 Alternative subgroup 2 sample inspection (first piece produced design inspection). In lieu of performing sample inspections of all characteristics or parameters detailed on the applicable printed board procurement documentation during subgroup 2, the manufacturers may use first piece produced design inspection for product acceptance. This type of inspection is only applicable to the criteria described in 4.4.1.2.1 and 4.4.1.2.2. The first piece produced design inspection can be performed on the first printed wiring board that is representative of all printed wiring boards in the production lot of the design. The use of automated inspection technology shall be acceptable.

4.4.3.2.1 Board features and conductor pattern. Unless otherwise specified, the accuracy of the printed board features and conductor pattern may be verified by performing first piece produced design inspection on a representative first production run piece or by sampling the printed boards in the lot.

4.4.3.2.2 Hole pattern accuracy. Unless otherwise specified, only the holes that are specifically dimensioned on the applicable printed board procurement documentation shall be inspected for hole pattern accuracy to meet the board dimensional requirements specified. The accuracy of the hole pattern may be verified by performing first piece produced design inspection on a representative first production run piece. Unless otherwise specified, the hole pattern accuracy of nonspecifically dimensioned holes, such as plated through holes and vias, do not need to be checked as their locations are controlled by external annular ring requirements.

4.4.3.3 Percent defective allowable (PDA) limits. When 100 percent of a production lot is inspected, either in lieu of sampling or due to rejection of a sample inspection lot, the PDA limits for this 100 percent inspection shall be 50 percent.



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TABLE I. Lot conformance inspection.

Inspection	Requirement paragraph	Method paragraph	Specimen to test <u>1/</u>				Sample plan <u>2/</u>
			B/P	THM	SMT	MIX	
Subgroup 1 (panel acceptance) Solder float thermal stress	<a href="#">3.7.6.2</a>	<a href="#">4.7.6.2</a>		A and B	A and B	A and B	Plan TJ
Subgroup 2 (100 percent) External visual inspection	<a href="#">3.7.1.1</a>	<a href="#">4.7.1.1</a>	X				100 percent
Subgroup 3a (Sample) Design and dimensional inspection	<a href="#">3.7.1.2</a>	<a href="#">4.7.1.2</a>	X				Plan BH or TJ <u>3/ 4/</u>
Subgroup 3b (Sample) Chemical: Ionic contamination	<a href="#">3.7.3.1.1</a>	<a href="#">4.7.3.1</a>	X				Plan BN or TN <u>5/ 6/</u>
Subgroup 4 Physical: Adhesion, marking	<a href="#">3.7.4.1</a>	<a href="#">4.7.4.1</a>	<u>7/</u>	<u>7/</u>	<u>7/</u>	<u>7/</u>	Plan BH or TJ <u>6/</u>
Adhesion, plating	<a href="#">3.7.4.2</a>	<a href="#">4.7.4.2</a>	X	C	C	C	Plan BH or TJ <u>6/ 8/</u>
Adhesion, solder mask	<a href="#">3.7.4.3</a>	<a href="#">4.7.4.3</a>	X	G	G <u>9/</u>	G <u>9/</u>	Plan BH or TJ <u>6/</u>
Bow and twist	<a href="#">3.7.4.4</a>	<a href="#">4.7.4.4</a>	X				Plan BH
Solderability Hole	<a href="#">3.7.4.6.1</a>	<a href="#">4.7.4.6</a>		S or A		S or A	<u>10/</u>
Surface	<a href="#">3.7.4.6.2</a>	<a href="#">4.7.4.6</a>			C or M	C or M	Plan TJ
Subgroup 5 Electrical: Continuity	<a href="#">3.7.5.1</a>	<a href="#">4.7.5.1</a>	X				Plan BH <u>11/</u>
Isolation resistance	<a href="#">3.7.5.2</a>	<a href="#">4.7.5.2</a>	X				Plan BH <u>11/</u>

1/ Test coupons are in accordance with IPC-2221. B/P is either a production printed board separated from the panel, a pallet of boards, or a partial or whole production panel of printed boards; THM is a through-hole mount test coupon; SMT is a surface mount test coupon; MIX is for printed board designs containing both through-hole and surface mount components test coupon.

2/ See MIL-PRF-31032 for C = 0 sampling plans. See 4.4.3.1 for explanation of codes.

3/ Surface imperfections (3.5.1.2) and subsurface imperfections (3.5.1.3) shall be inspected prior to solder mask application.

4/ See 4.4.3.1.1 for test specimen selection options.

5/ Inspection shall be performed prior to solder mask application. Additional inspections on completed printed boards may be specified.

6/ Test coupon, partial or whole production panel, pallet, or production printed board, manufacturer option.

7/ See 4.7.4.1 for test specimen description and quantity.

8/ Applicable to platings only. This inspection does not need to be performed on solder or organic coatings.

9/ Test coupon "T" shall be used when production printed boards have tented via holes (type 2 only).

10/ For designs containing plated holes (see 4.4.3.1.2).

11/ Type 2 only.

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4.5 Periodic conformance inspection. Periodic conformance inspection shall be in accordance with TRB approved periodic conformance inspection plan or table II herein.

TABLE II. Periodic conformance inspection baseline test coverage.

Inspection	Requirement paragraph	Method paragraph	Frequency
Elongation <u>1/</u>	<a href="#">3.7.3.2.1</a>	<a href="#">4.7.3.2</a>	Monthly
Tensile strength <u>1/</u>	<a href="#">3.7.3.2.2</a>	<a href="#">4.7.3.3</a>	Monthly
Purity of copper	<a href="#">3.7.3.2.3</a>	<a href="#">4.7.3.4</a>	Monthly
Rework simulation <u>2/</u>	<a href="#">3.7.4.5</a>	<a href="#">4.7.4.5</a>	Monthly
Moisture and insulation resistance <u>2/</u>	<a href="#">3.7.6.1</a>	<a href="#">4.7.6.1</a>	Monthly

1/ A minimum of ten test specimens (five lengthwise and five crosswise) shall be inspected.

2/ A minimum of two test specimens for each inspection.

4.6 Capability verification inspection. Capability verification inspection shall be in accordance with the TRB approved capability verification inspection plan. The frequency of this verification shall be as a minimum every 2 years. Each base material type qualified shall be verified. The following tests and inspections should be considered when accomplishing capability verification inspection: Thermal shock (see [3.7.6.3](#)), convection air oven solder reflow thermal stress (see [3.7.6.2.2](#)) and direct current induced thermal cycling (see [3.7.6.4](#)).

#### 4.7 Methods of inspection.

##### 4.7.1 Visual and dimensional inspection.

4.7.1.1 External visual inspection. The external visual features of the printed board specimen shall be inspected in accordance with test method number [2.1.8 of IPC-TM-650](#), except that the magnification shall be 1.75x (3 diopters), minimum. If confirmation of a suspect defect cannot be determined at 1.75X, it shall be verified at progressively higher magnifications, up to 30X.

4.7.1.2 Design and dimensional inspection. The design and dimensional features of the printed board test specimen shall be inspected using test method numbers [2.2.1 and 2.2.2 of IPC-TM-650](#), as applicable. Referee inspection needed to confirm a suspected defect or deviation of the printed board test specimen features shall be accomplished at a magnification of up to 30X, as applicable to confirm the suspected defect or deviation.

4.7.1.3 Alternate plating and coating measurement techniques. When a conductor surface finish plating or coating thickness is less than 0.00125 mm (.00005 inch), the thickness measurements shall be performed in accordance with one of the following procedures:

- a. [ASTM B567](#), measurement of thickness by the beta backscatter method.
- b. [ASTM B568](#), measurement of thickness by X-ray spectrometry.

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4.7.2 DPA by microsection evaluation. Microsection examination (to evaluate characteristics of plated-hole structures, plating thickness, foil thickness, etc.) shall be accomplished by using the following preparation and inspection methods.

4.7.2.1 Microsection preparation. Microsection preparation shall be accomplished by using methods in accordance with either method A or B of test method number 2.1.1 of IPC-TM-650. Automatic microsectioning techniques may be used in lieu of IPC-TM-650 methods. The following details shall apply:

- a. Number of holes for each test specimen. A minimum of at least three plated holes shall be cross sectioned vertically for each test specimen required.
- b. Grinding and polishing accuracy. The grinding and polishing accuracy for mounts shall be in accordance with the minimum qualities specified in test method 2.1.1 of IPC-TM-650.
- c. Pre-microetch evaluations. The plated holes shall be evaluated for plating separations prior to microetching.
- d. When more than two test specimens are contained in a mount (coupon-stacking or gang mounting), the following shall apply:
  - (1) The test specimens shall not be in direct contact with any other specimen in the mount. The recommended minimum distance between test specimens in a mount is 0.25 mm (.010 inch).
  - (2) The traceability requirements of MIL-PRF-31032 shall apply.

4.7.2.2 Microsection examination and inspection. Microsection examination and inspection shall be accomplished in accordance with test method number 2.2.5 of IPC-TM-650 to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, and so forth, in plated holes. If more than three plated holes are in a row on a test specimen, as with the A/B coupon design, all holes in the row shall be evaluated. Each side of the plated holes shall be viewed independently. The following details shall apply:

- a. Magnifications. The test specimens shall be inspected at the magnification specified in test method number 2.2.5 of IPC-TM-650. Referee inspections shall be accomplished at a magnification of 200X to 400X  $\pm$ 5 percent.
- b. Pre and post microetch evaluations. The plated holes shall be evaluated for plating separations both prior to and after microetching. Pre- and post-microetching evaluations shall be accomplished at magnifications specified above.
- c. Measurements. Thickness measurements shall be averaged from at least three determinations for each side of the plated hole. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in 3.6.3.2.1.

EXAMPLE: The copper plating thickness of the plated-through hole wall shall be determined from the average of three measurements, approximately equally spaced, taken on each side of the hole.

- d. Plating or coatings that are less than 0.00125 mm (.00005 inch) in thickness shall not be measured using metallographic techniques. See 4.7.1.3 for alternate measurement techniques. Platings and coatings less than the metallographic limit shall be evaluated using the alternate measurement techniques of 4.7.1.3.

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4.7.3 Chemical test methods.

4.7.3.1 Ionic contamination. The test for ionic contamination shall be performed in accordance with test method number [2.3.25 of IPC-TM-650](#).

4.7.3.2 Elongation of copper. The test for elongation of copper shall be performed in accordance with test method number [2.4.18.1 of IPC-TM-650](#). The travel speed of testing shall be 50.0 mm  $\pm$  1.0 mm (1.97  $\pm$  .03 inches) for each minute of test.

4.7.3.3 Tensile strength of copper. The test for tensile strength of copper shall be performed in accordance with test method number [2.4.18.1 of IPC-TM-650](#) with the following exceptions:

- a. The travel speed of testing shall be 50.0 mm  $\pm$  1.0 mm (1.97  $\pm$  .03 inches) for each minute.
- b. The mean average cross-sectional area shall be calculated using the following steps:
  - (1) Measure the thickness of specimens by use of an optimizer (an electrical-type measuring device) or vernier micrometer, provided that the thickness is measured to at least the nearest 2 percent.
  - (2) Measure and record the specimen width dimension to the nearest 0.025 mm (.001 inch).
  - (3) The mean average cross-sectional area is the result of the average thickness multiplied by the average width.

4.7.3.4 Purity of copper. The test for purity of plated copper shall be performed in accordance with test method number [2.3.15 of IPC-TM-650](#).

4.7.4 Physical test methods.

4.7.4.1 Adhesion, marking. Test specimens which represent all types of marking used on the lot (except etched marking) shall be subjected to the solderability test in [4.7.4.6](#). The side of the test specimen that is marked shall be placed against the solder. After the test, the test specimen shall be examined in accordance with [4.7.1](#) and the requirements of [3.7.4.1](#) shall be met.

4.7.4.2 Adhesion, plating. The test for plating adhesion shall be performed in accordance with test method number [2.4.1 of IPC-TM-650](#). If overhanging metal break off and adheres to the tape, it is evidence of outgrowth, overhang or slivers, but not of plating adhesion failure.

4.7.4.3 Adhesion, solder mask. The test for solder mask adhesion shall be performed in accordance with test method number [2.4.28.1 of IPC-TM-650](#).

4.7.4.4 Bow and twist. The tests for bow and twist shall be performed in accordance with test method number [2.4.22 of IPC-TM-650](#).

4.7.4.5 Rework simulation.

4.7.4.5.1 Single and double sided without plated holes. The rework simulation test shall be performed in accordance with test method number [2.4.21 of IPC-TM-650](#).

4.7.4.5.2 Double sided with plated holes. The rework simulation test shall be performed in accordance with test method number [2.4.36 of IPC-TM-650](#).

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4.7.4.6 Solderability. The tests for hole or surface solderability shall be performed in accordance with appendix J of [MIL-PRF-31032](#).

4.7.5 Electrical test methods.

4.7.5.1 Continuity and isolation, production screening. Printed boards shall be electrical tested using either automatic or manual equipment capable of verifying the level C requirements of [IPC-9252](#) for 100 percent continuity and isolation.

4.7.5.2 Continuity and isolation, qualification and periodic testing.

4.7.5.2.1 Continuity. A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed those specified in the applicable design standard for the smallest conductor in the circuit.

4.7.5.2.2 Isolation (circuit shorts). A test voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The test voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer (when applicable). For manual testing, the test voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be the maximum rated voltage specified. If the maximum rated voltage on the printed board is not specified, the test voltage shall be 40 volts minimum.

4.7.6 Environmental test methods.

4.7.6.1 Moisture and insulation resistance. The test for moisture and insulation resistance shall be performed in accordance with class 3 test conditions of test method number [2.6.3 of IPC-TM-650](#) using specimen preparation method A. The initial and final insulation resistance shall be greater than, or equal to, 500M ohm when measured at 500 volts (+10, -0 percent) dc.

4.7.6.2 Resistance to soldering heat.

4.7.6.2.1 Solder float thermal stress. The test for solder float thermal stress shall be performed in accordance with test condition A of appendix F of [MIL-PRF-31032](#).

4.7.6.2.2 Solder reflow thermal stress. The test for solder reflow thermal stress shall be performed in accordance with test condition D of appendix F of [MIL-PRF-31032](#).

4.7.6.3 Thermal shock. The test for thermal shock shall be performed in accordance with test method number [2.6.7.2 of IPC-TM-650](#) except that the temperature extremes shall be -65 degrees Celsius and +125 degrees Celsius for all base materials and minimum dwell time at each temperature extreme shall be 15 minutes.

4.7.6.4 Temperature cycling.

4.7.6.4.1 DC current induced. The test for DC current induced thermal cycling shall be performed in accordance with test method number [2.6.26 of IPC-TM-650](#).

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## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-PRF-31032 are applicable to this specification.

6.1.1 Intended use. This specification sheet was developed for the use of verifying the performance of rigid, woven glass reinforced, thermosetting resin base materials, single and double sided printed wiring boards, with or without plated holes, that will use soldering for component mounting. Printed wiring boards of other base material types or construction styles can be tested or verified to the performance requirements contained in this document, however, the performance parameters of other performance specifications sheets may be more appropriate.

6.2 Acquisition requirements.

6.2.1 Primary acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, revision letter, and date of this specification.
- b. The specific issue of individual documents referenced (see section 2).
- c. Title, number, and date of applicable printed board procurement documentation or drawing. Identification of the originating design activity and, if applicable, the Government approved deviation list for the printed board procurement documentation or drawing.
- d. The complete product procurement documentation part or identifying number (see 3.1).
- e. The printed wiring board classification (type 1 or 2, see 1.2 and 3.3).
- f. Title, number, revision letter (with amendment number when applicable), and date of the applicable design standard with performance classification.
- g. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the product inspection lot to be supplied with each shipment by the QML manufacturer, if applicable.
- h. Requirements for certificate of compliance, if applicable.
- i. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- j. Packaging required (see 5.1).
- k. If special or additional identification marking is required (see 3.8).
- l. Requirements for the solderability test method to be used (see appendix J of MIL-PRF-31032).

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6.2.2 Optional acquisition data. The following items are optional and are only applicable when specified in the printed board procurement documentation.

- a. Requirements for any special or additional cleanliness (see 3.7.3.1.2).
- b. Requirements for any accelerated aging for solderability testing (see appendix J of MIL-PRF-31032).
- c. Requirements for failure analysis, corrective action and reporting of results.
- d. Requirements for electrical testing (see 3.7.5).
- e. Requirements for the disposition of lot conformance inspection sample units.
- f. Requirements for quality data and records to be delivered with the order.
- g. Requirements for special or additional identification marking is required (see 3.8).
- h. Any other special requirements.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-31032) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [5998.Qualifications@dla.mil](mailto:5998.Qualifications@dla.mil) or at URL [https://landandmaritimeapps.dla.mil/Offices/Sourcing\\_and\\_Qualification/offices.aspx](https://landandmaritimeapps.dla.mil/Offices/Sourcing_and_Qualification/offices.aspx). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <https://qpldocs.dla.mil>.

6.4 Replacement information. This specification includes a majority of the performance requirements of previous revisions of MIL-P-55110 and MIL-PRF-55110 for types 1 and 2 printed wiring boards constructed using woven glass reinforced epoxy or polyimide resin base material (legacy types GB, GE, GF, GH, GM, and GI). Printed wiring boards conforming to this specification sheet would be comparable to printed wiring boards conforming to MIL-P-55110 or MIL-PRF-55110.

6.5 Tin finishes and whisker growth. Use of tin plating or coating is prohibited (see 3.4.1). The use of alloys with tin content greater than 97 percent, by mass, may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture and can develop under typical operating conditions on products that use such materials. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys containing at least 3 percent lead, by mass, have shown to inhibit the growth of tin whiskers. For additional information on this matter, refer to ASTM B545 (Standard Specification for Electrodeposited Coating of Tin).

6.6 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where changes from the previous issue were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

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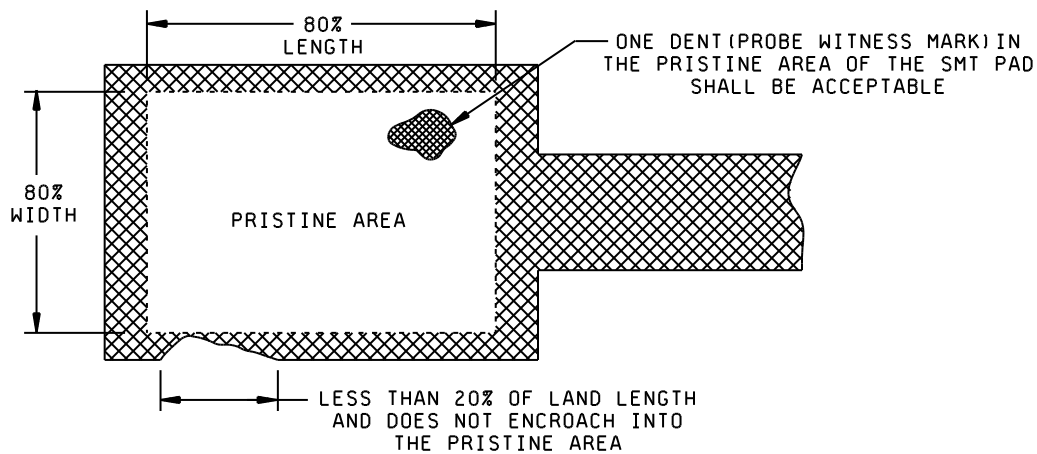


FIGURE 1. Rectangular surface mount lands.

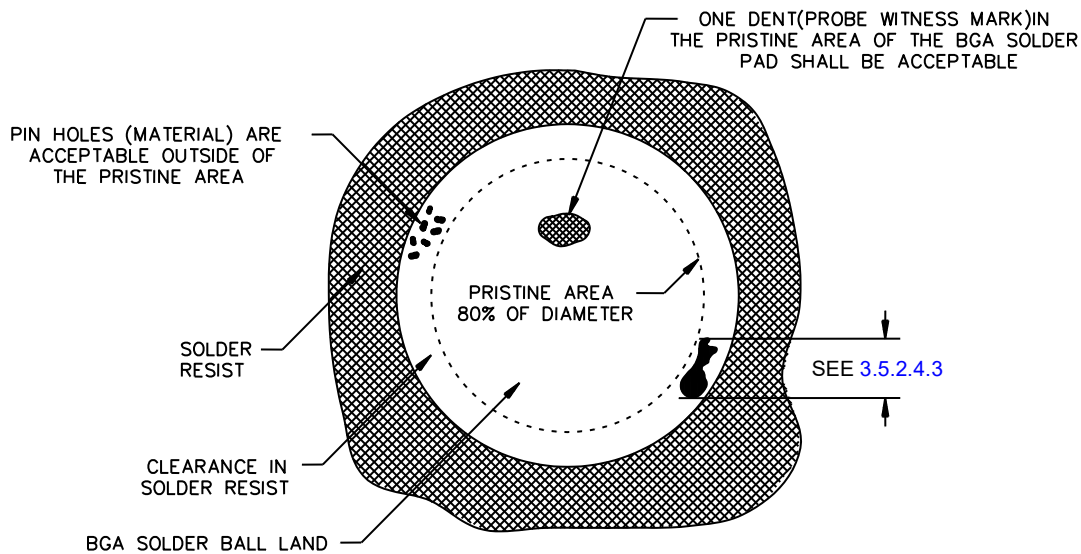


FIGURE 2. Round surface mount lands (BGA pads).



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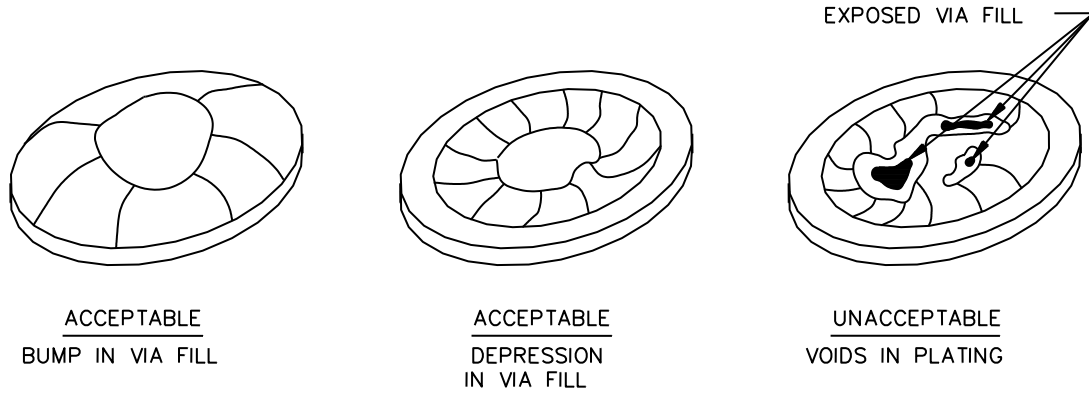


FIGURE 3. Via copper cap plating deviations.

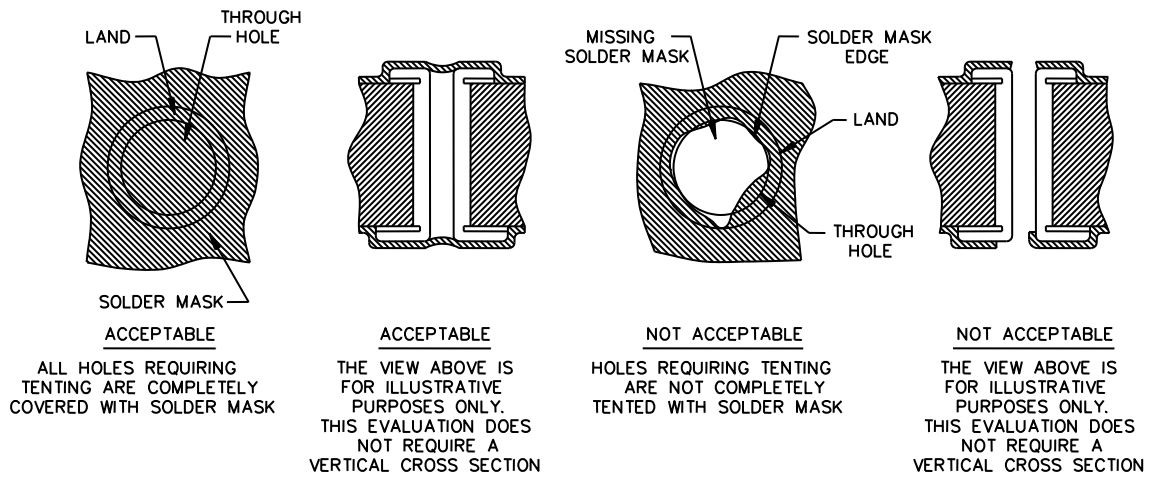
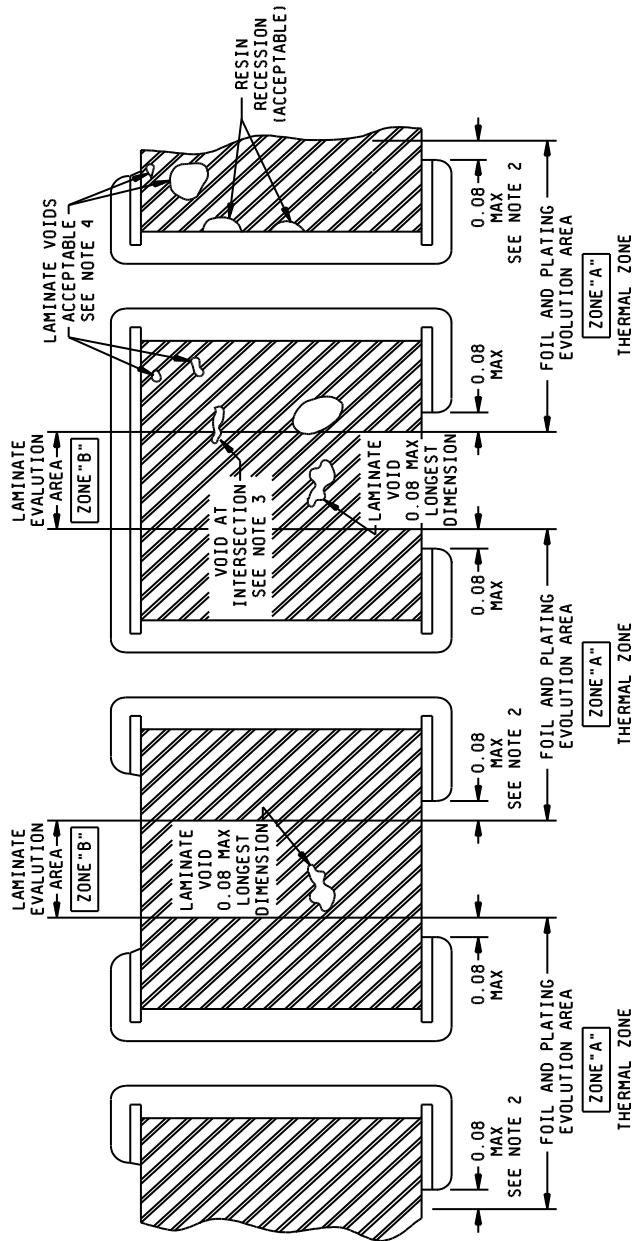


FIGURE 4. Solder mask tenting deviations.

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- NOTES:
1. Dimensions are in millimeters.
  2. Typically beyond land edge most radially extended.
  3. Voids at intersection of zone A and zone B. Laminate voids greater than 0.08 (.003 inch) that extend into zone B are rejectable.
  4. Laminate voids are not evaluated in zone A.

FIGURE 5. Typical plated-through hole cross section after resistance to soldering heat or rework simulation.

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Custodians:

Army – CR  
Navy – EC  
Air Force – 85  
DLA – CC

Preparing activity:

DLA – CC

(Project 5998-2020-002)

Review activities:

Army – AR, MI  
Navy – CG

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.