

The document and process conversion measures necessary to comply with this amendment shall be completed by 11 March 2013.

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## PERFORMANCE SPECIFICATION SHEET

### PRINTED WIRING BOARD, RIGID, SINGLE AND DOUBLE SIDED, THERMOPLASTIC RESIN BASE MATERIAL, WITH OR WITHOUT PLATED-THROUGH HOLES, FOR HIGH FREQUENCY APPLICATIONS

This specification is approved for use by all Departments and Agencies of the Department of Defense.

The requirements for acquiring the product described herein shall consist of this specification sheet and [MIL-PRF-31032](#).

#### 1. SCOPE

1.1 Scope. This specification covers the generic performance requirements for single and double sided (one or two conductor layers) printed wiring boards (hereafter designated printed board) with or without plated holes, constructed of thermoplastic base materials, that will use soldering for component/part mounting (see [6.1](#)). The printed board may contain an external heat sink.

1.2 Classification. Printed boards covered by this specification sheet are classified by the following types and compositions, as specified (see [3.1](#)).

1.2.1 Printed board type. Printed boards covered by this specification sheet are classified by the following types:

Type 1 – Rigid single sided.

Type 2 – Rigid double sided.

1.2.2 Composition. The composition designation is defined by the resin system of the dielectric base material (see [6.5](#)) as follows:

H – Homogenous base material printed boards. Printed board of this composition contain only thermoplastic resin base materials (see [6.5.1](#)).

B – Metal backed printed boards. Printed boards of this composition contain a heavy layer of metal as specified (see [6.5.2](#)).

Comments, suggestions, or questions on this document should be addressed to: DLA Land and Maritime, ATTN: VAC, P. O. Box 3990, Columbus, OH 43218-3990 or emailed to [5998.Documents@dla.mil](mailto:5998.Documents@dla.mil). Since contact information can change, you may want to verify the currency of this address information using the ASSIST Online database at <https://assist.dla.mil>.

1.2.3 Wrap plating (surface and knee continuous copper plating). The wrap plating grade designation is defined by the amount of plated-through hole surface and knee continuous copper plating thickness remaining after surface processing. The grades are as follows:

- A – Printed boards of this grade have 80 percent or more of the specified wrap plating thickness after surface processing.
- B – Printed boards of this grade have 50 percent or more of the specified wrap plating thickness after surface processing.
- C – Printed boards of this grade have 20 percent or more of the specified wrap plating thickness after surface processing.

Unless otherwise specified, the default grade of wrap copper plating is grade A.

## 2. APPLICABLE DOCUMENTS

2.1 General. The documents listed in this section are specified in sections 3, 4, or 5 of this specification. This section does not include documents cited in other sections of this specification or recommended for additional information or as examples. While every effort has been made to ensure the completeness of this list, document users are cautioned that they must meet all specified requirements of documents cited in sections 3, 4, or 5 of this specification, whether or not they are listed.

### 2.2 Government documents.

2.2.1 Specifications, standards, and handbooks. The following specifications, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-PRF-31032 – Printed Circuit Board/Printed Wiring Board, General Specification for.

#### DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-202 – Electronic and Electrical Component Parts.  
MIL-STD-883 – Microcircuits.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch> or <https://assist.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2.2 Other Government documents, drawings, and publications. The following other Government documents, drawings, and publications form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

#### NATIONAL AERONAUTICS AND SPACE ADMINISTRATION (NASA)

NASA 1124 – Outgassing Data for Selecting Spacecraft Materials.

(Hard copies of this document are no longer available from the NASA Goddard Materials Branch or the Document Automation and Production Service Detachment Office (DAPS). This information is only available at <http://outgassing.nasa.gov>.)

2.3 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents are those cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

- ASTM B567 – Standard Test Method for Measurement of Coating Thickness by the Beta Backscatter Method.
- ASTM B568 – Standard Test Method for Measurement of Coating Thickness by X-Ray Spectrometry.
- ASTM D3165 – Standard Test Method for Strength Properties of Adhesives in Shear by Tension Loading of Single-Lap-Joint Laminated Assemblies.
- ASTM E53 – Standard Test Method for Determination of Copper in Unalloyed Copper by Gravimetry.
- ASTM E345 – Standard Test Methods of Tension Testing of Metallic Foil.
- ASTM E595 – Standard Test Method for Total Mass Loss and Collected Volatile Condensable Materials from Outgassing in a Vacuum Environment.

(Application for copies should be addressed to the ASTM International, 100 Barr Harbor Drive, P. O. Box C700, West Conshohocken, PA 19428-2959 or <http://www.astm.org>.)

JEDEC – SOLID STATE TECHNOLOGY ASSOCIATION (JEDEC)

- JESD22-A102 – Accelerated Moisture Resistance – Unbiased Autoclave.

(Application for copies should be addressed to JEDEC – Solid State Technology Association, 3103 North 10th Street, Suite 240-S, Arlington, VA 22201 or <http://www.jedec.org>.)

IPC – ASSOCIATION CONNECTING ELECTRONICS INDUSTRIES (IPC)

- IPC-T-50 – Terms and Definitions for Interconnecting and Packaging Electronic Circuits.
- IPC-A-600 – Acceptability of Printed Boards.
- IPC-OI-645 – Standard for Visual Optical Inspection Aids.
- IPC-TM-650 – Test Methods Manual.
- IPC-CC-830 – Qualification and Performance of Electrical Insulating Compound for Printed Wiring Assemblies.
- IPC-2141 – Design Guide for High-Speed Controlled Impedance Circuit Boards.
- IPC-2221 – Generic Standard on Printed Board Design.
- IPC-2251 – Design Guide for the Packaging of High Speed Electronic Circuits.
- IPC-2252 – Design and Manufacturing Guide for RF/Microwave Circuit Boards.
- IPC-9252 – Requirements for Electrical Testing of Unpopulated Printed Boards.
- J-STD-003 – Solderability Tests for Printed Boards.

(Application for copies should be addressed to the IPC – Association Connecting Electronics Industry, 3000 Lakeside Drive, Suite 309 S, Bannockburn, IL 60015-1249 or <http://www.ipc.org>.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.4 Order of precedence. Unless otherwise noted herein or in the contract, in the event of a conflict between the text of this document and the references cited herein, the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

### 3. REQUIREMENTS

3.1 Printed board detail requirements. Printed boards delivered under this specification sheet shall be in accordance with the requirements as specified herein, and documented in the printed board procurement documentation. Only printed wiring boards which are verified and meet all the applicable performance requirements contained herein and the design, construction, and material requirements of the printed board procurement documentation shall be certified as compliant and delivered.

3.1.1 Conflicting requirements. The order of precedence of conflicting requirements shall be in accordance with [MIL-PRF-31032](#).

3.1.2 Reference to printed board procurement documentation. For the purposes of this specification sheet, when the term "specified" is used without additional reference to a specific location or document, the intended reference shall be to the applicable printed board procurement documentation.

3.1.3 Terms and definitions. The definitions for all terms used herein shall be as specified in [IPC-T-50](#) and those contained herein.

3.2 Qualification. Printed boards furnished under this specification sheet shall be technologies that are manufactured by a manufacturer authorized by the qualifying activity for listing on the applicable qualified manufacturers list before contract award (see [4.2](#) and [6.3](#)).

3.3 Design (see 3.1 and 6.2). Printed boards shall be of the design specified. Unless otherwise noted herein, if individual design parameters are not specified in the printed board procurement documentation, then the baseline design parameters shall be as specified in [IPC-2221](#), [IPC-2141](#), [IPC-2251](#), and [IPC-2252](#), performance class 3. Test coupons shall be as specified in the applicable design standard and shall reflect worst-case design conditions of the printed boards that they represent.

3.3.1 Conductors. This specification sheet differentiates between low frequency conductors, ground planes, and voltage planes and those conductors used for high frequency signals. The terms "signal conductor", "signal line", and "signal plane" are used within this specification sheet to distinguish those conductive patterns from non-critical low frequency conductors, ground planes, and voltage planes.

3.3.2 Critical-controlled conductors and spacings. Unless otherwise specified, when necessary for proper verification of critical-controlled widths or critical-controlled spacings, signal conductors or the spacing between them deemed critical shall be identified as such. The terms "critical-controlled signal conductor", "critical-controlled signal line" and "critical-controlled spacing" are used herein when addressing these type of conductive pattern features.

3.4 Printed board materials. All materials used in the construction of compliant printed boards shall comply with the applicable specifications referenced in the printed board procurement documentation. If materials used in the production of printed boards are not specified, then it is the manufacturer's responsibility to use materials which will meet the performance requirements of this specification sheet. Acceptance or approval of any printed board material shall not be construed as a guarantee of the acceptance of the completed printed board.

3.4.1 Prohibited materials (see 6.6). Unless otherwise specified, electroplated or immersion tin and electroplated silver shall not be used as a finish either externally, internally, or as an undercoat. Electroplated or immersion tin is any tin or tin alloy containing more than 97 percent tin. Tin shall be alloyed with a minimum of three percent lead. The use of tin-lead (Sn-Pb) finishes is acceptable provided that the minimum lead content is three percent. Acceptance or approval of any constituent material shall not be construed as a guaranty of the acceptance of the finished product.

3.5 External visual and dimensional requirements. Printed board test specimens (the finished printed boards or supporting test coupons, as applicable) shall conform to the requirements specified in 3.5.1 through 3.5.5.2. After solder mask application, the printed board test specimens shall also conform to the requirements of 3.5.4. Scratches, dents, and tool marks shall not bridge or expose signal conductors, expose base metal, expose or disrupt reinforcement fibers, reduce dielectric properties, and reduce spacing below the minimum requirements specified herein. The figures, illustrations, and photographs contained in IPC-A-600 can aid in the visualization of externally observable accept/reject conditions of test specimens.

3.5.1 Base material.

3.5.1.1 Edges of base material. Base material edges include the external edge of the printed board, the edges of cutouts, and the edges of non-plated-through holes. Burrs, chips, delaminations, haloing, nicks, and other penetrations along the base material edges of completed printed boards shall be acceptable provided the imperfection does not reduce the edge spacing specified by more than 50 percent. If no edge spacing requirement is specified, the imperfection penetration shall not exceed 2.5 mm (.0984 inch). Loose metallic burrs shall not be acceptable. Base material edges include the external edge of the printed board, the edges of cutouts, and the edges of non-plated-through holes.

3.5.1.2 Surface imperfections. Imperfections in the surface of the base material such as blistering, burrs, cuts, dents, exposed reinforcement material fibers, foreign materials, gouges, nicks, pits, resin scorched areas, resin starved areas, scratches, tool marks, variations in color such as white spots or black spots, or other visual defects detrimental to the performance of the base material shall be acceptable in localized concentrations providing the following conditions are met:

- a. The imperfection does not bridge conductors.
- b. The dielectric spacing between the imperfection and a conductor is not reduced below the specified minimum conductor spacing requirements.
- c. Localized concentration of these imperfections are no closer than 6.5 mm (.26 inch) to any conductor.

3.5.1.2.1 Exposed or disrupted fibers. Exposed or disrupted reinforcement fibers shall not bridge conductors and shall not reduce the conductor spacing below the minimum conductor spacing requirements. Unless otherwise specified, weave texture (reinforcement texture) or weave exposure (exposed reinforcement material fibers) by mechanical fabrication operations shall be acceptable provided that they do not violate the minimum conductor spacing requirements.

3.5.1.2.2 Surface pits and voids. Surface pits and voids in the base material shall be acceptable providing the following conditions are met:

- a. Surface voids are no bigger than 0.8 mm (.031 inch) in the longest dimension.
- b. The surface voids do not bridge conductors.
- c. The total area of all surface voids does not exceed 5 percent of the total printed board area.
- d. The surface void does not affect the performance of the base material.

3.5.1.3 Subsurface imperfections. Subsurface imperfections (such as blistering, crazing, delamination, foreign inclusions, and haloing) shall be acceptable providing the following conditions are met:

- a. The imperfections do not reduce conductor or dielectric spacing below the specified minimum requirements.
- b. The imperfections do not bridge more than 25 percent of the distance between adjacent conductors or plated-through holes and vias that are not electrically common.
- c. The imperfections do not propagate as a result of testing (such as rework simulation, resistance to soldering heat, or thermal shock).
- d. The longest dimension of any single imperfection is no greater than 0.80 mm (.031 inch). In non-circuitry areas, the maximum size shall not be greater than 2.00 mm (.079 inch) in the longest dimension or 0.01 percent of the printed board area, maximum.
- e. No more than two percent of the printed board area on each side shall be affected.

3.5.1.4 Measling and crazing. Unless otherwise specified, measling and crazing shall comply with the class 3 acceptable conditions of [IPC-A-600](#).

3.5.1.5 Bonding material adhesive bleed (when applicable) (see [figure 1](#)). Bonding material adhesive bleed along the junction of a conductor and access hole or cutout shall be acceptable provided the dimension of adhesive bleed onto the conductor is no greater than 0.8 mm (.031 inch) in width. All adhesive in access holes and cutouts shall be firmly bonded to the printed board surface.

### 3.5.2 Conductive pattern.

3.5.2.1 Board edge plating (for shielding). The requirements for plating the edges of the printed board base material shall be as specified.

3.5.2.2 Bonding of conductor to base material and lifted lands. There shall be no peeling or lifting of the conductive pattern (lands or conductors) from the base material. The completed printed board shall not exhibit any lifted land. (NOTE: See [3.6.6](#) for allowances for the acceptable lifting of lands following resistance to soldering heat, rework simulation, and thermal shock testing.)

3.5.2.3 Conductor finish. The conductor finish shall be as specified. Unless otherwise specified, the following requirements shall apply.

3.5.2.3.1 Coverage. The conductor finish shall completely cover the exposed conductive pattern. Complete coverage does not apply to the vertical conductor edges.

3.5.2.3.1.1 Dewetting. For tin alloys, reflowed tin-lead, or solder coated surfaces, a maximum of five percent of dewetting is permitted on any conductive surface where a solder connection will be required. Dewetting on conductors, ground, or voltage planes not used for solder connections shall meet the requirements of [J-STD-003](#).

3.5.2.3.1.2 Nonwetting. For tin alloys, reflowed tin-lead, solder coated surfaces, nonwetting is not permitted on any conductive surface where a solder connection will be required. Absence of solder on the vertical sides of lands shall be acceptable.

3.5.2.3.1.3 Edge board contacts. Unless otherwise specified, these requirements apply to the critical contact area. The critical contact area for edge board contacts shall be as specified.

- a. Defects or surface imperfections in the contact finish shall not expose base metal in critical contact area.
- b. There shall be no nodules or metal bumps in the contact finish in the critical contact area.
- c. Pits, dents, or depressions in the edge board contact finish shall not exceed 0.15 mm (.0059 inch) in their longest dimension. There shall be no more than three occurrences for each edge board contact, and no more than 30 percent of the contacts shall be affected.
- d. Exposed copper, or the overlap of surface finishes at plating junctions, shall be no greater than 0.8 mm (.031 inch). Discoloration of the conductor finish is permitted in the plating overlap zone (see 3.5.2.3.1.4.b).

3.5.2.3.1.4 Plating junctions. Unless otherwise specified, these requirements apply to all junctions of different platings or coatings.

- a. There shall be no exposed copper in the junction of metallic platings or coatings.
- b. An overlap of metallic platings or coatings shall be acceptable if it is no greater than 0.8 mm (.031 inch) in length.
- c. When both solder coating and gold plating are present at a plating junction, a discolored or gray-black area at that plating overlap zone shall be acceptable.

3.5.2.3.2 Conductor finish plating and coating voids in plated-through holes. The conductor finish plating and coating shall not have voids that exceed the following limits:

- a. No more than one final finish void in any plated-through hole.
- b. Not more than five percent of the plated-through holes shall have final finish voids.
- c. Any final finish void present is not more than five percent of the plated-through holes length.
- d. Any final finish void present is less than 90 degrees of the circumference of the plated-through hole.

3.5.2.3.3 Whiskers. There shall be no whiskers of solder or other platings on the surface of the conductive pattern.

3.5.2.4 Lands for component attachment. The lands to be used for component mounting shall be as specified. Imperfections on component hole lands, surface mount lands, or wire bond pads shall not exceed the requirements specified herein.

3.5.2.4.1 Component hole lands. The external annular ring for component hole lands shall be as specified. Unless already at the specified minimum limit, a 20 percent reduction of the specified external annular ring due to defects such as pits, dents, nicks, pinholes, or splay, in isolated areas, shall be acceptable.

3.5.2.4.2 Rectangular surface mount lands (see figure 2). Defects such as nicks, dents, and pin holes along the external edge of the land shall not exceed 20 percent of either the length or width of the land and shall not encroach the pristine area, which is defined by the central 80 percent of the land width by 80 percent of the land length as shown on figure 2. Defects internal to the land shall not exceed 10 percent of the length or width of the land and shall remain outside of the pristine area of the surface mount land. One electrical test probe witness mark is allowed within the pristine area.

3.5.2.4.3 Round surface mount lands (ball grid array [BGA] lands) (see figure 3). Defects such as nicks, dents, and pin holes along the edge of the land shall not radially extend towards the center of the land by more than 10 percent of the diameter of the land and shall not extend more than 20 percent around the circumference of the land as shown on figure 3. There shall be no defects within the pristine area which is defined by the central 80 percent of the land diameter. One electrical test probe witness mark is allowed within the pristine area.

3.5.2.4.4 Wire bond lands. Unless otherwise specified, the maximum conductor finish roughness (surface roughness) for pads or areas designated for wire bonding shall be no greater than 0.8 micrometers (31 micro inches). Unless otherwise specified, the wire bond land bonding area shall be defined as the pristine area as shown on figure 2 for rectangular pads or on figure 3 for round pads. There shall be no pits, nodules, scratches, electrical test probe witness marks, or other defects in the pristine area that exceed the surface roughness limits.

3.5.2.5 Conductor pattern imperfections. Unless otherwise specified, any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce non-critical conductors width by more than 20 percent of its minimum specified width. There shall be no occurrence of the allowed width reductions greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.5.1 Cuts and scratches. A scratch of any length or width is permissible on ground or voltage planes, provided the dielectric is not exposed. Scratches on non-critical conductors may be of any length, but no deeper than 20 percent of the total conductor thickness.

3.5.2.5.2 Dents. A dent of any length or width on ground planes shall be acceptable provided the clad surface is not torn. Dents on conductive patterns may be of any length, but no deeper than 0.013 mm (.0005 inch).

3.5.2.5.3 Pinholes. Pinholes in ground or voltage planes in non-critical areas shall be acceptable provided they have no single diameter greater than 0.5 mm (.0197 inch) and do not exceed three for each 25 mm (.984 inch) diameter. A pinhole in a conductive pattern shall be acceptable, provided they do not reduce the width of a conductive pattern by 10 percent. Pinholes shall be limited to no more than one for each 25 mm (.984 inch) of conductive length.

3.5.2.5.4 Pits. Pits in ground or voltage planes shall be acceptable provided they do not exceed 25 percent of the surface area. Any pit in the conductive pattern is acceptable provided the outline dimension does not exceed 10 percent of the conductor width, and there is no more than one pit for each 25 mm (.984 inch) of the conductor length.

3.5.2.5.5 Superfluous metal. Unless otherwise specified, small particles of metal such as residual copper or subsequent plating after etching, which remain affixed to areas that are intended to be free of conductive material, shall be acceptable providing the following conditions are met:

- a. The conductive particle is no closer than 0.13 mm (.005 inch) to the nearest conductor.
- b. The conductive particle does not reduce the spacing between adjacent conductors to below the minimum spacing specified (see 3.1) or 0.13 mm (.005 inch) when not specified.
- c. The conductive particle is smaller than 0.13 mm (.005 inch) at its greatest diameter or length.
- d. The conductive particle does not affect the electrical parameters of the printed wiring board.



3.5.2.6 Conductor width and spacing.

3.5.2.6.1 Conductor spacing. The conductor spacing between both critical-controlled signal conductors and non-critical conductors shall be as specified.

3.5.2.6.2 Conductor width. The conductor width of both critical-controlled signal conductors and non-critical conductors shall be as specified.

3.5.2.6.3 Width and spacing imperfections.

3.5.2.6.3.1 Critical-controlled signal conductor width imperfections. Unless otherwise specified, conductor width imperfections on direct opposite sides of a critical-controlled signal conductor, when combined, shall not exceed 10 percent of the specified conductor width. A single conductor width deviation along any 25 mm (.984 inch) segment of a specified critical-controlled signal conductor shall be acceptable. The maximum length of any conductor width imperfection shall be no greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.6.3.2 Critical-controlled signal conductor spacing imperfections. Unless otherwise specified, isolated protrusions on multiple critical controlled signal conductors shall not exceed 10 percent of the specified spacing. Unless otherwise specified, conductor protrusions in proximity of, or directly opposite to, adjacent conductor protrusions shall not reduce the specified spacing by more than 10 percent. A single such protrusion is allowed along any 25 mm (.984 inch) segment of the signal conductor pattern with width specified. The maximum length of any conductor protrusions shall be no greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.6.3.3 Non-critical conductor pattern width imperfections. The conductor pattern shall contain no cracks, splits, or tears. Any combination of edge roughness, nicks, pinholes, cuts, or scratches exposing the base material shall not reduce non-critical conductor widths by more than 20 percent. There shall be no occurrence of the acceptable reductions greater than 25 mm (.984 inch) or 20 percent of a conductor length, whichever is less.

3.5.2.6.3.4 Non-critical conductor pattern spacing imperfections. Unless otherwise specified, isolated protrusions on multiple critical controlled signal conductors shall not exceed 10 percent of the specified spacing. Unless otherwise specified, conductor protrusions in proximity of, or directly opposite to, adjacent conductor protrusions shall not reduce the specified spacing by more than 10 percent. A single such protrusion is allowed along any 25 mm (.984 inch) segment of the signal conductor pattern with width specified. The maximum length of any conductor protrusions shall be no greater than 13.0 mm (.51 inch) or 10 percent of a conductor length, whichever is less.

3.5.2.7 Edge plating (for electrical shielding). The requirements for edge plating shall be as specified. The printed board procurement documentation shall define exceptions such as utilizing a ribbon of copper to connect upper and lower ground planes.

3.5.2.8 Via cap plating. Cap plating over filled vias shall meet the requirements of 3.5.5. Unless otherwise specified, there shall be no voids in the cap plating over the filled portion of vias.

3.5.3 Dimensional (interface and physical dimension) requirements. The printed boards shall meet the interface and physical dimensions specified. The dimensional requirements include items such as cutouts, overall thickness, periphery, and other design features specified. In the event that a dimensional characteristic is not specified, then the applicable performance class 3 default requirements of the IPC's 2200 series of documents on the design of printed boards shall apply for that characteristic.

3.5.3.1 Conductor pattern feature accuracy. Conductor pattern feature accuracy shall be as specified.

3.5.3.2 Hole pattern accuracy. The accuracy of the hole pattern (size and location) in the printed board shall be as specified.

3.5.3.3 Hole size. The hole size and tolerance shall be as specified. Unless otherwise specified, hole size tolerance shall be applied after plating. Only specific dimensioned holes, to include both non-plated-through and plated-through, shall be inspected for hole pattern accuracy to meet board dimensional requirements of 3.5.3.2. Nodules or rough plating in plated-through holes shall not reduce the hole diameter below the minimum limits specified.

3.5.3.4 Metal backing materials. When inspected in accordance with 4.7.1, the machining (cutting, drilling, lasing, and tapping) of metal backing materials of printed boards shall meet the dimensional and tolerancing requirements specified.

3.5.3.5 Edge board contacts edge condition. The end, or beveled edge, of edge board contacts shall be smooth with no burrs, roughness, or lifted plating. There shall be no separation of the edge board contacts from the base material or any loose fibers on the beveled edge. Exposed copper on the end, or beveled edge, of the edge board contact shall be acceptable.

3.5.3.6 Slots. The side walls, and if applicable, bottom surfaces of machined slots, shall not contain any burrs, protrusions, or rough edges that decrease the usable area beyond the total profile tolerance specified.

3.5.4 Solder mask (when applicable). The cured solder mask shall not exhibit any chalking, crazing, peeling, skipping, softening, swelling, or wrinkles in excess of the limits specified herein. Unless otherwise specified, the following solder mask conditions shall apply.

3.5.4.1 Coverage. Coverage imperfections (such as blisters, skips, and voids) shall be acceptable providing the following conditions are met:

- a. The solder mask coverage imperfection shall not expose two adjacent electrically isolated lands or conductors whose spacing is less than the electrical spacing required for the voltage range and environmental condition specified in the applicable design standard.
- b. In areas containing parallel conductors, the solder mask coverage imperfection shall not expose two adjacent isolated conductors whose spacing is less than 0.5 mm (.02 inch) unless one of the conductors is a test point, or other feature area, which is purposely left uncoated for subsequent operations.
- c. The exposed conductor(s) shall not be bare copper.
- d. The coverage imperfection does not expose plated-through holes required to be tented.

3.5.4.2 Discoloration. Discoloration of metallic surfaces under the cured solder mask shall be acceptable.

3.5.4.3 Registration. The solder mask shall be registered to the land or terminal patterns in such a manner as to meet the requirements specified. If no requirements are specified, the following shall apply:

- a. Solder mask misregistration onto plated-through component hole lands (plated-through holes to which solder connections are to be made) shall not reduce the external annular ring below the specified minimum requirements. Misregistration shall not expose adjacent, electrically isolated lands or conductors.
- b. Solder mask shall not encroach into plated-through hole barrels, or onto other surface features (such as edge board contacts or lands of unsupported holes), to which solder connections will be made.

- c. Solder mask in plated-through holes or vias in which no lead is to be soldered shall be acceptable.
- d. Unless a partial coverage allowance is specified, test points which are intended for assembly testing shall be free of solder mask.
- e. On areas where the conductor pattern continues under solder mask, there shall be no exposed copper at the conductor finish to solder mask interface. Unless otherwise specified, the conductor finish plating or coating extending a maximum of 0.25 mm (.00984 inch) under the edge of the solder mask shall be acceptable.
- f. Unless otherwise specified, solder mask encroachment onto surface mount lands shall comply with the following:
  - (1) On surface mount lands with a pitch of 1.25 mm (.05 inch) or greater, encroachment is on one side of the land only and does not exceed 0.05 mm (.002 inch).
  - (2) On surface mount lands with a pitch less than 1.25 mm (.05 inch), encroachment is on one side of the land only and does not exceed 0.025 mm (.00098 inch).

3.5.4.4 Thickness. Solder mask thickness shall be as specified.

3.5.4.5 Solder mask cure. The cured solder mask coating shall not exhibit tackiness, blistering, or delamination.

3.5.4.6 Soda straw voids. There shall be no visible soda straw voids between the solder mask and the printed board base material surface and the edges of the conductor patterns.

3.5.5 Via protection.

3.5.5.1 Filled via, resin, cap plating (see figure 4). When the printed board design requires the copper cap plating of filled vias (see 3.1), all vias required to be protected shall be completely covered by the cap plating. Visually discernable protrusions (bumps) and depressions (dimples) in the copper plating over filled vias shall be acceptable providing they meet the requirements of 3.6.5. Voids in the copper cap plating over the filled portion of the via shall not be acceptable.

3.5.5.2 Unfilled via, solder mask tenting (see figure 5). When the printed board design requires the tenting of solder mask over unfilled vias (see 3.1), all vias required to be protected shall be completely covered by solder mask. Voids in the solder mask over the via exposing the hole shall not be acceptable.

3.6 Plated hole structural requirements (doubled sided only) (by microsectioning) (see figure 6). Vertical cross sections of printed board test specimens (production printed boards or test coupons) shall conform to the requirements in 3.6.1 through 3.6.8, as applicable. Barrel cracks, butt plating joints, circumferential separations, corner cracks, and cracked copper plating shall not be acceptable. IPC-A-600 contains figures, illustrations, and photographs that can aid in the visualization of internally observable accept/reject conditions of cross sectioned test specimens.

3.6.1 Base material. Unless otherwise specified, the base material imperfections shall apply.

3.6.1.1 Dielectric layer thickness. The minimum dielectric thickness between conductor layers shall be as specified.

3.6.1.2 Laminate cracks and voids. Laminate voids with the longest dimension of 0.08 mm (.003 inch) or less shall be acceptable provided the conductor spacing is not reduced below the minimum dielectric spacing requirements, laterally or vertically, as specified. After undergoing rework simulation (see 3.7.4.7), resistance to soldering heat (see 3.7.6.2) or thermal shock (see 3.7.6.3), laminate voids are not evaluated in zone A (see figure 4).

3.6.1.3 Resin recession. Resin recession at the outer surface of the plated hole barrel shall be permitted and is not cause for rejection.

3.6.2 Conductor finish. The conductor finish shall be as specified (see 3.1). Unless otherwise specified, the following conductor finish conditions specified shall apply.

3.6.2.1 Outgrowth and overhang. There shall be no outgrowth on the conductor edges when finished with fused tin-lead or solder coating. The maximum permissible outgrowth on conductor edges finished with surface finish metals other than tin-lead or solder shall be 0.025 mm (.00098 inch).

3.6.2.2 Thickness (plating or coating). The plating or coating thickness of the conductor finish shall be as specified. Voids in any conductor finish plating coating shall meet the requirements of 3.6.5.3.a and 3.6.5.3.b.

3.6.2.3 Protective finishes for metal backing materials. The plating, coating, or surface treatment type and thickness of metal backing materials shall be as specified (see 3.1).

3.6.3 Conductor thickness. The conductor thickness shall be as specified (see 3.1).

3.6.3.1 Minimum thickness of copper foil with copper plating. When a conductor thickness is specified, the conductor thickness (copper foil and copper plating) shall be equal to or greater than the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (copper foil and copper plating) shall be within the specified tolerance for the specified thickness. If only a starting copper foil weight requirement is specified, the thickness limits for conductors with plating shall meet the class 3 requirements for External Conductor Thickness After Plating table of IPC-2221. If only final copper foil weight requirement is specified, the limits for minimum conductor thickness shall be as defined by the procuring activity.

3.6.3.2 Minimum thickness of copper foil without additional copper plating. When a minimum conductor thickness is specified, the conductor thickness (copper foil) shall be equal to or greater than the specified thickness. When a conductor thickness with tolerance is specified, the conductor thickness (copper foil) shall be within the specified tolerance for the specified thickness. If only a starting copper foil weight requirement is specified, the limits for minimum internal layer foil thickness after processing shall be in accordance with Internal Layer Foil Thickness After Processing table of IPC-2221.

3.6.4 Conductor width. The conductor width shall be as specified (see 3.1).

3.6.5 Plated-through hole plating. Unless otherwise specified, copper plating thickness applies to the hole wall, the hole knee, and the surface land of the plated-through hole.

3.6.5.1 Copper plating thickness. Unless otherwise specified, the copper plating thickness shall be in accordance with the applicable design standard. Any hole wall copper plating thickness less than 90 percent of the specified thickness shall be treated as a void. Any 10 percent thickness reduction shall be non-continuous (isolated; not more than 10 percent of the composite board thickness).

3.6.5.2 Wrap copper plating. Unless otherwise specified, the plated-through hole wrap plating (continuous hole-knee-surface copper plating) thickness (see 1.2.3) shall be as specified. The wrap plating shall not be reduced by more than 80 percent for grade A, 50 percent for grade B, and 20 percent for grade C of the specified wrap copper plating thickness due to planarization or other processing (see figure 7).

3.6.5.3 Copper plating voids. The copper plating in the plated-through hole shall not exhibit any void in excess of the following:

- a. There shall be no more than one plating void for each panel, regardless of length or size.
- b. There shall be no plating void longer than five percent of the total printed board thickness.

Conductor finish plating or coating material between the base material and copper plating (i.e., behind the hole wall copper plating) is evidence of a void. Any plated-through hole exhibiting this condition shall be counted as having one void for panel acceptance purposes.

3.6.5.4 Hole wall dielectric to plated barrel separation. There shall be no separations between the plated hole barrel and dielectric wall, or resin recession in the non-stressed test specimens. Resin recession greater than 0.08 mm (.003 inch) depth, or more than 40 percent of cumulative dielectric thickness, shall be acceptable in the post resistance to soldering heat test specimens.

3.6.5.5 Miscellaneous hole and plating deficiencies. Burrs, nodules, plating folds, or plated reinforcement material fibers that project into the copper plating shall be acceptable provided that the hole diameter and the hole wall copper thickness are not reduced below their specified limits. Butt plating joints, circumferential separations, corner cracks, and cracked plating shall not be acceptable.

3.6.5.6 Wicking. Wicking of copper plating extending 0.08 mm (.003 inch) into the base material shall be acceptable provided it does not reduce the conductor spacing below the minimum clearance spacing requirements specified.

3.6.6 Lifted lands (after rework simulation, resistance to soldering heat, or thermal shock) (see figure 8). After undergoing rework simulation (see 3.7.4.7), resistance to soldering heat (see 3.7.6.2) or thermal shock (see 3.7.6.3), the maximum allowed lifted land distance from the printed board surface plane to the outer lower edge of the land shall be the thickness (height) of the terminal area or land. The completed, non-stressed printed board shall not exhibit any lifted lands.

3.6.7 Metallic cracks. There shall be no cracks in the platings or coatings. For terminal or land areas plated with copper, cracks are permissible in the external layer (outer) copper foil provided they do not extend into the plated copper.

3.6.8 Undercutting. Undercutting of the edge of the conductor shall not exceed the total thickness of copper foil and copper plating, or 10 percent of the conductor width, whichever is least.

### 3.6.9 Via cap plating.

3.6.9.1 Thickness. For designs that specify copper plating for via protection, the minimum via cap plating thickness over filled vias shall be as specified (see 3.1). Unless otherwise specified, the minimum via cap copper plating thickness over filled vias shall be in accordance with wrap plating thickness specified (see 1.2.3).

3.6.9.2 Cap plating imperfections (see figures 9 and 10). When cap plating of a filled via is specified (see 3.1), voids in the plating over the via fill shall not be acceptable. Separation of the via cap plating to via fill material shall be acceptable. Separation of the via cap plating to underlying plating shall not be acceptable.

3.6.9.3 Via fill imperfections. Depressions (dimples) below the surface of the land shall be no greater than 0.08 mm (.003 inch). Protrusions (bumps) of the cap plating above the surface of the land shall be no greater than 0.05 mm (.002 inch).

3.7 Performance requirements. The performance requirements specified in 3.7.1 through 3.7.6.3 shall be verified by the test methods detailed in 4.7. Unless otherwise specified by the Technical Review Board (TRB), test optimization in accordance with MIL-PRF-31032 may be used, but the printed boards shall be capable of meeting all of the performance requirements specified herein and as specified, regardless of the verification method used.

3.7.1 Acceptability (visual and dimensional acceptability of printed boards). When examined as specified in 4.7.1, the printed boards shall conform to the acceptance requirements specified in 3.3 (design), 3.4 (material), 3.5 (external visual and dimensional), 3.8 (marking), and 3.9 (workmanship), inclusive.

3.7.2 Destructive physical analysis (DPA) by microsectioning and evaluation of printed board test specimens. When printed board test specimens (completed printed boards, supporting test coupons, or qualification test specimens) are vertically cross sectioned and examined as specified in 4.7.2, the requirements specified in 3.1, 3.3, and 3.6 shall be met. Non-stressed test specimens shall be evaluated when examination of the stressed cross sections suggest that a failure condition may exist in the completed boards (prior to resistance to soldering heat).

### 3.7.3 Chemical requirements.

3.7.3.1 Ionic contamination (cleanliness). When printed board test specimens are tested in accordance with 4.7.3.1, the levels of ionic contamination shall be in accordance with the requirements of 3.7.3.1.1 or 3.7.3.1.2, as applicable.

3.7.3.1.1 Prior to the application of solder mask (when applicable). Unless otherwise specified, prior to the application of solder mask, the level of ionic contamination shall not exceed 1.56 micrograms/square centimeter (10.06 micrograms/square inch).

3.7.3.1.2 Completed printed boards (when specified, see 3.1 and 6.2.1.a). The levels of ionic contamination for completed printed boards shall be as specified.

### 3.7.3.2 Copper plating characteristics.

3.7.3.2.1 Elongation of copper. When copper plating is tested in accordance with 4.7.3.2.1, the elongation shall be 12 percent minimum.

3.7.3.2.2 Tensile strength of copper. When copper plating is tested in accordance with 4.7.3.2.2, the tensile strength shall be 248 MPa (36,000 psi) minimum.

3.7.3.2.3 Purity of copper. When copper plating is tested in accordance with 4.7.3.2.3, the purity of the copper shall be 99.50 percent minimum.

### 3.7.4 Physical requirements.

3.7.4.1 Adhesion, marking. After marking is tested in accordance with 4.7.4.1, any specified markings which are missing in whole or in part, faded, shifted (dislodged), or smeared to the extent that it is no longer legible shall constitute failure. A slight change in the color of ink or paint markings after the test shall be acceptable.

3.7.4.2 Adhesion, plating. When tested as specified in 4.7.4.2, there shall be no part of the conductor pattern or copper plating protective finish (coating or plating) removed from the printed board test specimen except for those related to outgrowth, overhang, or slivers.

3.7.4.3 Adhesion, solder mask (when applicable). When tested as specified in 4.7.4.3, the maximum percentage of cured solder mask lifted from the surface of the base material, conductors, and lands of the coated printed board test specimen shall not exceed the following limits:

- a. Bare copper or base material: Zero percent.
- b. Non-melting metals (e.g., gold or nickel plating): Five percent.
- c. Melting metals (e.g., tin-lead plating, solder coating, indium, bismuth, and others): Ten percent.

3.7.4.4 Bow and twist (when specified). When printed boards are tested as specified in 4.7.4.4, the maximum limit for bow and twist shall be as specified.

### 3.7.4.5 Component attachment.

3.7.4.5.1 Solderability (see 6.2.1.b). Printed boards that require soldering during assembly processes require solderability testing. Printed boards using only surface mount component do not require hole solderability testing. Printed board designs that do not require soldering to attach components (as in the case where press-fit components or wire bonding are used) do not require solderability testing. When required by the procurement documentation, accelerated conditioning for coating durability shall be in accordance with J-STD-003. The default category of coating durability of J-STD-003 is category 2. Printed board designs that are constructed in part or entirely of ceramic filled base materials, or have heavy backing may experience hole solderability non-compliance when using test method C of J-STD-003 due to the thermal conductivity of the base material or backing material. Other solderability test conditions of J-STD-003 should be used in order to ensure compliance to the solderability requirement of this specification sheet.

3.7.4.5.1.1 Hole solderability. After undergoing the test specified in 4.7.4.5.1, the holes on the printed board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.4.5.1.2 Surface solderability. After undergoing the test specified in 4.7.4.5.1, the lands on the printed board test specimen shall conform to the class 3 acceptance criteria specified in J-STD-003.

3.7.4.5.2 Wire bond pull strength (when specified, see 3.1). When inspected as specified in 4.7.4.5.2, plated bonding areas shall be capable of meeting the requirements of table I of method number 2.4.42.3 of IPC-TM-650 without incurring any of the following failures:

- a. Wire bond failure (interface between wire and conductive layer).
- b. Separation of conductive layers on the bonding area.
- c. Bonding area lifted from the base material.

3.7.4.5.2.1 Failure criteria. Any bond pull which results in separation of bonds at the bond interface at an applied stress less than the specified stress for the applicable material and construction shall constitute a failure. Unless otherwise specified, the applied nondestructive pull stress shall be 80 percent of the minimum bond strengths for the applicable material, size and construction given in table I of method number 2.4.42.3 of IPC-TM-650.

3.7.4.6 Lap shear strength (for designs with metal backing material). When inspected as specified in 4.7.4.6, lap shear strength shall meet or exceed the requirements specified (see 3.1). Unless otherwise specified, the lap shear strength test specimens shall not exhibit adhesion failure. Cohesion failure shall be acceptable.

3.7.4.7 Rework simulation.

3.7.4.7.1 Unsupported land. After undergoing the test specified in 4.7.4.7, the lands on the printed board test specimens shall withstand 2.27 kg (5 pounds) or 3.45 MPa (500 psi), whichever is less, after completion of the five cycles of soldering and four cycles of desoldering.

3.7.4.7.2 Plated holes. After undergoing the test specified in 4.7.4.7, the printed board test specimens shall meet the following requirements:

- a. External visual and dimensional inspection: When inspected as specified in 4.7.1, there shall be no evidence of blistering or delamination in excess of that allowed in 3.5.
- b. Internal visual and dimensional inspection: The printed board test specimens shall undergo DPA by microsectioning and evaluation of test specimen in accordance with 4.7.2 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.5 Electrical requirements.

3.7.5.1 Continuity and isolation (circuit shorts).

3.7.5.1.1 Continuity. When tested in accordance with 4.7.5.1, unless otherwise specified, there shall be no circuit whose resistance exceeds 10 ohms. For referee purposes, 0.5 ohm maximum for each 25.0 mm (.984 inch) of circuit length shall apply.

3.7.5.1.2 Isolation (circuit shorts). When tested as specified in 4.7.5.1, the resistance between mutually isolated conductors shall be greater than 100 megohms.

3.7.5.2 Dielectric withstanding voltage.

3.7.5.2.1 DC voltage, after moisture and insulation resistance (MIR). When tested as specified in 4.7.5.2.1, printed boards shall withstand the application of the specified voltage for the specified duration without any dielectric breakdown, flashover, or sparkover between conductors.

3.7.6 Environmental requirements.

3.7.6.1 Moisture and insulation resistance. When tested as specified in 4.7.6.1, the printed board test specimen shall have a minimum of 500 megohms of resistance between conductors. After the test, the printed board test specimen shall not exhibit blistering, measing, or delamination in excess of that allowed in 3.5.1.



3.7.6.2 Resistance to soldering heat.

3.7.6.2.1 Solder float thermal stress.

3.7.6.2.1.1 Unsupported holes. After undergoing the test specified in 4.7.6.2.1, the printed board test specimen shall be inspected in accordance with 4.7.1 and not exhibit any cracking or separation of plating or conductors, terminals or lands shall not lift in excess of that allowed in 3.6.6, and blistering or delamination shall not exceed the limits in 3.5.

3.7.6.2.1.2 Plated holes. After undergoing the test specified in 4.7.6.2.1, the printed board test specimen shall be inspected in accordance with 4.7.1 and blistering or delamination shall not exceed the limits in 3.5. The printed board test specimen shall then be microsectioned and inspected in accordance with 4.7.2 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.6.2.2 Solder reflow thermal stress (for surface mount designs). After undergoing the test specified in 4.7.6.2.2, the printed board test specimen shall be inspected in accordance with 4.7.2 and shall meet the requirements of 3.1, 3.3, and 3.6.

3.7.6.3 Thermal shock. While undergoing the test specified in 4.7.6.3, a resistance change of 10 percent or more between the first and last high temperature measurements shall be considered a reject. After the test, when printed wiring board test specimens are inspected as specified in 4.7.1, there shall be no evidence of plating cracks, blistering, or delamination in excess of that allowed in 3.5.1.3.

3.7.6.4 Direct current induced thermal cycling (when specified, see 3.1). After undergoing the test specified in 4.7.6.4, the printed board test specimen shall be inspected in accordance with 4.7.2 and shall meet the requirements of 3.5. For capability verification inspection testing, the following conditions shall be considered:

- a. Number of samples: Six.
- b. Test temperature: 150 degrees Celsius.
- c. Resistance change: 10 percent.
- d. Maximum number of cycles: 250 for each 24 hour period.
- e. Data collection frequency: 10 cycles.
- f. Cooling ratio: 0.66.
- g. Table selection: System.

3.7.7 Optional requirements.

3.7.7.1 Optional visual requirements.

3.7.7.1.1 Optional visual inspection (when specified, see 3.1). When specified, each printed board shall be visually inspected to assure conformance with the applicable requirements of test method 2032 of MIL-STD-883, and the applicable printed board procurement documentation.

3.7.7.1.2 Surface examination of conductors (when specified, see 3.1). When specified, the surface of the printed board specimen shall be inspected for additional criteria detailed in the printed board procurement documentation.

3.7.7.1.3 Laser marking legibility test (applicable to laser marked printed boards) (when specified, see 3.1). When printed board specimens are tested as specified in 4.7.7.1.3, the marking shall remain legible.

3.7.7.1.4 Fused tin-lead plate coverage (when used as a surface finish) (when specified, see 3.1). After fusing of tin-lead plating, the resulting solder coating shall homogeneous and completely cover the terminal pads and conductors with no pitting, pinholes, or nonwetted areas. The fused tin-lead solder coating coverage is not applicable to the sidewalls of terminals or conductors.

3.7.7.2 Optional dimensional requirements.

3.7.7.2.1 Hole size, drilled (when specified, see 3.1). When drilled holes are inspected in accordance with 4.7.7.2.1, the hole size shall be within the specified tolerance.

3.7.7.2.2 Hole size, plated (when specified, see 3.1). When plated holes are inspected in accordance with 4.7.7.2.2, the hole size shall be within the specified tolerance.

3.7.7.2.3 Tin-lead plating thickness (intended to be a surface finish) (when specified, see 3.1). When tin-lead plating is inspected prior to fusing, it shall be 0.00762 mm (.0003 inch) minimum.

3.7.7.2.4 Solder mask thickness (when specified, see 3.1). When solder mask is inspected in accordance with 4.7.2, the thickness shall be within the specified tolerance.

3.7.7.3 Optional chemical testing.

3.7.7.3.1 Organic contamination (when specified, see 3.1). When non-solder mask coated printed boards are tested in accordance with 4.7.7.3.1, any visual evidence of organic residue shall constitute a failure.

3.7.7.3.2 Resistance to solvents (marking inks or paints) (when specified, see 3.1). After marking is tested in accordance with 4.7.7.3.2, any specified markings which are missing in whole or in part, faded, smeared, or shifted (dislodged) to the extent that they cannot be readily identified shall constitute failure.

3.7.7.4 Optional physical requirements.

3.7.7.4.1 Coefficient of thermal expansion (CTE) (when specified, see 3.1). When tested as specified in 4.7.7.4.1, printed board test specimens that have metal cores or other constraining materials and a requirement to constrain the thermal expansion in the planar directions, the CTE shall be within  $\pm 2$  ppm for each degree Celsius for the CTE and temperature range specified.

3.7.7.4.2 Die to die pad shear strength (diebond adhesion) (when specified, see 3.1). When tested as specified in accordance with 4.7.7.4.2, the die to die pad attach area shall exhibit a minimum shear strength as follow:

- a. All die with an area larger than 4.0 square mm ( $64 \times 10^{-4}$  square inch) shall withstand a minimum force of 2.5 kg.
- b. All die with an area smaller than or equal to 4.0 square mm ( $64 \times 10^{-4}$  square inch) shall withstand a minimum force of 62.5 kg per square cm.

3.7.7.5 Optional electrical requirements.

3.7.7.5.1 Impedance testing (when specified, see 3.1). When impedance resistance values are specified, all printed boards shall be electrically testing tested as specified in 4.7.7.5.1.

3.7.7.5.2 Characteristic impedance of conductors (when specified, see 3.1). When conductors are tested as specified in 4.7.7.5.2, the characteristic impedance shall be within the specified tolerance of the nominal impedance (see 3.1).

3.7.7.5.3 Dielectric withstanding voltage.

3.7.7.5.3.1 AC voltage (hi-pot). When tested as specified in 4.7.7.5.3.1, printed boards shall withstand the application of the specified voltages for the specified duration without arcing, breakdown of insulation, or damage. There shall be no leakage current greater than that specified.

3.7.7.5.3.2 DC voltage, reduced barometric pressure (when specified, see 3.1). When tested as specified in 4.7.7.5.3.2, printed boards shall withstand the application of the specified voltages for the specified duration without any momentary or intermittent arcing, breakdown of insulation, nor shall there be any visible evidence of damage. There shall be no leakage current greater than that specified.

3.7.7.5.4 Surface insulation resistance (as received) (when specified, see 3.1). When tested as specified in 4.7.7.5.4, the resistance between mutually isolated conductors shall be greater than 500 megohms.

3.7.7.6 Optional environmental requirements.

3.7.7.6.1 Accelerated moisture resistance (when specified, see 3.1). After undergoing the test specified in 4.7.7.6.1, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. A resistance increase of 10 percent or more shall be considered a reject.

3.7.7.6.2 Fungus resistance (when specified, see 3.1). All external materials shall be non-nutrient to fungus growth or shall be suitably treated to retard fungus growth. The manufacturer shall certify that all external materials are fungus resistant or shall perform the test specified in 4.7.7.6.2. There shall be no evidence of fungus growth on the external surfaces.

3.7.7.6.3 Mechanical shock (specified pulse) (when specified, see 3.1). After undergoing the test specified in 4.7.7.6.3, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. The requirements of 3.5 shall be met when specified.

3.7.7.6.4 Outgassing (when specified, see 3.1) (see 6.2.1.e). When inspected as specified in 4.7.7.6.4, unless otherwise specified, the printed board test specimens shall meet the following requirements:

- a. Total mass loss (TML) shall not exceed 1.0 percent.
- b. Collected volatile condensable material (CVCM) shall not exceed 0.1 percent.

Materials data listed in the latest revision of NASA Publication 1124 which meet these TML and CVCM may be used in lieu of actual testing of the materials.

3.7.7.6.5 Radiation hardness (when specified, see 3.1). When printed board specimens are tested as specified in 4.7.7.6.5, there shall be no defects such as measing, delamination, or weave texture. The insulation resistance between conductors shall be not less than 500 megohms. After the test, the requirements specified in 3.7.5.2 (DWV) shall be satisfied.

#### 3.7.7.6.6 Vibration.

3.7.7.6.6.1 Vibration, sinusoidal (when specified, see 3.1). After undergoing the test specified in 4.7.7.6.6.1, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. Unless otherwise specified, the requirements specified in 3.5.1.2, 3.5.1.3, and 3.7.4.4 shall be met.

3.7.7.6.6.2 Vibration, resonance dwell (when specified, see 3.1). After undergoing the test as specified in 4.7.7.6.6.2, the printed board test specimen shall be capable of meeting the requirements specified in 3.7.5.1 and 3.7.5.2. Unless otherwise specified, the requirements specified in 3.5.1.2, 3.5.1.3, and 3.7.4.4 shall be met.

#### 3.8 Marking.

3.8.1 Product identification and traceability. Product identification and traceability marking shall be in accordance with MIL-PRF-31032.

3.8.2 Marking legibility. After any or all tests, marking that is either etched, screened, or ink stamped shall comply with the class 3, acceptable conditions detailed in IPC-A-600.

3.9 Workmanship. Printed boards shall be processed in such a manner as to be uniform in quality and shall be free from defects that will affect life, serviceability, or appearance.

### 4. VERIFICATION

4.1 Classification of inspections. The inspection requirements specified herein are classified as follows:

- a. Qualification inspection (see 4.2).
- b. Conformance inspection (see 4.3 and table I and II).
- c. Capability verification inspection (see 4.6).

4.1.1 Sampling and inspection. Sampling and inspection shall be in accordance with MIL-PRF-31032, and as specified herein.

4.1.2 Standard test and inspection conditions. Unless otherwise specified by the applicable test method or procedure, inspections and tests may be performed at ambient conditions.

4.2 Qualification inspection. Unless otherwise specified by the TRB approved qualification test plan, qualification inspection shall be in accordance with MIL-PRF-31032 and as specified herein.

4.2.1 Qualification test vehicles. The qualification test vehicles to be subjected to qualification inspection shall be in accordance with the TRB approved qualification test plan and the applicable qualification test vehicle specifications.

4.2.1.1 Sample. The number of qualification test vehicles to be subjected to qualification inspection shall be in accordance with TRB approved qualification test plan.

4.2.2 Test routine. The qualification test vehicles shall be subjected to the inspections and tests specified in tables I, II and III.

4.2.3 Qualification by similarity. A production lot may be considered qualified by similarity if the dimensional parameters are within 10 percent of those currently qualified and the processing steps used are a set or subset of those processes used for a previous qualified technology. When producing printed board designs that exceed the currently qualified process limits, the TRB shall review and approve the lot conformance inspection data before release of the final product.

4.3 Conformance inspection. Conformance inspection shall be in accordance with MIL-PRF-31032 and shall consist of lot conformance inspection (see 4.4) and periodic conformance inspection (see 4.5).

4.4 Lot conformance inspection. Lot conformance inspection shall be in accordance with MIL-PRF-31032 and table I herein. Panels, pallets, and printed boards to be delivered in accordance with this specification sheet shall have been subjected to and passed all applicable inspections and tests of table I prior to delivery of product. Lot conformance inspection testing by subgroup or within a subgroup may be performed in any sequence.

4.4.1 Sample inspections. Panels and printed boards to be delivered in accordance with this specification sheet shall have been subjected to, and passed, all the inspections of table I, subgroups 1, 2, 3, 4, and 5.

4.4.1.1 Sampling. Samples shall be randomly selected from each inspection lot. The lot conformance inspection sample plan uses a two-character designator that identifies the inspection specimen (first letter) and the C=0 sample size series (second letter) in accordance with appendix E of MIL-PRF-31032. The letter "B" is used as the first letter when pallets or production printed boards are to be sampled in their deliverable form. The letter "T" is used as the first letter when test vehicles (test coupons or partial or whole production panels) are to be sampled based on the number of panels in the lot. The second letter of the two-character designator uses the letters "H", "J", and "N" to identify the C=0 sample size series. The C=0 sample size series identifies the number to sample based on the lot size.

4.4.1.1.1 Panels and pallets. When a verification is performed when the printed boards are still on either a partial or whole production panel, the number to be sampled shall be the number of production panels in the lot, not the number of printed boards on the production panel. When the deliverable item is a pallet (or array) of printed boards, the number to be used for sampling is the number of pallets in the lot, not the number of printed boards on the pallet.

4.4.1.1.2 Test coupons. When using the "S" test coupon, the number of samples to be tested shall be based on a statistical sample of the inspection panels in the lot using plan TJ. When using the "A" test coupon, the number of samples to be tested shall be based on the same statistical sample as the "S" test coupon, but a multiple of 4 shall be applied to the resulting sample size. The "A" test coupons shall be selected in groups of 4, taken from the same inspection panel.

4.4.1.2 Percent defective allowable (PDA) limits. When 100 percent of a production lot is inspected, either in lieu of sampling or due to rejection of a sample inspection lot, the PDA limits for this 100 percent inspection shall be 50 percent.

TABLE I. Lot conformance inspection.

| Inspection                   | Requirement paragraph | Method paragraph | Specimen to test <u>1/</u> |           |             |           | Sample plans and notes <u>2/</u> |
|------------------------------|-----------------------|------------------|----------------------------|-----------|-------------|-----------|----------------------------------|
|                              |                       |                  | B/P                        | THM       | SMT         | MIX       |                                  |
| Subgroup 1                   |                       |                  |                            |           |             |           |                                  |
| Resistance to soldering heat | 3.7.6.2               | 4.7.6.2          |                            | A and B   | A and B     | A and B   | Plan TJ                          |
| Subgroup 2                   |                       |                  |                            |           |             |           |                                  |
| Acceptability                | 3.7.1                 | 4.7.1            | X                          |           |             |           | Plan BH or TJ <u>3/</u>          |
| Subgroup 3                   |                       |                  |                            |           |             |           |                                  |
| Ionic contamination          | 3.7.3.1.1             | 4.7.3.1          | X                          |           |             |           | Plan BN or TN <u>4/ 5/</u>       |
| Subgroup 4                   |                       |                  |                            |           |             |           |                                  |
| Physical:                    |                       |                  |                            |           |             |           |                                  |
| Adhesion, marking            | 3.7.4.1               | 4.7.4.1          | X                          | <u>6/</u> | <u>6/</u>   | <u>6/</u> | Plan BH or TJ <u>5/</u>          |
| Adhesion, plating            | 3.7.4.2               | 4.7.4.2          | X                          | C         | C           | C         | Plan BH or TJ <u>5/ 7/</u>       |
| Adhesion, solder mask        | 3.7.4.3               | 4.7.4.3          | X                          | G         | T <u>8/</u> | G – T     | Plan BH or TJ <u>5/ 8/</u>       |
| Bow and twist                | 3.7.4.4               | 4.7.4.4          | X                          |           |             |           | Plan BH                          |
| Solderability                |                       |                  |                            |           |             |           |                                  |
| Hole                         | 3.7.4.5.1.1           | 4.7.4.5.1        |                            | S or A    |             | A or S    | Plan TJ <u>9/</u>                |
| Surface                      | 3.7.4.5.1.2           | 4.7.4.5.1        |                            |           | C or M      | C or M    | Plan TJ                          |
| Subgroup 5                   |                       |                  |                            |           |             |           |                                  |
| Continuity and isolation     | 3.7.5.1               | 4.7.5.1          | X                          |           |             |           | 100 percent <u>10/</u>           |

1/ Test coupons are in accordance with IPC-2221. B/P is either a production printed board separated from the panel, a pallet of boards, or a partial or whole production panel of printed boards; THM is a through-hole mount test coupon; SMT is a surface mount PWB test coupon; MIX is for printed board designs containing both through-hole and surface mount components test coupon.

2/ See MIL-PRF-31032 for C = 0 sampling plans. See 4.4.1.1 for explanation of codes.

3/ See 4.4.1.1.1 for test specimen selection options. Surface imperfections (3.5.1.2) and subsurface imperfections (3.5.1.3) shall be inspected prior to solder mask application.

4/ Inspection shall be performed prior to solder mask application. Additional inspections on completed printed boards may be specified.

5/ The test specimen(s) to be examined can be either a test coupon, partial or whole production panel, pallet or production printed board, to be determined by the manufacturer.

6/ See 4.7.4.1 for test specimen description and quantity.

7/ All surface platings or coatings shall be inspected.

8/ The "T" test coupon shall be used when production printed boards have tented via holes.

9/ For designs containing plated holes (see 4.4.1.1.2).

10/ Type 2 only.

4.5 Periodic conformance inspection. Periodic conformance inspection shall be in accordance with TRB approved periodic conformance inspection plan or table II herein.

TABLE II. Periodic conformance inspection baseline test coverage.

| Inspection                                  | Requirement paragraph | Method paragraph | Sample size | Frequency |
|---------------------------------------------|-----------------------|------------------|-------------|-----------|
| Elongation of copper                        | 3.7.3.2.1             | 4.7.3.2.1        | <u>1</u> /  | Monthly   |
| Tensile strength of copper                  | 3.7.3.2.2             | 4.7.3.2.2        | <u>1</u> /  | Monthly   |
| Purity of copper                            | 3.7.3.2.3             | 4.7.3.2.3        | <u>2</u> /  | Monthly   |
| Lap shear strength                          | 3.7.4.6               | 4.7.4.6          | <u>3</u> /  | Monthly   |
| Rework simulation                           | 3.7.4.7               | 4.7.4.7          | <u>3</u> /  | Monthly   |
| Moisture and insulation resistance          | 3.7.6.1               | 4.7.6.1          | <u>3</u> /  | Monthly   |
| Dielectric withstanding voltage, DC voltage | 3.7.5.2               | 4.7.5.2          | <u>3</u> /  | Monthly   |

1/ A minimum of ten test specimens (five lengthwise and five crosswise) shall be inspected.

2/ A minimum of one test specimen for each copper plating tank shall be inspected.

3/ A minimum of two test specimens shall be inspected.

4.6 Capability verification inspection. Capability verification inspection shall be in accordance with the TRB approved capability verification inspection plan and supplemented with the verifications of table III herein. Unless otherwise specified in the TRB approved capability verification inspection plan, the supplemental verifications listed in table III shall be performed every 2 years. Each base material type qualified shall be verified.

TABLE III. Supplemental capability verification inspection verifications.

| Inspection                             | Requirement paragraph | Method paragraph |
|----------------------------------------|-----------------------|------------------|
| Rework simulation                      | 3.7.4.7               | 4.7.4.7          |
| Solder reflow thermal stress           | 3.7.6.2.2             | 4.7.6.2.2        |
| Thermal shock                          | 3.7.6.3               | 4.7.6.3          |
| Direct current induced thermal cycling | 3.7.6.4               | 4.7.6.4          |

#### 4.7 Methods of inspection.

##### 4.7.1 Visual and dimensional inspection.

4.7.1.1 Visual inspection. The visual features of the printed board specimen shall be inspected in accordance with test method number 2.1.8 of IPC-TM-650, except that the magnification shall be 7x to 10x, minimum. If confirmation of a suspect defect cannot be determined at 10x, it shall be verified at progressively higher magnifications, up to 30x.

4.7.1.2 Dimensional inspection. The dimensional features of the printed board test specimen shall be inspected using test method numbers 2.2.1 and 2.2.2 of IPC-TM-650, as applicable. Unless otherwise specified, the magnifications in table IV shall be used for the conductor width or land diameter/width of features under inspection. Referee inspection needed to confirm a suspected defect of the printed board test specimen features shall be accomplished at a magnification of up to 40x, as applicable to confirm the suspected nonconformance. Dimensions identified as critical shall be measured at 30x to 100x maximum, as applicable. Characteristics not observable through solder mask shall be evaluated prior to its application to the surface of the printed board. Verification of printed wiring board dimensional parameters using automated inspection technology (AOI and AXI) shall be acceptable.

TABLE IV. Inspection magnification.

| Conductor width or land diameter/width   | Magnification <sup>1/</sup> |                    | IPC-OI-645 grade |
|------------------------------------------|-----------------------------|--------------------|------------------|
|                                          | Standard inspection         | Referee inspection |                  |
| Greater than 1.0 mm (.04 inches)         | 1.75x                       | 4x                 | IV and V         |
| From 0.5 to 1.0 mm (.02 to .04 inches)   | 4x                          | 10x                | V and VI         |
| From 0.25 to 0.5 mm (.001 to .02 inches) | 10x                         | 20x                | VI and VII       |
| Less than 0.25 mm (.001 inches)          | 20x                         | 40x                | VII and VIII     |

<sup>1/</sup> Referee conditions are used to verify printed wiring boards rejected at the standard inspection magnification power. For printed wiring board designs with mixed conductor and land diameters and widths, the greater magnification power may be used for the inspection of the entire printed wiring board.

4.7.1.2.1 Board and conductor pattern features. The accuracy of board and conductor pattern features may be verified by performing first piece inspection on a representative first production run part or by sampling the printed boards in the lot. The use of automated inspection technology shall be acceptable.

4.7.1.2.2 Hole pattern accuracy. Unless otherwise specified, only the holes that are specifically dimensioned shall be inspected for hole pattern accuracy to meet printed board dimensional requirements. Unless otherwise specified, the hole pattern accuracy for the nonspecifically dimensioned holes, such as plated through holes and vias, need not be checked as their locations are set by the supplied hole location database and are controlled by external and internal annular ring requirements. Unless otherwise specified, the accuracy of the hole pattern may be verified by using a representative first piece specimen for the lot or by sampling the printed boards in the lot. The use of automated inspection technology shall be acceptable.

4.7.1.2.3 Hole size. The finished hole size tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of measurements needed for each hole size shall be determined by the manufacturer using an adequate sample of holes based on the number of holes within the population.

4.7.1.3 Alternate plating and coating measurement techniques. When a plating or coating thickness is less than 0.00125 mm (.00005 inch), the thickness measurements shall be performed in accordance with one of the following procedures:

- a. [ASTM B567](#) , measurement of thickness by the beta backscatter method.
- b. [ASTM B568](#), measurement of thickness by X-ray spectrometry.

4.7.1.4 Scratch depth. Testing for scratches should be in accordance with test method number [2.1.9 of IPC-TM-650](#). Other suitable electronic means may be used.

4.7.1.5 Wire bond pad surface roughness. The printed board specimen shall be inspected for surface roughness in accordance with test method number [2.4.15 of IPC-TM-650](#). Only the pristine area shall be evaluated.



4.7.2 Destructive physical analysis (DPA) by microsection evaluation of printed board test specimens. Automatic microsectioning techniques may be used in lieu IPC-TM-650 methods specified in 4.7.2.1.

4.7.2.1 Mount preparation. Microsection mount preparation shall be accomplished by using methods in accordance with either numbers 2.1.1 or 2.1.1.2 of IPC-TM-650. The following details shall apply:

- a. Number of holes for each specimen. A minimum of at least three plated-through holes cross sectioned vertically shall be made for each test specimen required.
- b. Accuracy. All plated-through holes of each test specimen in the mount shall be sectioned, ground, and polished to within  $\pm 10$  percent of the center of the drilled diameter of the holes.
- c. Pre-microetch evaluations. The plated-through holes shall be evaluated for plating separations prior to microetching.
- d. When more than two specimens are contained in a mount (coupon-stacking or gang mounting), the following shall apply:
  - (1) The specimens shall not be in direct contact with any other specimen in the mount. The recommended distance between specimens in a mount is 0.25 to 1.57 mm (.010 to .062 inch).
  - (2) An orientation mark or other identification marking shall identify layer one of the first specimen. Also, unless otherwise listed on the mount, traceability identifying all specimens contained in a mount shall be available.

4.7.2.2 Mount examination and inspection. The examination and inspection of microsection mounts to evaluate characteristics such as dielectric spacing, etchback, plating thickness, foil thickness, and other characteristics, in plated-through holes shall be accomplished in accordance with test method number 2.2.5 of IPC-TM-650. Each side of all plated-through holes in the mount shall be viewed independently. The following details shall apply:

- a. Magnifications. The specimens shall be inspected at magnifications specified in test method number 2.2.5 of IPC-TM-650. Referee inspections shall be accomplished at a magnification of twice the recommended magnification.
- b. Evaluations. The plated-through holes shall be evaluated for foil and plating cracks and plating separations both prior to and after microetching the surface of the microsection mount. Pre- and post-microetching evaluations for the criteria of 3.1, 3.3, and 3.6 shall be accomplished at magnifications specified above.
- c. Measurements. Measurements shall be averaged from at least three determinations for each side of the plated-through hole. The copper plating thickness of the plated-through hole wall shall be determined from the average of three measurements, approximately equally spaced, taken on each side of the hole. Isolated thick or thin sections shall not be used for averaging; however, isolated areas of reduced copper thickness shall be measured and evaluated to the copper plating void rejection criteria specified in 3.6.5.
- d. Plating that is less than 0.00125 mm (.00005 inch) in thicknesses shall not be measured using metallographic techniques. See 4.7.1.3 for alternate measurement techniques.

#### 4.7.3 Chemical test methods.

4.7.3.1 Ionic contamination (cleanliness). The printed board specimen shall be inspected for ionic contamination in accordance with test method number [2.3.25 of IPC-TM-650](#).

#### 4.7.3.2 Copper plating tests.

4.7.3.2.1 Elongation of copper. The test for elongation of plated copper shall be performed in accordance with [ASTM E345](#) or test method number [2.4.18.1 of IPC-TM-650](#). The travel speed of testing shall be 50.0 mm  $\pm$ 1.0 mm (1.97  $\pm$ .03 inch) for each minute.

4.7.3.2.2 Tensile strength of copper. The test for tensile strength of plated copper shall be performed in accordance with [ASTM E345](#) or test method number [2.4.18.1 of IPC-TM-650](#). The travel speed of testing shall be 50.0 mm  $\pm$ 1.0 mm (1.97  $\pm$ .03 inch) for each minute. The mean average cross-sectional area shall be determined using the following:

- a. Measure the thickness of the test specimens by use of an optimizer, an electrical type measuring device, or vernier micrometer, provided that the thickness is measured to at least the nearest two percent.
- b. Measure the test specimen width dimension to the nearest 0.025 mm (.001 inch).
- c. The mean average test specimen cross-sectional area shall equal the average thickness multiplied by the average width.

4.7.3.2.3 Purity of copper. The test for purity of plated copper shall be performed in accordance with [ASTM E53](#) or test method number [2.3.15 of IPC-TM-650](#).

#### 4.7.4 Physical test methods.

4.7.4.1 Adhesion, marking. Test specimens which represent all types of marking used on the lot (except etched marking) shall be subjected to the solderability test in [4.7.4.5.1](#). The side of the test specimen that is marked shall be placed against the solder. After the test, the test specimen shall be examined in accordance with [4.7.1](#) and the requirements of [3.7.4.1](#) shall be met.

4.7.4.2 Adhesion, plating. The test for plating adhesion shall be performed in accordance with test method number [2.4.1 of IPC-TM-650](#). If overhanging metal breaks off and adheres to the tape, it is evidence of outgrowth, overhang, or slivers, but not of plating adhesion failure.

4.7.4.3 Adhesion, solder mask. The test for solder mask adhesion shall be performed in accordance with test method number [2.4.28.1 of IPC-TM-650](#).

4.7.4.4 Bow and twist. The tests for bow and twist shall be performed in accordance with test method number [2.4.22 of IPC-TM-650](#).

#### 4.7.4.5 Component attachment.

4.7.4.5.1 Solderability. The tests for hole or surface solderability shall be performed in accordance with [J-STD-003](#) or the SERA test described in appendix G of [MIL-PRF-31032](#). Unless otherwise specified (see [3.1](#)), the tests of [J-STD-003](#) that used Sn-Pb solders (A, B, C, or D) shall be used. The default category of coating durability of [J-STD-003](#) is category 2. When required by the procurement documentation, accelerated conditioning for coating durability shall be in accordance with [J-STD-003](#).

NOTE: Printed board designs that do not require soldering to attach components (as in the case where press-fit components or wire bonding are used) do not require solderability testing. Printed boards that require soldering during assembly processes require solderability testing. Printed boards using only surface mount component do not require hole solderability testing.

4.7.4.5.2 Wire bond pull strength. The test for wire bond pull strength shall be performed in accordance with test method number 2.4.42.3 of IPC-TM-650.

4.7.4.6 Lap shear strength (for designs with metal backing material). The tests for lap shear strength shall be performed in accordance with ASTM D3165 with a testing temperature of 25 degrees C  $\pm$ 5 degrees C. The printed board test specimens shall be a minimum of 25.0 mm (.98 inch) wide with a 13.0 mm (.51 inch) lap overlay.

4.7.4.7 Rework simulation.

4.7.4.7.1 Single and double sided without plated holes. The rework simulation test shall be performed in accordance with test method number 2.4.21 of IPC-TM-650.

4.7.4.7.2 Double sided with plated holes. The rework simulation test shall be performed in accordance with test method number 2.4.36 of IPC-TM-650.

4.7.5 Electrical test methods.

4.7.5.1 Continuity and isolation.

4.7.5.1.1 Production screening. Printed boards shall be electrical tested using either automatic or manual equipment capable of verifying the level B requirements of IPC-9252 for 100 percent continuity and isolation.

4.7.5.1.2 Qualification and referee testing.

4.7.5.1.2.1 Continuity. A current shall be passed through each conductor or group of interconnected conductors by applying electrodes on the terminals at each end of the conductor or group of conductors. The current passed through the conductors shall not exceed those specified in the applicable design standard for the smallest conductor in the circuit.

4.7.5.1.2.2 Isolation (circuit shorts). A test voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The test voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer. For manual testing the test voltage shall be 200 volts minimum and shall be applied for a minimum of 5 seconds. When automated test equipment is used, the minimum applied test voltage shall be the maximum rated voltage specified. If the maximum rated voltage on the printed board is not specified, or is less than 40 volts, the test voltage shall be 40 volts minimum.

4.7.5.2 Dielectric withstanding voltage.

4.7.5.2.1 DC voltage, after MIR (atmospheric pressure). The printed wiring board test specimen shall be tested in accordance with test condition B of test method number 2.5.7 of IPC-TM-650. The following details and exceptions apply:

- a. Test specimen: The test specimen shall be as identified in table II and shall be subjected to the moisture and insulation resistance test.
- b. Points of application: The dielectric withstanding voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.
- c. Examination after test: During the tests, the leakage current shall be monitored and the test specimens examined for evidence of arcing and breakdown. At the conclusion of the test, test specimens shall be examined for evidence of damage.

4.7.6 Environmental test methods.

4.7.6.1 Moisture and insulation resistance. The test for moisture and insulation resistance shall be performed in accordance with class 3 of test method number [2.6.3 of IPC-TM-650](#) using either specimen preparation method (A or B). The initial and final insulation resistance shall be greater than or equal to 500M ohm when measured at 500 volts (+10, -0 percent) DC.

4.7.6.2 Resistance to soldering heat.

4.7.6.2.1 Solder float thermal stress. The test for solder float thermal stress shall be performed in accordance with condition C of appendix F of [MIL-PRF-31032](#).

4.7.6.2.2 Solder reflow thermal stress. The test for solder reflow resistance to soldering heat shall be performed in accordance with condition D or H of appendix F of [MIL-PRF-31032](#).

4.7.6.3 Thermal shock. The printed wiring board test specimen shall be tested in accordance with test method number [2.6.7 of IPC-TM-650](#), with the following details:

- a. Test specimen: The test specimen shall be either a suitable test specimen designed for the test or a portion of the production printed board.
- c. Test condition: Unless otherwise specified, test condition B shall be used.
- b. Maximum change in resistance: 10 percent.

4.7.6.4 Direct current induced thermal cycling. The test for direct current induced thermal cycling shall be performed in accordance with test method number [2.6.26 of IPC-TM-650](#).

4.7.7 Optional verifications.

4.7.7.1 Optional visual verifications.

4.7.7.1.1 Visual and mechanical inspection. Unless otherwise specified, printed board specimens shall be examined under 30x to 60x magnification. In case of conflict, 30x will be the referee power, unless otherwise specified, to verify that the materials, design, construction, physical dimensions, and workmanship are in accordance with the applicable requirements (see [3.1](#), [3.4](#), [3.5](#), [3.5.1](#) through [3.5.4.6](#) inclusive, and [3.9](#)).

4.7.7.1.2 Surface examination of conductors. The conductors of the printed board specimen shall be inspected for workmanship in accordance with test method number [2.1.5 of IPC-TM-650](#).

4.7.7.1.3 Laser marking legibility test. Printed board specimens shall be coated with 0.13 mm (.005 inch) minimum of silicon resin insulating compound, type SR in accordance with [IPC-CC-830](#). After curing, coated printed board specimens shall be examined for legibility under normal production room lighting by an inspector at 10x magnification.

4.7.7.1.4 Tin-lead plating thickness. Tin-lead plate test coupons shall be removed from the production panel prior to fusing to verify plating thickness. Alternate measuring techniques of [4.7.1.3](#) may be used.

4.7.7.2 Optional dimensional verifications.

4.7.7.2.1 Hole size, drilled. The measurement for drilled hole size shall be in accordance with test method number [2.2.6 of IPC-TM-650](#). Finished hole size tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of measurements for each hole size shall be documented in the QM plan, determined by the TRB to adequately sample the quantity of holes within the population.

4.7.7.2.2 Hole size, plated. The measurement for plated hole size shall be in accordance with test method number [2.2.7 of IPC-TM-650](#). Finished hole size tolerance shall be verified on a sample basis across all hole sizes applicable to the design. The number of measurements for each hole size shall be documented in the QM plan, determined by the TRB to adequately sample the quantity of holes within the population.

4.7.7.3 Optional chemical verifications.

4.7.7.3.1 Organic contamination. The measurement for organic contamination shall be in accordance with test method numbers [2.3.38 and 2.3.39 of IPC-TM-650](#). If evidence of organic contamination is detected by test method [2.3.38](#) of IPC-TM-650, then test method number [2.3.39](#) of IPC-TM-650 shall be used to determine the nature of the contaminant.

4.7.7.3.2 Resistance to solvents (marking ink or paint). Marking ink or paint resistance to solvents shall be tested in accordance with test method number [2.3.4 of IPC-TM-650](#). The following details apply:

- a. The marked portion of the test specimen shall be brushed.
- b. After the test, the test specimen shall be visually inspected in accordance with [4.7.1](#) for legibility of marking and the requirements of [3.7.7.3.2](#).

4.7.7.4 Optional physical verifications.

4.7.7.4.1 Coefficient of thermal expansion (CTE). The test for CTE shall be performed in accordance with test method number [2.4.41.2 of IPC-TM-650](#).

4.7.7.4.2 Die to die pad shear strength. The test for die to die pad shear strength shall be performed in accordance with test method number [2.4.42.2 of IPC-TM-650](#).

4.7.7.5 Optional electrical verifications.

4.7.7.5.1 Impedance testing. Impedance testing shall address the parameters required by the level C requirements of [IPC-9252](#).

4.7.7.5.2 Characteristic impedance of conductors. When specified in the applicable printed board procurement documentation, perform characteristic impedance testing for conductors in accordance with test method number [2.5.5.7 of IPC-TM-650](#). The characteristic impedance shall meet the requirements specified in the applicable printed board procurement documentation.

4.7.7.5.3 Dielectric withstanding voltage.

4.7.7.5.3.1 AC voltage (hi-pot). When specified, the printed wiring board test specimen shall be tested in accordance with test method number 2.5.7 of IPC-TM-650. The following details and exceptions apply:

- a. Test specimen: The test specimen shall be the production printed board.
- b. Specimen preparation: Unless otherwise specified, the production printed boards shall not be prepared in accordance with the test method.
- c. Magnitude of test voltage: The maximum voltage, rate of voltage rise per second, and when applicable, leakage current shall be as specified.
- d. Nature of potential: Alternating current.
- e. Duration of application of specified test voltage: Unless otherwise specified, a minimum duration of 5 seconds for quality conformance inspection, 1 minute for qualification inspection.
- f. Points of application: Unless otherwise specified, the specified voltage shall be applied between all common portions of each conductor pattern and all adjacent common portions of each conductor pattern. The voltage shall be applied between conductor patterns of each layer and the electrically isolated pattern of each adjacent layer.

4.7.7.5.3.2 DC (reduced barometric pressure). Printed board test specimens shall be tested in accordance with method 105 of MIL-STD-202. The following details and exceptions shall apply:

- a. Method of mounting: As used in 4.7.5.2.1.
- b. Test condition: G.
- c. Period of time at reduced pressure prior to application of potential: One minute.
- d. Tests during subjection to reduced pressure: A potential of 500 volts shall be applied for one minute.
- e. Points of application: As specified in 4.7.5.2.1.b.
- f. Examination and measurement: As specified in 4.7.5.2.1.b.

4.7.7.5.4 Surface insulation resistance (as received). The printed wiring board test specimen shall be tested in accordance with test method number 2.6.3.5 of IPC-TM-650. The following details and exceptions apply:

- a. Sample preparation. Test coupons or production printed boards should be conditioned at 50 ±5 degrees Celsius with no added humidity for a period of 24 hours.
- b. Test routine. After cooling, the insulation resistance test shall be performed in accordance with the ambient temperature measurements specified in test condition B of test method number 2.6.3 of IPC-TM-650.

#### 4.7.7.6 Optional environmental verifications.

4.7.7.6.1 Accelerated moisture resistance. The accelerated moisture resistance testing of printed board test specimens shall be performed in accordance with test condition C of [JESD22-A102](#). Test exposure times shall be 96 hours. Final measurements shall be made at room temperature.

4.7.7.6.2 Fungus resistance. The test for fungus resistance shall be performed in accordance with test method number [2.6.1 of IPC-TM-650](#).

4.7.7.6.3 Mechanical shock. The test for mechanical shock shall be performed in accordance with test method number [2.6.5 of IPC-TM-650](#). The following details and exceptions shall apply:

- a. Test specimen: The test specimen shall test coupons or production printed boards as specified.
- b. Method of mounting: The test specimens shall be restrained from movement as specified. If not specified, the test specimen shall be secured on all four corners to a rigid fixture.
- c. Number and direction of blows: The test specimens shall be subjected to three blows in each of the three mutually perpendicular axes.
- d. Shock pulse waveform: The shock pulse shall be 100Gs with a duration of 6.5 ms for each pulse.
- e. Measurements: Unless otherwise specified after the test, the test specimen shall comply with [3.7.5](#).

4.7.7.6.4 Outgassing. The determination of the maximum TML and VCM from the original specimen mass shall be tested in accordance with test method number [2.6.4 of IPC-TM-650](#) or [ASTM E595](#). Test specimens shall be approximately 1 cubic cm in volume. The test specimens shall be placed in a vacuum chamber capable of achieving  $7 \times 10E-3$  Pa for 24 hours.

4.7.7.6.5 Radiation hardness. The test specimen shall be exposed to gamma ray irradiation by using cobalt 60 at a rate of  $0.5 \times 10E4$  Gray to  $1 \times 10E4$  Gray for each hour until the total dose amounts to  $1 \times 10E4$  Gray. After the irradiation, the test specimen shall be inspected visually to verify that there is no degradation in any portion of the test specimen. After the exposure, the tests of moisture insulation resistance and dielectric withstanding voltage shall be performed in accordance with [4.7.6.1](#) and [4.7.5.2](#), respectively. The insulation resistance shall be measured using the same circuit pattern used for the dielectric withstanding voltage test.

4.7.7.6.6 Vibration. Printed board test specimens shall be tested in accordance with [4.7.7.6.6.1](#) or [4.7.7.6.6.2](#) as specified. The following details and exceptions shall apply:

- a. Test specimen: The test specimen shall test coupons or production printed boards as specified.
- b. Method of mounting: The test specimens shall be restrained from movement as specified or, if not specified, secured on all four corners to a rigid fixture. These fixtures shall be constructed in a manner to insure that the points of the test specimen mounting supports will have the same motion as the vibration test table. The fixtures shall also be of a construction that will preclude any resonance in the fixture when subjected to vibration within the test frequency range, and the fixture shall be monitored for these features on the vibration table. Test leads used during this test shall be no larger than AWG size 22 stranded wire, so that the influence of the test lead on the test specimens will be held to a minimum. The test lead length shall be no greater than is necessary. A shielded cable, which may be necessary because of the field surrounding the vibration table, shall be clamped to the test specimens mounting jig.
- c. Direction of motion: Three mutually perpendicular directions (unless otherwise specified, see [3.1](#)).

- d. Electrical load conditions: The electrical load shall consist of the monitor circuit only.
- e. Measurements during vibration: Each test specimen shall be monitored to determine electrical discontinuity by a method which shall at least be sensitive enough to monitor or register, automatically, any electrical discontinuity of 0.1 ms or greater duration.
- f. Measurements after vibration: Continuity shall be measured as specified in 4.7.5.1.2.1.
- g. Examination after test: Unless otherwise specified, after the test the test specimen shall show no evidence of mechanical damage or delamination.

4.7.7.6.6.1 High frequency. The printed board test specimen shall be tested in accordance with test method 204 of MIL-STD-202, test condition D (10 Hz to 2,000 Hz, 20 G).

4.7.7.6.6.2 Random. The printed board test specimen shall be tested in accordance with test method 214 of MIL-STD-202, test condition II, letter G (27.8 G), for 15 minutes. Output to be measured at the geometric center of the test coupon or production board.

## 5. PACKAGING

5.1 Packaging. For acquisition purposes, the packaging requirements shall be as specified in the contract or order (see 6.2). When packaging of materiel is to be performed by DoD or in-house contractor personnel, these personnel need to contact the responsible packaging activity to ascertain packaging requirements. Packaging requirements are maintained by the Inventory Control Point's packaging activities within the Military Service or Defense Agency, or within the Military Service's system commands. Packaging data retrieval is available from the managing Military Department's or Defense Agency's automated packaging files, CD-ROM products, or by contacting the responsible packaging activity.

## 6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Intended use. This specification sheet was developed for the use of verifying the performance of homogenous thermoplastic resin base materials (primarily polytetrafluoroethylene resins) printed boards of single or double sided conductor layers. The printed boards will use soldering for component mounting and may or may not have plated-through holes or metal backing materials. Printed boards of other base material types or construction styles can be tested or verified to the performance requirements contained in this document; however, the performance parameters of other MIL-PRF-31032 performance specifications sheets may be more suited for verifying those designs.

6.2 Acquisition requirements. Acquisition documents should specify the following:

- a. Title, number, revision letter, and date of this specification.
- b. The specific issues of individual documents referenced (see section 2).
- c. Title, number, and date of applicable printed board procurement documentation or drawing. Identification of the originating design activity and, if applicable, the Government approved deviation list for the printed board procurement documentation or drawing.
- d. The complete product procurement documentation part or identifying number (see 3.1).
- e. The printed wiring board classification (type 1 or 2, see 1.2.1 and 3.1), composition (H or B see 1.2.2 and 3.1), and wrap plating grade (A, B, or C see 1.2.3 and 3.1).



- f. Title, number, revision letter (with amendment number when applicable), and date of the applicable design standard with performance classification.
- g. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the product inspection lot to be supplied with each shipment by the QML manufacturer, if applicable.
- h. Requirements for certificate of compliance, if applicable.
- i. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.
- j. Packaging (see 5.1).
- k. If special or additional identification marking is required (see 3.8).

6.2.1 Optional acquisition data. The following items are optional and are only applicable when specified in the printed board procurement documentation.

- a. If any special or additional ionic contamination testing is required (see 3.7.3.1.2).
- b. The durability of coating rating (accelerated aging for solderability testing) if other than category 2 (see J-STD-003).
- c. Requirements for failure analysis, corrective action, and reporting of results.
- d. Disposition of lot conformance inspection sample units.
- e. Any other special requirements.

6.3 Qualification. With respect to products requiring qualification, awards will be made only for products which are, at the time of award of contract, qualified for inclusion in Qualified Manufacturers List (QML-31032) whether or not such products have actually been so listed by that date. The attention of the contractors is called to these requirements, and manufacturers are urged to arrange to have the products that they propose to offer to the Federal Government tested for qualification in order that they may be eligible to be awarded contracts or orders for the products covered by this specification. Information pertaining to qualification of products may be obtained from DLA Land and Maritime, ATTN: VQE, P.O. Box 3990, Columbus, OH 43218-3990 or e-mail [5998.Qualifications@dla.mil](mailto:5998.Qualifications@dla.mil), or at Universal Resource Locator (URL) [http://www.landandmaritime.dla.mil/offices/sourcing\\_and\\_qualification/Offices](http://www.landandmaritime.dla.mil/offices/sourcing_and_qualification/Offices). An online listing of products qualified to this specification may be found in the Qualified Products Database (QPD) at <http://assist.dla.mil>.

6.4 Replacement information. This specification sheet includes a majority of the performance requirements of previous revisions of MIL-P-55110 and MIL-PRF-55110 for types 1 and 2 printed wiring boards constructed using woven glass reinforced polytetrafluoroethylene resin base material (legacy types GR, GT, GX, and GY) and other types of thermoplastic base materials. Printed wiring boards conforming to this specification sheet would be comparable to printed wiring boards conforming to MIL-P-55110 or MIL-PRF-55110.

6.5 Composition.

6.5.1 Thermoplastic resin base materials. A base material that resin system is based on a plastic that can be repeatedly softened and reshaped, without any significant change in inherent properties, by exposure to heat and hardened by cooling.

6.5.2 Metal backed printed boards. A double-sided printed wiring board design that includes a metal support that functions as both a heat sink and a ground plane.

6.6 Tin finishes (see 3.4.1). The use of alloys with tin content greater than 97 percent may exhibit tin whisker growth problems after manufacture. Tin whiskers may occur anytime from a day to years after manufacture, and can develop under typical operating conditions on products that use such materials. Tin whisker growth could adversely affect the operation of electronic equipment systems. Conformal coatings applied over top of a whisker-prone surface will not prevent the formation of tin whiskers. Alloys of three percent lead have shown to inhibit the growth of tin whiskers. For additional information on this matter refer to ASTM B545.

6.7 Supporting documents. The documents in this section may be used as guidelines for the development of a capability verification inspection program and are not mandatory for this specification sheet.

DEPARTMENT OF DEFENSE SPECIFICATIONS

MIL-HDBK-1547 – Electronic Parts, Materials, and Processes for Space and Launch Vehicles.

(Copies of these documents are available online at <https://assist.dla.mil/quicksearch> or <https://assist.dla.mil> or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

6.8 Changes from previous issue. The margins of this specification are marked with vertical lines to indicate where modifications generated by this amendment were made. This was done as a convenience only and the Government assumes no liability whatsoever for any inaccuracies in these notations. Bidders and contractors are cautioned to evaluate the requirements of this document based on the entire content irrespective of the marginal notations.

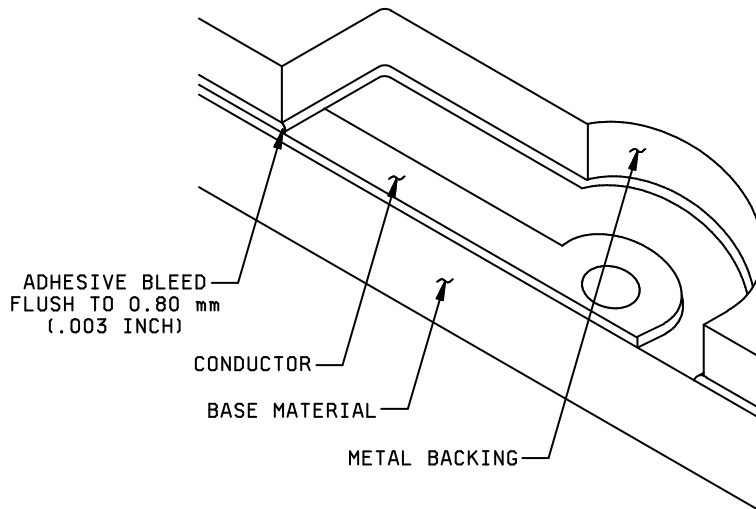


FIGURE 1. Adhesive bleed near conductor.

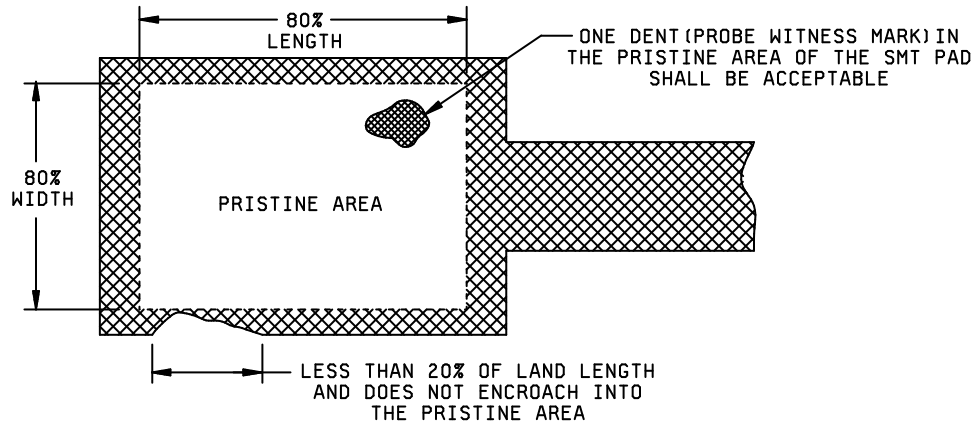


FIGURE 2. Rectangular surface mount lands.

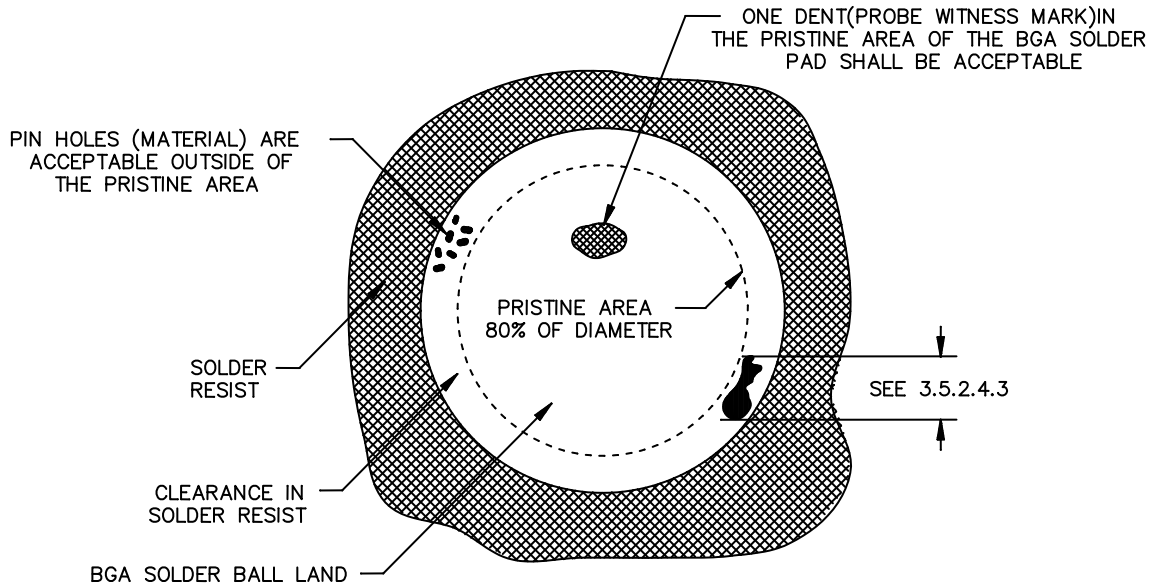


FIGURE 3. Round surface mount lands (BGA pads).

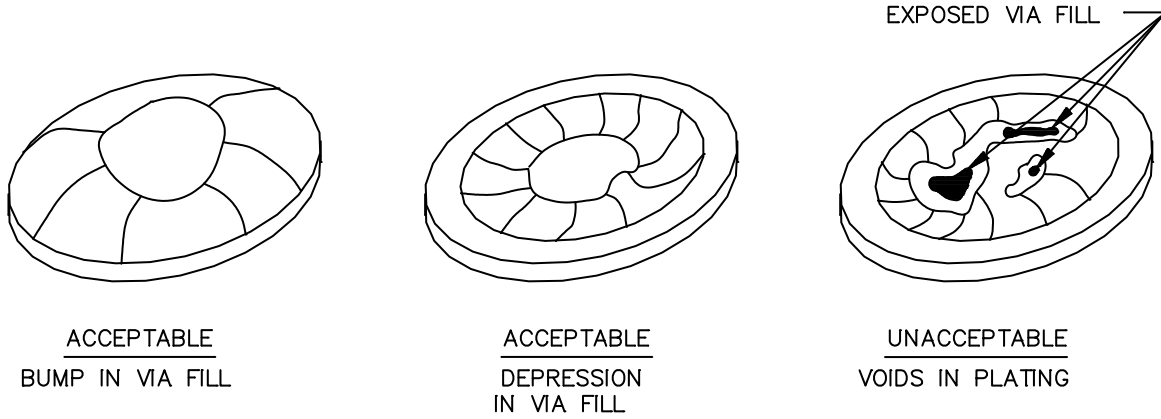


FIGURE 4. Via copper cap plating deviations.

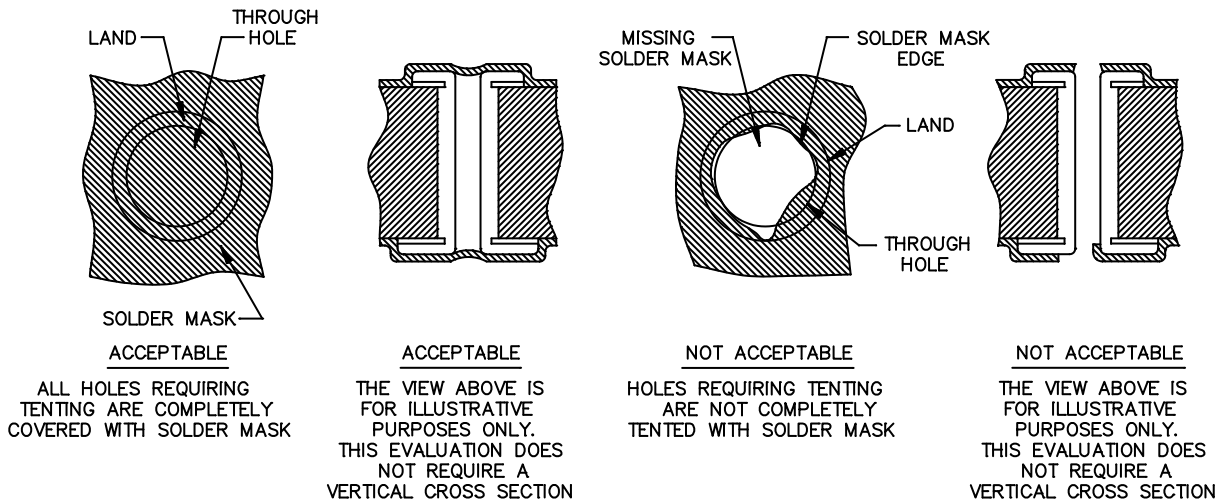
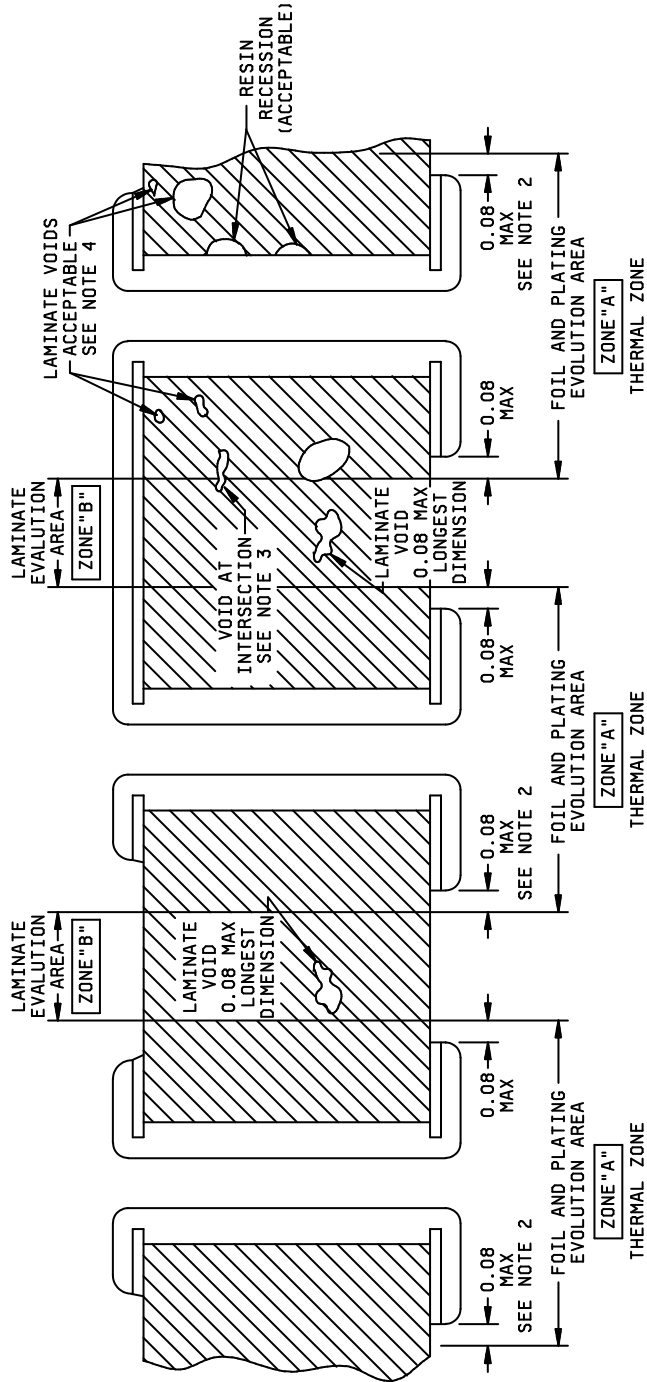


FIGURE 5. Solder mask tenting deviations.



NOTES:

1. Dimensions are in millimeters.
2. Typically beyond land edge most radially extended.
3. Voids at intersection of zone A and zone B. Laminate voids greater than 0.08 mm (.003 inch) that extend into zone B are rejectable.
4. Laminate voids are not evaluated in zone A.

FIGURE 6. Plated hole structural requirements, homogenous construction (via microsection).

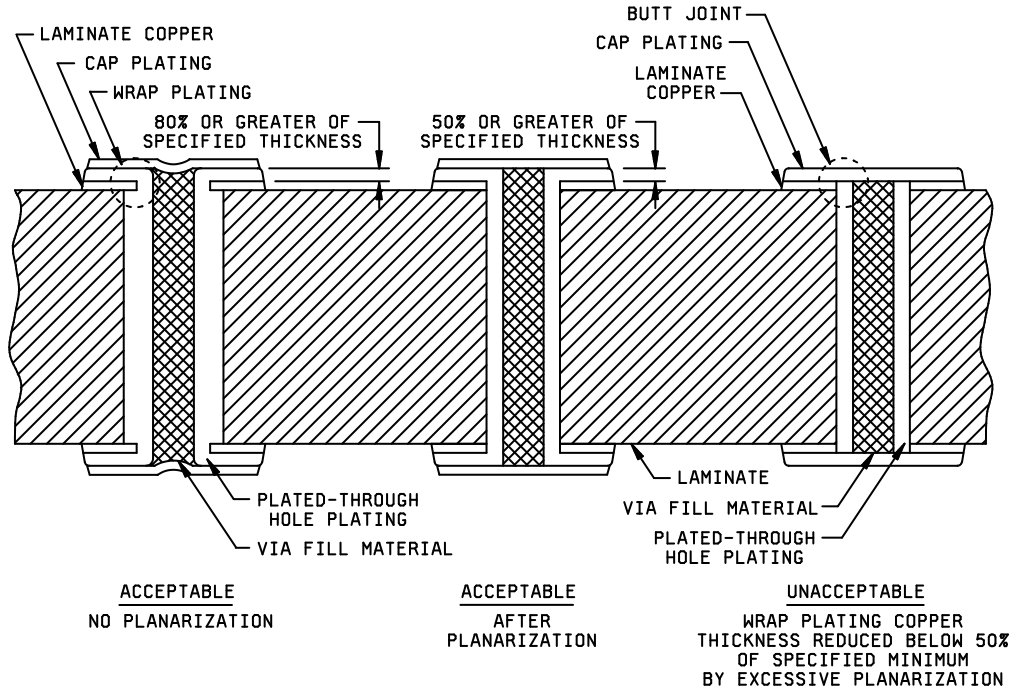


FIGURE 7. Plated-through hole wrap plating (continuous hole-knee-surface copper plating).

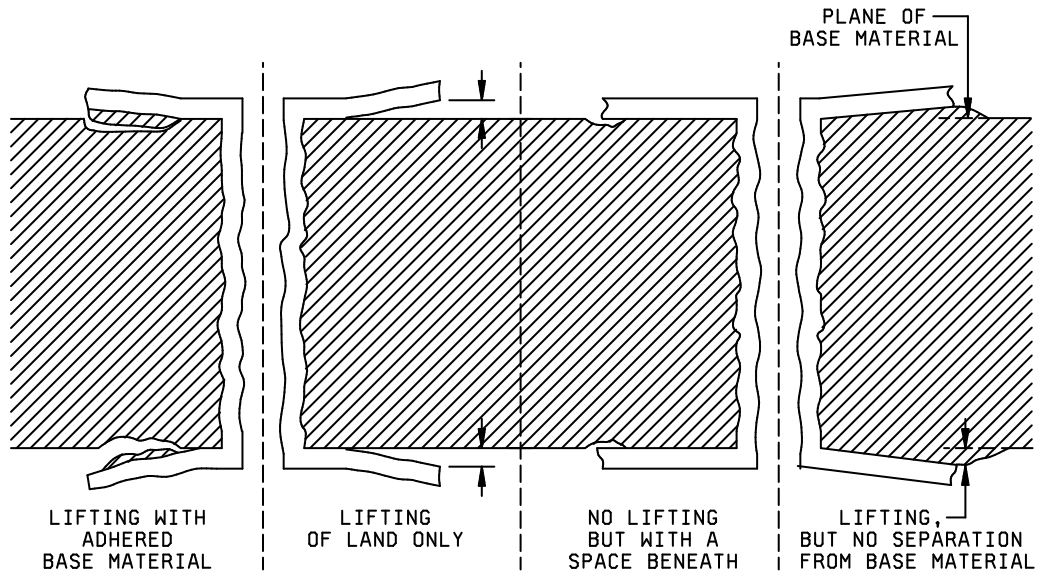


FIGURE 8. Lifted lands.

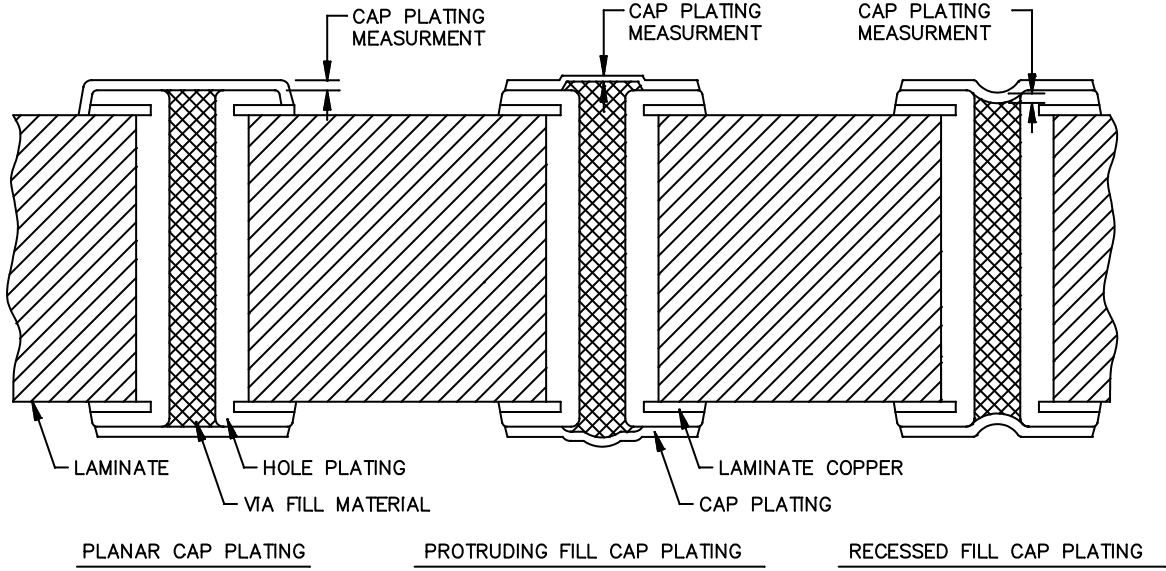


FIGURE 9. Acceptable via cap plating.

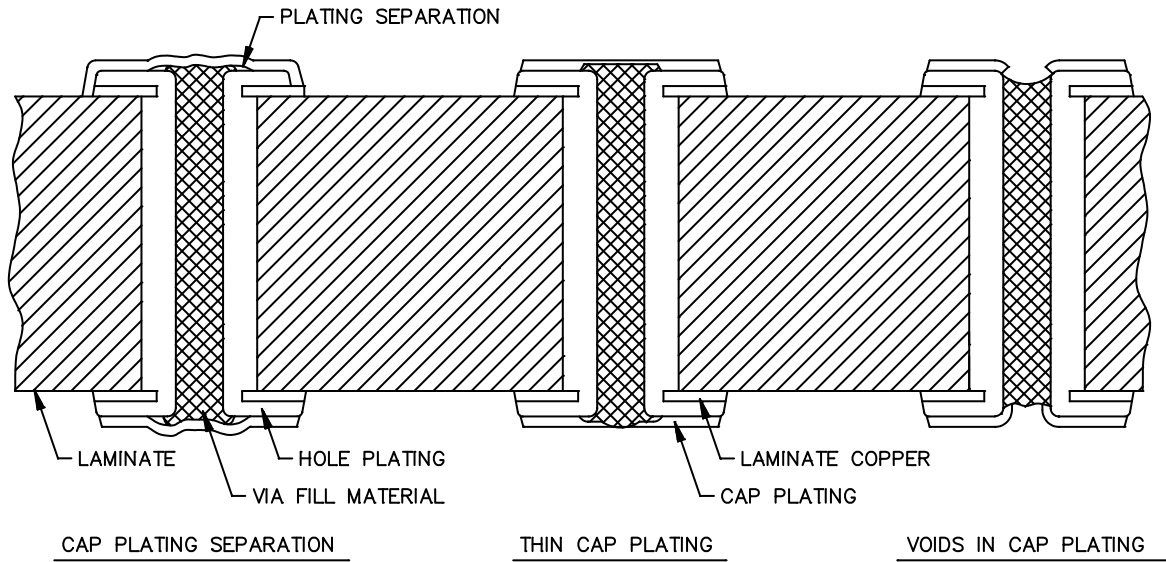


FIGURE 10. Unacceptable via cap plating.

Custodians:  
Army – CR  
Navy – EC  
Air Force – 85  
DLA – CC

Preparing activity:  
DLA – CC

Project: 5998-2012-066

Review activities:  
Army – MI  
Air Force – 99

NOTE: The activities listed above were interested in this document as of the date of this document. Since organizations and responsibilities can change, you should verify the currency of the information above using the ASSIST Online database at <https://assist.dla.mil>.