A block level description of

AgFo

Ver 1.0

RAMAN RESEARCH INSTITUTE B A N G A L O R E 560080 I N D I A

* ERNI ZD and FRC connectors

Certain number of LV only, GC, Clock compatible (CC), SM cum LV compatible signals from different FPGA banksare available in the **FRC** and **ERNI** connectors. The table-1 below catagorically lists this distribution.

J#	#LV	#CC	CC-SM	SM	#GC	Bank#s
14	5	1	2	4	-	13
15	5	-	-	7	-	13,11
16	12	-	-	-	-	11,15
17	6	4	-	-	-	15
18	8	4	-	-	-	17
19	8	-	-	-	4	17,**4**

TABLE-1

note:
- J# corresponds to the connector number in the AgFo ver1.0 schematics.
- FRC J14,18,and 19 signals are also available in **ERNI J35**
- FRC J15,16,and 17 - do - in **ERNI J36**
- All GC,CC,SM also work as LV.
- (avoid J14..19, to get best speed performance through ERNI J35,36)
- J35 gets 40 pairs, J36 gets only 35 pairs from FPGA
- Use FRC path for slow rates (tested upto 31+MHz, may work to 60+)
- One of the FRC J17 gets only 10 pairs.
- FRC path was used for the X2 DAS interface.
- It can be noticed that, in the AgFo Ver1.0, pcb tracks connecting J35, J36 with FPGA runs toching the pads of J14 to J19 and further optimization possible.

12-LEDs

- Twelve LEDs arranged in the form of a Circular layout. These are for displaying any diagnostic signals from the FPGA (for eg, LED-1,2,.. can blink to show channel-1,2.. activities and so on). The LED layout is arranged in a way that the LED number can be easily comphrehended from its position in the CLOCK Face like layout.
- These LEDs are connected/powered from the BANK-2. The 3.3V supply for this bank comes from LDO U14.
- If an output pin goes high an LED will light-up,.
- It is a good practice to drive the LEDs with very low drive strength from the FPGA to avoid unnecessary ground bounces.
- FPGA Pins used are: LED-1 to 12 are pins W16, Y16, AA14, AA13, AA17, Y17, AA18, Y18 respectively.

XII
12-LEDs display diagnostics signals
IX III
VI

EXTRNAL CLOCKS

- **SMA J4** allows LVTTL/LVCMOS3.3V clocks to be fed to the AgFo from an external source. This clock will reach FPGA at Pin AF12,AE12 of BANK-18 after being converted to LVDS in the U12 BUFFER chip
- **SMA J10** and **J34** allows LVDS clocks to be fed to the FPGA from an external source. This differntial signal reach the FPGA at pinsAB7, AB6 of BANK-18

J10 J34

EXTERNAL CLOCKS

J4

8-Berg-stick pins aid monitoring signals

12

XTAL OSC 125.0000 MHz

XTAL OSC

- A CRYSTAL Oscillator of 125.0000 MHz Provides the basic clock rference required for the 2.5Gbps MGT operation and 1.25Gbps for the Gigabit Ethernet.
- The Jumper J23 allows 3.3Volt as well as 2.5Volt Crystal oscillators to be used

BUFFERS

BUFFERS U12

- mgtck1, mgtck2 from the XTAL clock buffer feeds MGT_112, (clock pins K3,K4) MGT_114 (clock pins T3,T4) respectively.
- mgtck3 from the XTAL clock buffer feeds MGT_116 clock pins (D3,D4)
- mgtck3 also goes to FPGA BANK-16 pins E5,D5.
- Single ended clock from SMA J4 is buffered and and fed to
- FPGA BANK-18 pins AF12,AE12

FIBER INTERFACE

- Four **FINISAR make SFF are used (F1, F2, F3, F4)**
- Part Number: **FTRJ1421SMCL** *(Jamie/Mark Leach)*
- Two of the four SFFs (F1,F2) connects to MGT_112, third (F3) to MGT114 and the fouth (F4) connects to MGT_116. The receiver of the third SFF (F3) is routed through a SCAN (a flexible) switch to facilitate driving the Clock/Timing signals that enters the SFF F3 to an external device/clock-system through SMA pairs J5,J6.
- Although all SFFs can drive up to 2.67Gbps bidirectional The F3 SFF reception can't exceed 1.5Gbps, since the SCAN switch is rated upto 1.5Gbps rate.
- No DC blocking capacitors are required as they are built in to the SFF device.
- Uses 1310 nm laser transmitter
  -transmission 1270 nm. to a max. of 1360 nm. (-20dB spectral width: 1nm.)
  -reception 1270nm to 1600 nm.
- Average receiver sensitivity at 2.67Gb/s -18 dBm.
- Pout: -5 to 0 dBm
- Can drive 9/125um SMF to 20Km/30Km
- Analog Diagnostic Functions
- <700mW power dissipation
- Compatible with Gigabit Ethernet
- Transmitter and Receivers are powered from independent LDOs
- A 3.3V supply for the transmitter Tvcc is derived from the LDO TPS74401/TPS74201 (U9).
- A 3.3V supply for the receiver Rvcc is derived from another LDO TPS74201 (U8).

Backplane 40x2 **ERNI ZD** x 2 connectors* J35, J36

(OR) 70 pairs Onboard **FRC connectors*** (12x2 x 6*) J14 to 19

75 pairs of diff. signals

LV1..43, 45, 47..72, 76..90

107 pairs

8

3.3V I/O Banks

VIRTEX-5 FPGA

2.5V I/O Banks

4 pairs

3 pairs

MGTs with 125MHz reference clock

2.67Gbps bidirectional FIBER INTERFACE x 4*

FINISAR SFF

1 pair

SWITCH (1.5Gbps) routes the CLOCK

1 pair

MGTs with external reference clock

3 pairs

SMA pairs x 8

RJ45 CAT5e connectors**
4 pairs x 1 port x 1,
4 pairs x 4 port x 2
J1,2,3

32 pairs of diff. signals

fda1..8, fdb1..8, fds1..8, fck1..8, gc8..11

CONFIG DONE LED

3.3V I/O Banks

DXP, DXN

8

USB card*** Interface for configuration and control

Slave Serial for configuration

MODE/JTAG for configuration

Temperature Monitor/FAN control

SWITCH

- **A flexible SWITCH SCAN90CP02** (U11) is used to route the third SFF (F3) receiver outputs
- The SCAN takes in two pairs of diffrential inputs
  i) from the third SFF (F3, pins 9, 8) receiver outputs and the
  ii) FPGA LV output "fcko" pair (FPGA pins D11, C11)
  and switch these inputs to an SMA pairs (J5, J6) and to the MGT_114 MGTRX0 (FPGA pins T1, R1).
- The various switch options can be controlled by hardwiring a Jumper available at J31, located close to the RJ connector J3.
- The SCAN also supports pre-emphasis and is controlled by setting the Jumper J30. This feature will be useful if the clock/timing signals to go a long way out through the SMAs (J5. J6).

8-Berg-stick Pins of J12

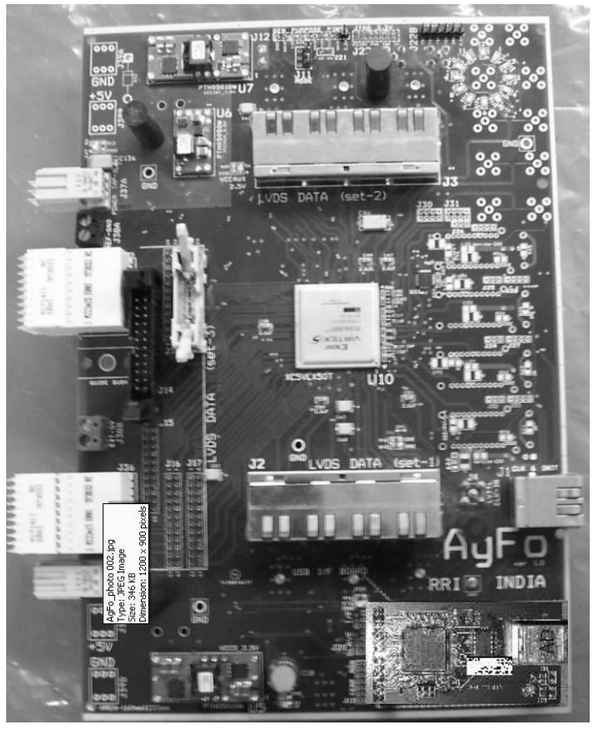
- Eight berg-sick pins are provided in J12 to aid monitoring any sinal being probed. These will be useful during code development/debugging. These lines come from BANK-2, which has the 3.3V I/O and is powered by LDO U14.
- PINS 2 to 9 of J12 are used, they come from FPGA pins: AA10, Y11, Y12, AA12, Y13, W14, Y15, AA15, respectively.
- J12 is located at the Upper edge, adjacent to the JTAG ports

CONFIG DONE LED

- This LED (D1) comes ON, when the FPGA gets booted.
- This LED is located in the component side just above the J20 SLAVE_SERIAL jumper/and beside the USB inteface port area.

SMA Pairs

The spare MGTs, ie., one port of MGT_116 and both ports of MGT_118 are routed to SMA pairs.
- **SMA pair J49.J50 forms MGTTX1_116** and the signals are coupled through 0.01uF capacitors (C135,C137)
- **SMA pair J51,J52 forms MGTRX1_116** and the signals are coupled through 0.01uF capacitors (C138,C139) and 100ohm parallel termination (R86).
- **SMA pair J47.J48 feeds clock to MGTTX0_118** through 0.01uF capacitors (C141,C140)
- **SMA pair J43,J44 forms MGTTX0_118** and the signals are coupled through 0.01uF capacitors (C149,C148)
- **SMA pair J45,J46 forms MGTRX0_118** and the signals are coupled through 0.01uF capacitors (C143,C142) and 100ohm parallel termination (R87).
- **SMA pair J53,J54 forms MGTTX1_118** and the signals are NOT coupled through capacitors to facilitate loop-back tests with one of the RX say, MGTRX1_118.
- **SMA pair J55,J56 forms MGTRX1_118** and the signals are coupled through 0.01uF capacitors (C144,C145) and 100ohm parallel termination (R88).
- 0402 (EIA) package 0.01uF is suitable for 3.125Gbps transmission with 8B//10B coding



** RJ45 connectors

Details about LV, CC, and GCs available in each of the RJ connectors, ie., J1 to 3 and corresponding FPGA banks used are listed below in TABLE-2:

J#	#LV	#CC	#GC	Bank#s
1	2	-	2	**3**, 16
2-port1	2	1	1	16, **3**
2-port2	2	1	1	16, **3**
2-port3	1	2	1	16, **3**
2-port4	3	-	1	16, **3**
3-port1	3	-	1	18, **4**
3-port2	2	1	1	18, **4**
3-port3	2	1	1	18, **4**
3-port4	3	-	1	18, **4**

TABLE-2

note:
- J1,2, 3 tracks are routed/adjusted for maintaining 100ohms differential Impedance.
- J1 can bring in/out LVDS Clock, TIMING signals
- J2 and J3 were used for interfacing to ADFB during the X2

USB CARD Interface

*** **Design provided by Joseph**
- USB card connects to J8 and J9 of ver 1.0 AgFo PCB only through an adaptor/jumper board. This is required to circumvent a J8/J9 placement error in the AgFo ver 1.0 board.
- The USB board takes power provided through J9
- BANK-1 connects to this port for USB based I/O (3.3V LVTTL)
- BANK-0 Slave-serial signals connects with this port through J8
- The 3.3V power for this section comes from LDO U14.

SLAVE SERIAL

- This port, J20 is located beside the USB interface (near J8, and sinal and shorted between them). The signals appear on a 100mil pitch berg sticks.
- J20 can be used to monitor the configuration signals as well to configure the FPGA if needed from an alternate host.
- Slave serial signals are from BANK-0
- It is a 3.3V LVTTL interface and the power comes from LDO U14

Mode control is on J11.

- These pins are pulled high in the PCB,
- Leaving these jumpers open enables the SLAVE SERIAL for the USB card based configuration.
- The **JTAG** mode is always available irrespective of the jumper setting.
- JTAG interface is provided in two parallel set of connectors J22 and J22B
- Since the signals of J22 and J22B are shorted in PCB, NEVER use BOTH (J22,22B) simultaneously.
- J22 is is a 7x2, 2mm pitch connector and the connections are compatible to work with XILINX high speed parallel Cable iV with model no. DLC7 or equivalent using the xilinx provided 7x2 FRC ribbon cable interface.
- J22B is a 100mil pitch, berg stick based connector and is meant to conect to any of the lower version but 3.3V compatible JTAG iterfaces.
- 4.7K Pullup resistor is provided for the TDO
- JTAG and MODE signals are from BANK-0 of the FPGA, which is powered on 3.3V from LDO U14.

Temperature Monitor

- The **FPGAs temperature sensing** pins DXP,DXN are connected to U13, a temperature sensor TMP401, a burr-brown product now available through Texas. This chip can be configured to switch a FAN ON or raise an alarm through J7 (located on the conventional solder side of the board beneath the USB card area) upon high temperature. It can communicate to a remote host through J13 (located beside the USB card interface, J9). This circutry is provided as a fail-safe arrangement, since it can operate irrespective of a specific code in FPGA.

J21

provides access to VP, VN pins of the FPGA, for external voltage measurement. This Jumper is located beneath the General Purpose Berg-Stick Pins J12.

- U5, PTH05010W supplies the VCCO 2.5V IO Banks of the FPGA and the XTAL X1 (J23) , LDOs, U1, U2, U3, and U4. Altering R13,R14 values will change output voltage of U5 LED D5 indicates the presence of output volatge from U5
- U6, PTH05050W supplies the VCCAUX 2.5V, AVDD (pin M15) for the FPGA. Altering R1,R2 values will change output voltage of U6 LED D6 indicates the presence of output volatge from U6
- U7, PTH05010W supplies the VCCINT 1.0V for the FPG Altering R3,R4 values will change output voltage of U7

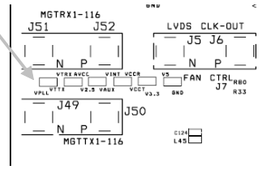
The Supply output from each of these regulators can be conveniently monitored in a Power **MONITORING-PAD-SET** provided at the solder side of the AgFo board (FINISAR mount side) it can be located between SMA pairs J51,52 and J49, J50.

FPGA core and I/O Supplies

1.0V 2.5V 2.5V

POWER Supply SWITCHERS

External +5V



POWER ENTRY

+5V Power enters the AgFo Board from backplane through ERNI POWER TAPs J37A and J37B. Each contact is rated for 8Amps. J39A,B,C,D and J38A,B are alternate power entry points and are of use during bench testing.

J37A,B

J39A,B,C,D

SHILED

Shild ground runs along the side of the boards and near the metal cover of RJ, FINISAR parts. These shiled grounds connects to the board ground through a resistor. (R23, R24,R25,R91A,B,C,D typically 1-Mohms)

Few OTHER FEATURES

LEDs indicator for FINISAR received Power detection
LED to indicate the +5V Power entry (D9)
Reverse connected Diode D22 is protects from reversed power polarity.
- LEDS to indicator for VCCO from U5 (D5), VCCAUX of U6 (D6), VCCR of U8 (D7), VCCT of U9 (d8), and VCCO_3.3 of U14 (D24) regulators.
- Impedance control achieved:

Best to normal: *MGT traces, Clocks traces, RJ45 traces, ERNI traces*
BANK-12 is completely unused. Bits toggling in Bank-12 can affect critical MGT's operation. When MGT 116 and 118 are to be used avoid using RJ25 of J2,3 (ie Bank -16,18).
See Table shown here.

Table 10-5: **Aggressive I/O Banks**

GTP_DUAL	FF665
MGT112	12
MGT114	12
MGT116	12,16
MGT118	12,18

- U1, TPS74401 provides the AVCCPLL 1.2V for the FPGA MGT Altering R5,R5b, and R6,R6b values will change output voltage of U1
- U2, TPS74401 provides the AVTTX 1.2V for the FPGA MGT Altering R7,R7b, and R8, R8b values will change output voltage of U2
- U3, TPS74401 provides the AVTRX 1.2V for the FPGA MGT and the AVCC_RXC 1.2V (through inductor L7). Altering R9,R9b, and R10, R10b values will change output voltage of U3
- U4, TPS74401 provides the AVCC 1.0V for the FPGA MGT Altering R11,R11b, and R15, R15b values will change output voltage of U4

LDOs U1,2,3, and 4 are powered from VCCO_2.5V from (PTH05050 (U5) Power enters each MGT through independent filter network.

- U8, TPS74201 provides the VCCR 3.3V for the FINISAR SFFs and SCAN (U11).
- Altering R16,R16b, and R17, R17b values will change output voltage of U8
- U9, TPS74401 provides the VCCT 3.3V for the FINISAR SFFs, Buffer (U12) and XTAL (X1). Altering R18,R18b, and R19, R19b values will change output voltage of U9
- U14, TPS74201 provides the VCCO 3.3V for the FPGA Banks 0,1, and 2, and TMP401 (U13) Altering R20,R20b, and R22, R22b values will change output voltage of U14.

- LDOs U8,9, and 14 are powered from External 5V.

3.3V I/O, MGT and SFF supplies,

VCCO_3.3V 3.3V | AVCCPLL 1.2V | AVTTX 1.2V | AVTRXC 1.2V | AVCC 1.0V | VCCR 3.3V | VCCT 3.3V

External +5V

VCCO_2.5 U5, PTH05050W

POWER Supply LDOs

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SOURCE:USB_PRABU-T//AgFoDocuments/LAYOUT_Plan_detailed/AgFo_overall_block_diagram-V0.sdr