Rev.	ECO	Description	Author	Approved	Date

Massachusetts Institute of Technology
Kavli Institute for Astrophysics and Space Research (MKI)

Printed Wiring Boards (Astro-E)

Dwg. No. 29-00103
May 28, 2014

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Preface

1.0 Scope

This drawing defines the design, fabrication, test and inspection requirements of double sided and multilayer printed wiring boards (PWB's), for use in Astro-E.

2.0 Applicable Documents

The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the latest released version on the date of invitation to bid, is applicable.

Standards	
IPC-CF-150F	Metal Foil for printed Wiring Applications (Institute for printed Circuits Standard)
IPC-D-275 (MIL-STD-275)	Printed Wiring for Electronic Equipment
Specifications	
MIL-P-55110	General Specification for Printed Wiring Boards
MIL-P-13949	Plastic Sheet, Laminated, Metal Clad (For Printed Wiring Boards), General Specification for
MIL-C-14550	Copper Plating (Electrodeposited)
MIL-P-81728	Plating, Tin Lead (Electrodeposited)
Handbooks	
NHB5300.4 (3I)	Requirements for Printed Wiring Boards
HB5300.4 (3K)	Design Requirements for Rigid Printed Wiring Boards and Assemblies
MIT	
36-02106	PC Design – Component Library

2.1 Order of Precedence

In the event of conflict between the text of this document and the references cited herein, the text of this document takes precedence.

3.0 Requirements

3.1 PWB Design

The goal for printed wiring board (PWB) design is per NHB5300.4 (3K). The requirement for the design of printed wiring boards is IPC-D-275, as modified by this specification.

3.1.1 Board Design – External Annular Rings

The board design shall allow fabrication with external annular rings for plated-through holes of 0.005inch, and 0.015 inch for non-plated-through holes.

3.1.2 Board Design – Internal Annular Rings
The board design shall allow fabrication with minimum annular ring in internal layers of 0.002 inch.

3.1.3 Conductor Thickness – External Layers
Conductor thickness and width for external layers should be per figure 6-1 of NHB5300.4(#K), assuming a 20°C rise.

3.1.4 Conductor Thickness – Internal Layers
Conductor thickness and width for internal layers should be per figure 62 of NHB5300.4(3K), assuming a 20°C rise.

3.1.5 Minimum Conductor Spacing
Minimum conductor spacing should be per table 6-1 of NHB5300.4(3K). If this requirement cannot be met, the conductor spacing may be reduced, but not less than the conductor spacing requirements of IPC-D-275.

3.1.6 Board Thickness
The thickness of finished boards as measured over the outside plating shall be per the PWB drawing.

3.2 PWB Layout and Outline

3.2.1 Layout
PWB layout shall be in accordance with the applicable MIT schematic and associated parts list.

3.2.2 Outline
PWB outline and layer assignments shall be in accordance with the applicable MIT outline drawing.

3.2.3 Surface Mount Land Patterns
Land patterns shall be in accordance with 36-02016.

3.2.4 Reference Designators
Reference designators are identified on the schematic drawing. The reference designators shall be marked adjacent to the envelope of the component on the PWB. If space does not permit, the reference designator may be placed within the part footprint.

3.3 Material

3.3.1 Copper
The copper clad laminated sheet and bonding material shall be in accordance with MIL-P-13949. Copper foil shall be in accordance with IPC-CF-150F, type THE, class 3, for 1 and 2 ounce/ft.^{2} copper.

3.3.2 Solder Mask
Solder Mask shall be SR-1000, Vacrel 8140, Ciba-Geigy Probimer 52, or Conformask 2000. Solder Mask must be applied over bare copper.

3.4 Plating

3.4.1 Copper

Plated through holes and outside layer conductor shall be copper plated per MIL-C-14550 to a minimum thickness of 0.01 inch.

3.4.2 Tin-Lead

Tin-lead plating shall be in accordance with MIL-P-8178, followed by reflow. Tin content is to be maintained at or above 58%. Tin lead fusing via hot oil reflow process is preferred, however, infrared leveling may be used.

3.5 PWB Fabrication

The goal for Printed Wiring Board (PWB) fabrication is per NHB5300.4 (3I). The requirement for the fabrication Printed Wiring Boards in MIL-P-55110 and this specification. Holes shall be drilled using new drills only, with 1200 hits predrill maximum. Panel stack during drilling shall not exceed three (3) panels.

3.6 Warp and Twist

Printed Wiring Boards shall not have warp or twist resulting in a total deviation from a flat plate exceeding 0.010 in/in.

3.7 Identification and Marking

Marking shall be on the part mounting side and shall include, s a minimum:

Marking	Obtained from
Manufacturer's Name	PWB Manufacturer
Manufacturer's P/N	PWB Manufacturer

3.7.1 Serial Number

Each PWB shall be uniquely serialized with a three (3) digit number, starting with 201 for Engineering boards and starting with 301 for fight boards, as stated in the purchase order.

3.8 Workmanship

Workmanship shall be of a quality which will assure a product free of foreign materials, burrs, corrosion, scratches, chips, sharp edges, particles, or other defects which could affect serviceability or appearance.

4.0 Quality Assurance Provisions

4.1 Responsibility for Inspection

Unless otherwise specified in this document, the PWB manufacturer is responsible for all inspections, examinations, and tests, as specified herein.

4.2 Quality Conformance Inspection (QCI) Test Coupons

4.2.1 Coupon Requirements

Quality conformance inspection shall be in accordance with <IL-P-55110. A total of three (3) coupons are required per panel. Coupons shall be clearly marked t identify panel and boards represented by the coupon.

4.2.2 Disposition of Coupons

The PWB manufacturer shall inspect one (1) coupon per this specification, deliver one (1) coupon per panel to MIT and archive one coupon.

4.2.3 Configuration

The configuration of the test coupons will conform to IPC-D-275

4.2.4 Coupon Microsections

1. Coupons for multi-layer PWB's require a pad at each layer of the microsection.
2. There shall be no delamination of the individual layers or plies when viewed in the microsection.
3. Plating voids are not permitted when viewed in the microsection.
4. Minimum annual ring on internal layers of multilayer boards is .002 inch.

4.3 Acceptance Tests

The circuitry of each board (100%), shall be tested for continuity and shorts in accordance with paragraph 3I516, subparagraph 10 of NHB5300.4 (3I). The minimum insulation resistance shall be greater than 100 Megohms at 60 V DC.

4.3.1 Visual Inspection

The PWB shall be inspects to insure that it meets the size and pattern requirements of the outline drawing, and the identification and marking requirements of 3.7 herein. Measling and crazing of the bare boards shall not exceed 2% of the board area, and shall not reduce the spacing by more than 25%.

4.3.1.1 Minimum External Annual Ring

Minimum external annular ring for plated-through holes is .005 inch, and .015 inch for non-plated-through-holes.

4.4 Inspection and Test Records

Test data for all acceptance/screening tests and inspections shall be submitted to MIT with the delivery of the PWB. In addition, the PWB manufacturer shall maintain inspection and test records for 36 months after PWB delivery to MIT.

4.5 Product Uniformity

All PWB's of a given part number and revision, delivered to MIT, shall be made with the same design, materials, processes, and procedures, and shall be tested and inspected to the same criteria conforming to this specification.

5.0 Preservation and Storage

5.1 Packing, Packaging, and Marking

Preservation, packing, packaging, and marking shall be in accordance with MIL-P-55110, paragraph 5.0, for immediate domestic usage.

6.0 Notes

6.1 Approved Sources of Supply

- Layout – TBD
- Fabrication - TBD