Rev.	ECO	Description	Author	Approved	Date
01	32-217	Initial Release	DAG		5/16/07
02	32-221	Minor Modifications following SN001 Test	DAG		6/7/07

CRaTER Digital Board Test Procedure

32-60003.04 - Version 0.02 – 07 June 2007

Test Unit: _____
Test Date: _____
Tested By: _____

1. Overview

This document describes the CRaTER Digital Board (CDB) test procedure. This procedure shall be performed on the flight CRaTER Digital Board prior to mating with other flight hardware. This test sequence shall provide a functional verification of all CDB functions, and an overall electrical checkout of the CDB subsystems.

2. Handling Issues

The flight CDB shall be handled with appropriate precautions to ensure high reliability. The board shall be handled only with clean gloves, and shall remain bagged or boxed in clean ESD-protected environment when not in use. An appropriately grounded ESD wrist-strap shall be used while handling the CDB, and gloves shall be periodically grounded to avoid charge build-up.

Probing on the flight hardware is to be minimized. Oscilloscope probes and other relatively heavy test probes that can stress component leads shall not be clipped directly to flight component leads.

3. Test Equipment

The testing shall involve the following equipment:

1. Bench Power Supply (triple: one independent output at 5V, 1A, and two tracking at +/- 5V, 0.5A)

2. Bench Power Supply Cable to on-board HD26.

3. CRaTER Engineering Unit (including the Analog board, Telescope, HD78 Analog to Digital cable assembly, DC to DC converters and power supply HD15 cable assembly).

4. Bench Power Supply (single: 0 - 35VDC at 1A). (May be able to reuse item 1 for this function.)

5. Connector savers: HD26 and HD78

6. Oscilloscope, Multimeter (capable of current, voltage and resistance measurements), Logic Analyzer

7. 1553 Bus Data Acquisition System (Ballard OmniBox) (+ bus coupler, terminator and cables, as per CRaTER engineering GSE set-up)

8. MCD Interface box (sits between the OmniBox and the CRaTER subsystem; gates/drives the spacecraft One-Hertz Clock.).

9. Sun Workstation (or equivalent GSE computer).

10. Thermometer (for measuring ambient room temperature).

4. Pre-Test Inspection

The CDB shall be inspected by QA following fabrication, and prior to the start of testing to verify appropriate workmanship levels.

Prior to testing, the CDB shall be inspected to verify the following:

1. CDB Serial number:_____
2. State of the following resistors (populated or not populated) (INST SER #) :
   R182_____ R180_____ R178_____ R176_____ R174_____
3. The "do not populate" parts are: C3, C7, C11, C69, C73, C77, D504, D505.
   R143____ R142____ (spare sites) R503_____ R535_____ (set at test)
   Check that they are not installed: ____ JP2 (installation as testpoint only)_____
4. All remaining components are installed. Note any exceptions other than the "do not populate" parts and the INST SER # resistors mentioned above:
   _____
5. Check these resistor values: R51 (200 Ω): _____, R52 (200 Ω): _____
6. Check tantalum capacitors (C21, C22, C23, C85, C86, C87, C88, C89, C501, C502) diodes (D1, D2, D506, D507, D501, D502, D503), transistors (Q1, Q501, Q504, Q502, Q503) and ICs are installed with the correct polarity according to the silk-screen on the PWB: _____ Check that D11, D12, D13, D14, D15, D16 are installed correctly (silkscreen does not apply). Anode should connect with analog ground; cathodes to peak stretcher inputs)_____
7. Check status of on-board jumper: JP1 (TRST to GND): _____ (should be installed as wire).

5. Initial Power On Test

5.1. *Configure CDB:*

〈 Measure Resistance of CDB prior to power-up. Note the following:
   1. VCC (TP19) to GND (TP17): _____ (should be > 200 ohms)
   2. VCC_A (Testpoint near U14) to GND (TP17): _____
      (should be > 200 ohms)
   3. AVP to AGND (U2-15 to U2-8):_____ (should be > 1Kohms)
   4. AVN to AGND (U2-2 to U2-8):_____ (should be > 1Kohms)

NOTE: actual measurement may vary depending on the ohmmeter used.

〈 Attach bench supplies with current monitor/limiters to provide +5.0V for VCC, +/-5V to AVP/AVN. Set the current limiters to: 5V = 0.8 A.; +/- 5V to 0.5A.

〈 Connect Chassis Ground to both supply returns at the power supply:_____

〈 Test the cable outputs before mating with the CDB:

Measure resistance: cable pin 23 to pin 19: _____ (should be close to 0 ohms)
Turn on Supply. Verify correct voltages:

VCC - pin 5 to pin 23:_____
AVP (+5V) – pin 3 to pin 19: _____ AVN(-5V) – pin 1 to pin 19:_____

5.2. *Power-up*

__ Verify that connector saver is in place for J1 connection.

- 〈 Power off the bench supply and attach power supply board the CDB connector J1 (via connector saver).
- 〈 Turn all the power supplies on simultaneously. Turn off immediately if any supply hits its current limit.

Verify supply voltages: VCC_____ AVP_____ AVN_____ VCC_A_____
Verify VREF (at U34-7):_____ (should be 2.5V)

Note current drains as shown on the power supply meters:
VCC_____ AVP_____ AVN_____

5.3. *Verify Clocks*

Using an oscilloscope, verify that the output of oscillator (Y1) generates a clean periodic clock. Probe at via (directly "above" TP24) connecting to FPGA (U15-82). Ground scope at TP17. CLK16M should be 16.0MHz, 50% Duty Cycle; 0-5V square wave; monotonic rise/fall times, <0.5Vpp ringing).
NOTES:_____
(If possible, take pictures of clock waveform and include with this procedure.)

Using an oscilloscope or logic analyzer, verify the one second tick (at testpoint TP15). It should be operating with a 1.05 second period, positive going pulse with high-period of 62.5ns). Period:_____ Pulse-width:_____

5.4. *Measure Power-on Reset*

With an oscilloscope, measure the power-on reset time (CH1 = VCC; CH2= HWRSTL U12-8). Note the time from +5.0V crossing 4V to RESET going inactive. _____

This value should be > 10milliseconds. OK:_____
(Attach pictures if possible.)

5.5. *Relay Turn-on*

Measure the relay turn-on time (CH1 = U19-8; CH2= HWRSTL U12-8). Note the time from HWRSTL deassertion to the RELAYON assertion. _____

This value should be between 1 and 2 seconds OK:_____

6. Basic Functionality Verification

6.1. *Connect GSE and 1553 Bus Data Acquisition*

With the power off, connect the GSE 1553 (OMNI-Bus box) to J3. Connect the S/C Clock to J4, pins 1 and 3.

Start up the following scripts on the GSE Computer: CHouse, CCmd. OK:_____

Reapply power to CDB. If the 1553 bus interface is working, data should appear at the GSE computer. Verify that the time is updating, and the housekeeping and secondary science messages are being transmitted. OK:_____

To observe the data, use "rtlm –x ….." or "CData 120 121 122 –z –x".

Check the FPGA Revision (returned in upper nibble of housekeeping "WORD 6":_____

Using rtlm, verify that all three types of telemetry packets (APIDs 120, 121 and 122) are being transmitted once/second:_____

Check Housekeeping supply voltage readout: VCC:_____ AVP_____ AVN_____

Housekeeping display should indicate the S/C Clock operation. OK: _____

Re-measure the one-second tick (at TP15). It should be operating with a 1.00 second period, positive going pulse with high-period of 62.5ns).
Period:_____ Pulse-width:_____

Remove the clock (using disable at the MCD Interface box). Housekeeping display should indicate the Internal Clock operation, and the one-second tick should revert to a period of 1.05 seconds. OK: _____

Re-enable the spacecraft clock. OK:_____

6.2. *Run Testmode diagnostics (verifies SRAM and 1553 bus interface)*

Send an "echo" command, with the data field set to 8. Verify for both sides.
Side A (J3) OK:_____ Side B (J4) OK:_____
Command the system into test mode. Verify that the test mode data patterns in the primary science telemetry. OK:_____

Using CArchive, set up a data storage file (all APIDs).
Note file name:_____

Run the system for at least 15 minutes in testmode, while archiving the data.
Time test started:_____ Time test ended:_____

Run the testmode check program as follows:

```
rtlm -x -r <filename>.bin | craterCheck
```

A summary of the following form should be printed to the screen:

```
removing comment line
!! Got the first testmode case - setting synch0 bit
!! Got the second testmode case - setting synch1 bit
** Duplicate Pkt Count  848    847
No more data .... terminating
IserNum: 10 Packets Checked: 2279   PS: 2079  SS: 100  HK: 100  Last SSCnt:  847
  Error Breakdown:   ApIDErr: 0  HdrBitCorr: 0
                     SSCnt - PS: 1  SS: 0  HK: 0   Drop1s: 0  Repeat1s: 1
                     PLen  - PS: 0  SS: 0  HK: 0
                     Data  - PS: 0  PS-MultErrs: 0
```

It is normal to get one "Duplicate Pkt Count" when the program terminates. This is tallied as one "Repeat1s" and one "SSCnt" error. Any other errors should be investigated, as they may indicate a faulty SRAM, FPGA or 1553 Bus Subsystem.

Note duration of testmode data collection:_____
Note results of craterCheck:

```
IserNum: ____ Packets Checked:_____   PS: _____  SS: _____  HK: ____  Last SSCnt:  _____
```

Error Count OK:_____

If the error count is "not OK", save the archived file for analysis. Debug (beyond the scope of this document) will be required.

6.3. *Check LLD and ECAL Voltages*

This section verifies the analog voltage generation (and the housekeeping analog to digital conversion) by checking some sample settings, comparing the housekeeping values to the actual measured values.

The LLD settings should default to midscale (setting = 128, 0x80); the ECAL defaults to the low setting (0).

Set these voltages via the Command Window (initiated with the CCmd script). To minimize probing, the voltmeter readings should be limited to the following settings: 0, 0x80, 0xFF. Record the Housekeeping results in decimal (volts) format, as shown on the CHouse display.

NOTE: DC values appear at: ECAL – U16-1; LLD-THIN – U17-1, LLD-THICK – U18-1.

Set to: Hex	Dec	LLD Thin Housekpg Volts	LLD Thin Housekpg Counts	LLD Thin Meter	LLD Thick Housekpg Volts	LLD Thick Housekpg Counts	LLD Thick Meter	ECAL Housekpg Volts	ECAL Housekpg Counts	ECAL Meter
Default Setting										
0x00	0									
0x01	1									
0x02	2									
0x04	4									
0x08	8									
0x10	16									
0x20	32									
0x40	64									
0x80	128									
0xFE	254									
0xFF	255									

6.4. *Check Bias Supplies*

6.4.1. Choose Bias Resistor

Resistor R502 should be populated with a 100K resistor. R503 should be open. R535 should have flying leads to which we will attach a select-at-test trial value. Command the bias supply on and record the value of the voltages at TP503 and TP504. We expect initial values of around 110 and 230 volts.

Then for each case, command the bias supply off, select a new value for R535, and command the bias supply on; record the test point values. Based on this data, the cognizant engineer will choose a fixed flight value to be inserted at R503. We expect the final values to be approximately 140 and 280 volts.

R535	TP503	TP504
Open		
100K		
50K		
25K		
10K		
Select:		

After the fixed value for R503 has been installed and verified, we can proceed.

6.4.2. Check Bias Supplies

The Bias Supplies default to "off". Record their default setting, command them on, and note the "on" voltages:

Set to:	Bias Thin Housekpg	Bias Thin Voltmeter	Bias Thick Housekpg	Bias Thick Voltmeter
Default Setting (Off)				
On				

NOTE: Bias voltages appear at: Bias Thin – TP506 (or R537); Bias Thick – TP505 (or R538)

Command the Bias Supplies off again, and verify the return to the off setting. OK:_____

Measure the turn-on time and overshoot for both supplies with an oscilloscope and store the plots with this test procedure.

Note overshoot for both supplies: Bias Thin:_____ Bias Thick:_____

7. Full System Test/Verification

7.1. *Integrate with the CRaTER Engineering System*

Power-down the bench supply and unplug the HD26 from the CDB. The CRaTER engineering unit is used for the remainder of this testplan. It should be assembled on the bench, powered by at J1 via the 28V bench supply (current limit set to 1 A.). _____ Chassis Ground should be connected to the Power Supply negative output._____

The Omnibus Box should be connected to the 1553 bus connector J3 (side A). The Spacecraft Clock should be connected at J2. _____

With the CDB in the engineering unit, but the HD26 still disconnected, verify supply voltages at the output of the HD26.

HD26-Pin	Signal Name	Measured Voltage	Expected Nominal (Volts)
1	AVN		-5
2	AVN		-5
3	AVP		+5
4	NC		float
5	VCC		+5
6	VCC		+5
7	GND		0
8	28VS		0
9	28VP		+28
10	AGND		0
11	AGND		0
12	AGND		0
13	AVP		+5
14	NC		float
15	GND		0
16	DTEMP2		~2V
17	DTEMP1		~2V
18	28VN		0
19	28VP		+28
20	AVP		+5
21	NC		float
22	PURFLWRATE		~2.5
23	GND		0
24	GND		0
25	GND		0
26	NC		float

HD26 Connector OK:____

Turn off bench supply and connect the HD26 (via a connector saver) to the CDB.

Connect the (engineering) analog board to the CDB via a connector saver at J5:____

Turn power on. Immediately turn-off if the supply hits the current limit.

7.2. *Housekeeping Checkout*

We are not calibrating the detector bias currents, since stability is the issue, not accuracy. The dosimeter is only an 8-bit value, and is what it is.

Quantity	Actual	Telemetry Hskp Vals	Telemetry Counts
28V bus voltage			
28V bus current			
+5V digital			
+5V analog			
-5V analog			

Note the Total Power number returned by CHouse: _____W _____ (counts)
Turn on the Bias Supply.
Note the Total Power number returned by CHouse: _____W _____ (counts)

Temperature reading must now be calibrated by letting the instrument stabilize to ambient with the power off, then turned on and all the temperatures (and purge rate) recorded after a 1 minute stabilization period. The resulting data will be used to normalize all the readings, most likely to the analog board reading.

Temperature	Ambient	Telemetry Hskp Vals	Telemetry Counts
Telescope			
Analog Board			
Digital Board			
DC-DC Supply			
Bulkhead			
PRT			
Purge Rate	Zero flow		

Following stabilization, archive a few seconds of the Housekeeping Telemetry and include with test procedure results.

7.3. *Check Interface and Operation with the Analog Board/Telescope*

In this section, the test pulser is used to stimulate the six measurement chains, and data integrity examined.

Turn on the Bias Supply. Record typical singles counts.

D1_____ D2_____ D3_____ D4_____ D5_____ D6_____

All singles counts should be close to zero; D2, D4 and D6 often show a few counts/seconds. OK_____

The PHA event counters should be all zeros, and LLD thresholds at their defaults (0.48V). OK_____

Verify that the test pulser is in its default state: ECAL = 0V, both pulser clocks off.____

For the following measurement sequence, disable all the detectors except the active measurement chain. Lower the LLD (Thin for D1, D3, and D5; Thick for D2, D4 and D6) until the event start arriving at the interface (as evidenced by the PHA event counters). Record this LLD setting for each detector.

Detector	Noise Floor (Borderline LLD Threshold)
D1	
D3	
D5	
D2	
D4	
D6	

Command the LLD settings to about 15mV. Record the settings:
LLD-Thin:_____(decimal, commanded parameter) _____mV (readback)
LLD-Thick_____ (decimal, commanded parameter) _____mV (readback)

Enable all six detectors.

Turn the pulser low clock on. Until the ECAL level is raised, the PHA event rate should be near zero. (D2, D4 and D6 may trigger every few seconds when the telescope is connected.) OK:_____

The Pulser Rate should be at 8Hz (default)._____

Set the ECAL voltage to the following levels and invoke the "statistics" program with the –m option (in order to view the min/max/mean values for each channel) and –n option (set the averaging interval to 32). Record the results for each D1 and store the results for all six detectors to be attached to this procedure. Use the following ECAL settings:

ECAL (dec) (commanded)	ECAL (hskpg readback)	D1 Std Dev	D1 Mean
31			
63			
127			
159			
191			
223			
247			

PHA Event Rates for above: Good:_____ Reject:_____ Total:_____

Set the Pulser Rate to 2KHz._____
As above, collect the statistics, with the averaging interval set to 4000:

ECAL (dec) (commanded)	ECAL (hskpg readback)	D1 Std Dev	D1 Mean
31			
63			
127			
159			
191			
223			
247			

PHA Event Rates for above: Good:_____ Reject:_____ Total:_____

,

Set the Pulser Rate to 8Hz_____ Turn the pulser low Clock off_____
Turn the pulser high clock on. ___

Collect statistics with the averaging interval set to 32.

ECAL (dec) (commanded)	ECAL (hskpg readback)	D1 Std Dev	D1 Mean
31			
63			
127			
159			
191			
223			
247			

PHA Event Rates for above: Good:_____ Reject:_____ Total:_____

Set the Pulser Rate to 2KHz_____
Collect statistics with the averaging interval set to 4000.

ECAL (dec) (commanded)	ECAL (hskpg readback)	D1 Std Dev	D1 Mean
31			
63			
127			
159			
191			
223			
247			

PHA Event Rates for above: Good:_____ Reject:_____ Total:_____

8. Marathon Test Log

During the execution of this test procedure, various CDB tests may be run in a batch mode, as listed below:

Test Name	Time started	Time stopped	Results/Comments