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CRaTER
Digital Electronics Worst Case Analysis

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1 Scope

A worst case analysis of the CRaTER digital electronics was performed and documented in this report. The CRaTER digital electronics consists of one printed circuit board. It interfaces to the Spacecraft (1553 bus + one differential signal) and the Analog Processing Board (APB).

The worst-case analysis addresses the digital circuitry, signal processing subsystem and the interface between the two power domains.

2 Applicable Documents

32-03003 CRaTER Digital Board Schematic
32-02052 Analog to Digital Subsystem Electrical ICD
32-02002 Spacecraft to CRaTER Electrical ICD
32-03010 Digital Subsystem Functional Specification

3 Digital Circuitry

3.1 Parts Types

The following parts types appear in the digital segment, or at the interface between digital and analog:

Description	Part Type	Vil max	Vih max	Vol max	Voh min
FPGA	RTSX72-SU	0.8	2	0.5	4.5
Schmitt trigger/inv	54AC14K02V	1	2	0.1	4.9
SRAM	2568C-30D	1.5	3.5	0.05	4.2
Diff Rec	26CT32K02V	0.8	2.5	0.4	4.1
1553 Bus Control	BU-63705F-300	0.8	2	0.5	4
Oscillator	QT50AC6M-16.000MHz	N/A	N/A	0.5	4.5
A/D Conv	MAX145	0.8	3	0.4	4.5
Demux	CD4514BMS	1.5	3.5	0.4	4.6
Analog Switch	CD4066BMS	1	3.5	2.5	2.5
Peak Stretcher	PH300RH	0.8	2.4	0.5	4
Comparator	RH119W	N/A	N/A	0.5 4.9	4.9

All of the logic thresholds below are drawn from the specification sheets, using the “low current” output model (since all parts are CMOS technology).

Voltage thresholds were computed based on a 5V digital supply. One component (MAX145) is powered by the analog supply. But, as can be seen above, this part will still perform adequately with 10% fluctuation in either supply.

3.2 Timing

3.2.1 Clocks

There are three clocked devices in the design. In the generation of control logic, only the rising edge of the system clock is used.

The BU-63705 is clocked at 16.000MHz, its nominal rated frequency (necessary for correct operation of the 1553 bus). Although the same master clock is used for the FPGA, the signals arriving from the BU-63705 to the FPGA are considered asynchronous. The 1553 Bus Data strobe is synchronized (with an edge detect and resampling) to the internal FPGA clock before any sampling/processing occurs.

16.000MHz is a relatively slow master frequency compared to the inherent speed of the FPGA technology. However, timing verification (both static and dynamic) is performed each time the FPGA is rerouted. The radiation tolerant FPGA is modeled with a TID specification of 50KRAD, and over the full military temperature range.

The third clocked component, the analog to digital converter (MAX145), operates at 2 MHz (maximum specified operation is 2.17MHz).

Comparator signals from the analog electronics to the FPGA are treated as asynchronous, and sampled/filtered/synchronized to the master clock.

3.2.2 Propagation Delays/Setup Margins

There is at least 20% margin on the data bus I/O (1553 bus and SRAM data) and serial data (ADC) input. All outputs strobes are held for at least 20% beyond the required minimum.

3.2.3 Transition Times

The Actel FPGA places a restriction on input transitions times, specifying a10ns maximum rise or fall time: "If t_r or t_f exceed the limit of 10ns, Actel can guarantee reliability but not functionality."

Unfortunately most devices do not specify the maximum transition times of their outputs. And the one that does, the oscillator, shows 15ns as the maximum rise/fall times. Here, the design fails "on paper". We will monitor the clock transition time and make sure that it is within the Actel limits, and exhibits all the characteristics of a good clock (monotonic rise/fall, minimal ringing).

The comparator output transition times are likely to be on the order of a few hundred nanoseconds. The FPGA does not use these signals as clocks. They are sampled, and activate a state machine if they show a solid high. The state machine locks this signal out for 12μs following activation; the comparator deasserts about half-way through this sequence. Although the design works around the Actel transition time issues, we will carefully monitor these signals during the engineering unit debug, and add AC14s in between the FPGA and the comparators if this is deemed necessary.

The 26C32 also specifies a maximum transitions time with respect to the differential inputs. In this case, the restriction is 500ns (very reasonable). The S/C Interface drives these inputs. We will verify the electrical characteristics of this signal (CLK1HZ) during integration.

3.3 State Machine Methodology

State machines are Gray-coded. All unused states are defined and result in a return of the state machine to its IDLE configuration (also forced as a result of a system reset). Each state machine is designed to avoid "hang-up" in the event of an SEU or similar anomaly.

3.4 Reset

The Power-On Reset jams all the FPGA state machines into their default configuration and serves as an input to BU-63705. Power-On Reset is held at least 25 milliseconds after Vcc has ramped up to nominal. Since the driver of the power-on reset is an AC14 gate, the rise time is very fast (a few nanoseconds).

For the FPGA, the reset pulse-width requirement is only a few periods of the system clock; BU63705 requires at least 100ns with a rise time of less than 10 microseconds. The oscillator startup time is specified as a maximum of 10 milliseconds.

Reset pulse width and oscillator startup will be verified during initial bench check-out, and re-checked with the actual flight-parts.

4 Data Acquisition

The requirements to meet the science goals can be met with an 8-bit converter; the desire is to have 10 bits of accuracy. The MAX145 is rated for 12 bits with no more than ½ LSB error over all combinations of supply voltage (2.7 to 5.25 VDC) and temperature (-40 to 85 C). The 5 volt analog bus supply is guaranteed to be within 75 mv of 5.000 VDC at the supply, so that adequate margin exists against the maximum specified voltage of the A/D. Any line drop, and certainly as much as 100mv might be expected, is easily within the acceptable (2.7 VDC) range of the A/D.

Similarly, the LT1498 op amps can operate from 2.2 to 30 VDC; the AD584 voltage reference is good from 4.5 to 15 VDC. Our only problem here is the Amptek peak stretcher, PH300, which the manufacturer simply specifies to operate at "+5" and "-5" VDC. We will have to screen these parts to assure that adequate performance margin exists.

5 Power Domain Interaction

There are two main services entering the digital electronics board: Vcc (5V digital) and A5VP/ A5VN (the plus and minus analog supplies, also 5V). Two DC/DC converters, powered by a common 28VDC input, provide these services. During normal operation, these supplies will be on at the same time. However, during testing, one or the other may be compromised. Care has been taken to assure that no part would be damaged should one of the services fail or be shorted to ground.

High voltage services (225V/75V) is derived from Vcc and enabled by the control logic resident in the FPGA. 2.5V, derived from Vcc, by a linear regulator, is supplied to the FPGA.

The digital control logic has the ability to sense the absence of A5VP. If the analog supply is not present, the digital controller will hold all logic signals to the analog segment at ground levels, force the analog housekeeping subsystem into a dormant state, and disable high voltage generation.

6 Termination and Decoupling

All strobes and clocks exiting the FPGA use series termination. The electrical characteristics will be examined and optimized on the engineering unit.

The master clock is terminated with a parallel R/C to ground.

Device decoupling consists of approximately one 0.056 μF capacitor (certain components are decoupled with 0.01 μF). The FPGA and 1553 bus I/F ICs use multiple decoupling capacitors, as recommended by the manufacturers' specifications.