Rev	ECO	Date	Change Summary	Author
A	32-205	28 Mar 2007	Initial Formal Release *(corresponds to FPGA Version 3)*	D. Gordon

CRaTER Digital Subsystem Functional Specification

Revision A
28 March 2007

Dwg. No.: 32-03010

References.

1. Spacecraft to CRaTER Data Interface Control Document, (32-02001.01), Revision E, January 12, 2007
2. CRaTER Analog to Digital Subsystem Electrical Interface Control Document, (32-02052), Revision B, 5/17/2006

Pre-Release Revision History

Rev	ECO	Date	Change Summary	Author
01	32-114	19 APR 2006	Initial Draft	D. Gordon
02	32-121	05 May 2006	Corrections to bit/byte ordering; addition of testmode; changed “Telem. Stall Counter” to “Good Event Counter”	D. Gordon
03	32-141	30 May 2006	Bias Clocks removed, Secondary bias voltage control signal added, Analog Voltage Monitor added	D. Gordon
04	32-178	05 Oct 2006	Correction to DetEnb field ordering in Secondary Science Testmode enhancements Addition of Relay Control for 1553 bus transformer Default Polarity of Test Pulser Clocks changed *(corresponds to FPGA Version 1)*	D. Gordon
05	32-190	06 Dec 2006	Pulser Low Frequency changed to 8Hz Housekeeping values averaged *(corresponds to FPGA Version 2)*	D. Gordon
06	32-204	27 Feb 2007	Pulser Clock is timed GATE is eliminated (held high); RAMP is extended *(corresponds to FPGA Version 3)*	D. Gordon

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1.0 Introduction

The CRaTER Digital Control (CDC) is a subsystem of the CRaTER (Cosmic Ray Telescope for the effects of Radiation), an instrument in the LRO (Lunar Reconnaissance Orbiter). The "front-end" interfaces to the analog electronics, receiving the linear and trigger outputs (preprocessed by the Analog Processing Board) corresponding to six solid state detectors. The "backend" interfaces to the spacecraft via a 1553 bus interface. A radiation tolerant field programmable logic array (FPGA) houses the digital circuitry that receives commands, collects the digitized "events", filters the events in accordance with the preset configuration, and formats/sends telemetry packets.

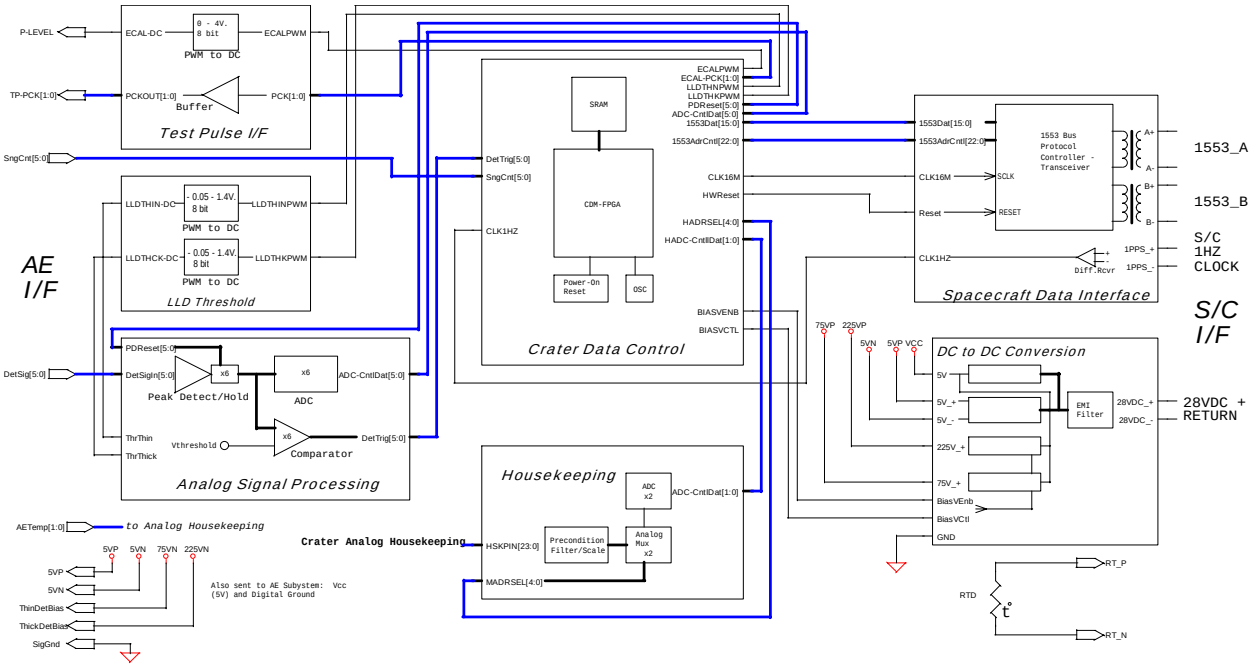


FIGURE 1. CRaTER Digital Subsystem: Overall Block Diagram

Figure 1 shows an overview of the CRaTER Digital Subsystem. Commands arrive at the 1553 Bus Interface, the top right module. Commands typically set values internal to the Crater Data Control (CDC) FPGA that relate to event acceptance criteria. A few commands directly set external controls, such as the Test Pulser DAC and Bias Voltage Enable. Events, processed and packetized by the CDC, are forwarded to the S/C via the 1553 bus interface.

The Analog Signal Processing subsystem consists of six identical slices. Each slice receives a detector signal, holds the peak, and compares it to a set threshold. A/D conversion follows peak detection if any of the events cross threshold. Additionally, six digital signals indicating detector specific threshold crossings are driven by the Analog Processing board. A test pulser DC level and clocks, configurable via the command interface, facilitate testing.

The Housekeeping Data Controller regularly acquires data from an on-board ADC, maintaining a register file which the 1553 Bus Interface Module periodically reads.

The Master Clock (16 MHz), generated via an on-board oscillator, drives the FPGA and the 1553 Bus Protocol IC.

This document describes the FPGA functionality, referring to the external circuitry only as it relates to the FPGA design.

2.0 CDC Subsystems

2.1 Timing Control

A 1PPS (1 second clock) is received from the Spacecraft.

Edge detect circuitry converts the 1 second clock (leading edge) into a one clock-pulse wide tick (TK1S) that is forwarded to all the CDC logic subsystems. TK1S loads the time registers, and causes the pre-staged commands to be registered into the active stage.

The S/C forwards a “Time of Next Sync Pulse” every second that updates the CDC “seconds and subseconds” registers. If the “Time of Next Sync Pulse” Command is not received during any one-second interval, the seconds and subseconds register are cleared by the following TK1S. These registers are a component of the secondary header, included with all three type of telemetry packets (Housekeeping, Secondary Science and Primary Science).

A division of the Master Clock serves as a backup for the spacecraft 1 second clock. Each TK1S clears the divider. In the absence of the 1 second clock, the counter will produce its own TK1S with a period of 1.05 seconds. An indication of the TK1S generator (internal versus external) is provided in the 1553 Telemetry Secondary Headers.

The timing control subsystem provides a relay control, asserted between 1 - 2.5 seconds following the deassertion of the power on reset signal. The relay control assures that the 1553 bus transformers are disconnected at power-on due to a potential overcurrent condition.

2.2 1553 Bus Control

The 1553 module consists of two autonomous subsystems: a command receiver/parser and a telemetry packet builder/transmitter. An external Remote Terminal IC (BU-63705) serializes/deserializes and performs error detection on the incoming “messages”. CDC logic strips the relevant data out of the commands and supplies data for telemetry.

CDC operates as a Remote Terminal (RT) at address 0x10 (16 decimal), set via BU-63705 inputs RTADDR(4:0) (= 10000) and RTADDRP (=0) (the parity bit). The BU-63705 responds only to commands and requests for telemetry that match the set RT address. Within the RT address, CRaTER responds to eight subaddress for commands (see Section 2.2.1) and three for telemetry (seeSection 2.2.2). Transactions directed to unused subaddresses will be serviced (i.e. data requests will be acknowledged); however, there will be no response from the subsystem, and data supplied (in response to telemetry requests) is indeterminate.

The BU-63705 configuration disables both broadcast mode and dynamic bus control.

2.2.1 Command Interface

Commands, listed below, arrive via the 1553 Bus. Since each command type is directed to a unique 1553 bus subaddress, each is allocated its own 1553 bus message. CDC prelatches the command word based on the word-count and subaddress output by the BU-63705. The headers and BU-63705 error flags are not monitored. CDC just strips the data word(s) relevant to each command type, and preloads them in expectation of the GBR (Good Block Received, status signal from BU-63705) strobe. Command reception is not finalized unless a GBR assertion follows

the actual command. This insures that the 1553-bus transmission has passed the BU-63705's internal error checking.

In a multibit field, the MSB is the highest numbered bit. Since the CCSDS convention is to number the MSB as 0, the field positions in this document may not be identical to those in the Spacecraft to CRaTER Data ICD.

Commands, identified by 1553 Bus subaddress, are defined below:

Sub-Address	Bits[a]	Command Type	Description
0x00	-	*Reserved*	not used
0x01	64	Next Time Value	D[62:32] - 31 bit value loaded into the seconds register (bit 63 is not used) D[31:28] - 4 bit value loaded into the subseconds register NOTE: Although a full 32 bits subseconds field is transmitted, only the upper 4 MSBs are implemented (lower 28 bits of subseconds are not used by CRaTER). Similarly, since only 31 bits of the seconds count is used; the MSBit is discarded.
0x02	16	Command Echo	D[15:0] - CMDECHO[15:0] This register is used to echo command reception into the secondary science telemetry packets. The register itself has no effect during normal operation; during "Testmode", Bits[3:0] are used to select the test type.
0x03	16	Discrete Commands	D[15:14] - not used D[13] - 1 -> Turn Detector Bias Off; (0 has no effect) (Default) D[12] - 1 -> Turn Detector Bias On; (0 has no effect) D[11] - 1-> Turn ECAL Low Range Off; (0 has no effect) (Default) D[10] - 1-> Turn ECAL Low Range On; (0 has no effect) D[9] - 1-> Turn ECAL High Range Off; (0 has no effect) (Default) D[8] - 1-> Turn ECAL High Range On; (0 has no effect) D[7] - 1-> Set ECAL Rate to 8Hz; (0 has no effect) (Default) D[6] - 1-> Set ECAL Rate to 2KHz; (0 has no effect) D[5] - not used D[4] - 1 -> Sets Data Test Mode; 0-> Clrs Data Test Mode (Default = 0) D[3:2] - not used D[1] - CLEAR - Initializes all commands to their default values D[0] - RESET - Causes a pulse reset to all CDC subsystems, except the command interface itself & the Source Sequence Counts NOTE: CLEAR and RESET take precedence over all other Discrete Command fields.
0x04	16	Detector Enables	D[15] - 1 -> Turn D1 Processing Off; (0 has no effect) D[14] - 1 -> Turn D1 Processing On; (0 has no effect) (Default) D[13] - 1 -> Turn D2 Processing Off; (0 has no effect) D[12] - 1 -> Turn D2 Processing On; (0 has no effect) (Default) D[11] - 1 -> Turn D3 Processing Off; (0 has no effect) D[10] - 1 -> Turn D3 Processing On; (0 has no effect) (Default) D[9] - 1 -> Turn D4 Processing Off; (0 has no effect) D[8] - 1 -> Turn D4 Processing On; (0 has no effect) (Default) D[7] - 1 -> Turn D5 Processing Off; (0 has no effect) D[6] - 1 -> Turn D5 Processing On; (0 has no effect) (Default) D[5] - 1 -> Turn D6 Processing Off; (0 has no effect) D[4] - 1 -> Turn D6 Processing On; (0 has no effect) (Default) D[3:0] - not used
0x05	64	Discriminator Accept Mask	D[63:0] - sets 64 bit value configuring the event accept criteria (based on the active LLDs). NOTE: Bit 0, a degenerate case, is not used. (Default = 0xFFFFFFFF)
0x06	16	Event Amplitude Discriminator - Thin Detectors	D[15:8] - not used D[7:0] - sets Low Level Discriminator (LLD) 8-bit register (Default = 0x80)

Sub-Address	Bits[a]	Command Type	Description
0x07	16	Event Amplitude Discriminator - Thick Detectors	D[15:8] - not used D[7:0] - sets Low Level Discriminator (LLD) 8-bit register (Default = 0x80)
0x08	16	Electrical Cal Amplitude	D[15:8] - not used D[7:0] - sets Electrical Cal (Test Pulser DC output) (Default = 0x00)
0x09 - 0x1F	--	*not used*	

a. Multiword 1553 bus messages are interpreted as follows: Word0: Bits[63:48]; Word1: Bits[47:32]; Word2: Bits[31:16]; Word3: Bits[15:0]. Word0 is the first message word received (corresponding to a "word count" value of 0).

The Discrete Command and Detector Enable Registers primarily consist of "Radio Buttons". Setting one bit of a two-bit group causes the control bit to be selectively turned on or off. If both bits of the group are zero (a no-op) or if both bits are one (an error condition), no action is taken. Multiple groups may be set or cleared simultaneously (i.e. using one 1553 bus message).

Setting the Bias Voltage On results in the application of an intermediate voltage to the detectors at the next one second tick. The full bias voltage is applied at the following one second tick. (This two step process avoids any bias overshoot in the turn-on process.) Setting the Detector Bias Off clears the Bias Voltage at the next one second tick. The Bias Voltage is cleared immediately if the 5V analog supply is not present (see "Analog Voltage Monitor" on page 15) or in response to a RESET or CLEAR command (see below).

Upon reception, most commands are latched into holding registers that are transferred to the active command bus at the next 1-Second Tick. Exceptions are RESET and CLEAR, which take effect immediately.

The system is required to accept only one command per second in addition to the "Time of Next Sync Pulse" command. However, there is nothing in the hardware that prevents the reception of multiple commands/second. The data and subaddress of the last command received during the previous second (excluding the "Time of Next Sync Pulse" command) are echoed in the secondary science packet (see Section 2.2.3.1 on page 9). In the absence of a command to Subaddresses 2 through 8 during the previous second, these fields are held at zero.

2.2.2 1553 Telemetry Interface

There are three types of telemetry packets transmitted via the 1553 bus: Housekeeping, Secondary Science and Primary Science. The Bus Controller (Spacecraft) retrieves Housekeeping and Secondary Science telemetry packets in the interval between 100 and 900 milliseconds following TK1S. Secondary Science Packets are requested every 1 second and Housekeeping Packets are requested every 16 seconds. The hardware, however, does not place any restriction on the message retrieval frequency. Primary science packets (which straddle seven 1553 bus messages) can be retrieved anytime relative to the one second clock.

Upon request, packet data is supplied as follows: the first three 16-bit words are the Primary Header; the next three words are the secondary header. The data is shown as it would appear on the bus connecting the CDC to the 1553 Protocol Chip. Thus the MSB is shown as the field that is shifted out first. In this document, within each field the MSB appears on the left.

Primary Science is retrieved as messages from RT-Subaddresses 0x0A through 0x11 (10-17 dec.) (see Section 2.8 on page 14 for more detail); secondary science from RT-Subaddress 0x14 (20 dec.) and Housekeeping from RT-Subaddress 0x15 (21 dec.)

2.2.3 Telemetry Header Formats

Both headers (primary and secondary), described in Reference 1, are summarized below:

WORD ADDR	WORD TYPE	WORD VALUE (in HEX)
0000	Primary Header - Word 0 D[15:13] - Version Number (0) D[12] - Type (Telemetry->0) D[11] - Secondary Header Flag (1) D[10:0] - Application Process ID Primary Science: 0x78 (120 dec) Secondary Science: 0x79 (121 dec) Housekeeping: 0x7A (122 dec)	Primary Sci: 0878 Secondary Sci: 0879 Housekeeping: 087A
0001	Primary Header - Word 1 D[15:14] - Segmentation Flags (both always equal 1) D[13:0] - Source Sequence Count	SSCNT[13:0] - each packet type maintains its own source sequence counter (cleared by PowerOn only) (Bits 15 & 14 are always set)
0002	Primary Header - Word 2 D[15:0]- (Packet Length - 1) (in bytes) including secondary header, but excluding primary header. This amounts to 20 words (40 bytes) for secondary science packets and 29 words (58 bytes) for housekeeping Primary Science Packets vary depending on the number of event words remaining in the transmission queue.	Primary Sci: 0005 - 01B5 Secondary Sci: 0027 Housekeeping: 0039
0003	Secondary Header - Word 0 D[15] - always 0 D[14:0] - Seconds[30:16] - upper half	0, SECCNTH[14:0] Value sent by the S/C during the previous second
0004	Secondary Header - Word 1 D[15:0]- Seconds Count - lower half	SECCNTL[15:0] Value sent by the S/C during the previous second
0005	Secondary Header - Word 2 D[15:12]- SubSeconds Count - upper nibble D[11:7] - not used (= 0) D[6] - Test Mode - 1 if configured for test mode D[5] - Internal Clock Mode: 1 if internal timer used to generate last TK1S; 0 if S/C 1 Hz clock present. D[4:0] Instrument Serial Number	(15:12),(11:7),(6),(5),(4:0) SSEC Null TstMd IntCk ISer Subseconds: Value sent by the S/C during the previous second.

If no time command has been received from the S/C during the previous second, the Seconds and Subseconds count fields = all zeros.

2.2.3.1 Secondary Science Application Data

Application data follows the 6-word header (shown above) as follows:

WORD ADDR (Hex)	WORD ADDR (Dec)	WORD CONTENT
06	6	D[15] - Bias Voltage Delayed Control D[14] - Bias Voltage Enable (On = 1) D[13] - ECAL Low Range (On = 1) D[12] - ECAL High Range (On = 1) D[11] - ECAL High Rate (On => 2KHz = 1) D[10:5] - DETENB[1:6] Enb D[4:0] - RT Subaddress of last command
07	7	D[15:0] - Contents of Last Command
08	8	D[7:0]- Event Amp Disc Setting: D1, D3, D5 (Thin)
09	9	D[7:0]- Event Amp Disc Setting: D2, D4, D6 (Thick)
0A	10	D[15:0]- Disc Accept Mask[63:48]
0B	11	D[15:0]- Disc Accept Mask[47:32]
0C	12	D[15:0]- Disc Accept Mask[31:16]
0D	13	D[15:0]- Disc Accept Mask[15:0]
0E	14	D[15:0]- Det_D1 Singles Counter[15:0]
0F	15	D[15:0]- Det_D2 Singles Counter[15:0]
10	16	D[15:0]- Det_D3 Singles Counter[15:0]
11	17	D[15:0]- Det_D4 Singles Counter[15:0]
12	18	D[15:0]- Det_D5 Singles Counter[15:0]
13	19	D[15:0]- Det_D6 Singles Counter[15:0]
14	20	D[15:0]- Good Event Counter[15:0]
15	21	D[15:0]- Event Reject Counter[15:0]
16	22	D[15:0]- Total Event Counter[15:0]

Data sent in the secondary science packet is latched on TK1S, and reflects system settings/behavior during the previous data interface. The “Last Command” and corresponding “RT SubAddr” are non-zero only if a command was received during that data interval.

2.2.4 Housekeeping Application Data

Application data follows the 6-word header (shown above) as follows (unused bits are set to zero):

WORD ADDR (Hex)	WORD ADDR (Dec)	WORD CONTENT	Comments
06	6	D[11:0] - 28V Monitor D[15:12] - FPGA Revision	AMUX Addr: 2
07	7	D[11:0] - 5V Digital Monitor	AMUX Addr: 1
08	8	D[11:0] - +5V Analog Monitor D[15:12] - 0xF when analog voltage is not present (AVMON = 0), otherwise these bits are set to zero.	AMUX Addr: 0
09	9	D[11:0] - -5V Analog Monitor	AMUX Addr: 3
0A	10	D[11:0] - 28V Current Monitor (= VREF (2.5V Internal Ref) for the first CRaTER Board (serial number 8))	AMUX Addr: 8
0B	11	D[11:0] - Det_D1 Bias Current Monitor	AMUX Addr: 16
0C	12	D[11:0] - Det_D2 Bias Current Monitor	AMUX Addr: 17
0D	13	D[11:0] - Det_D3 Bias Current Monitor	AMUX Addr: 18
0E	14	D[11:0] - Det_D4 Bias Current Monitor	AMUX Addr: 19
0F	15	D[11:0] - Det_D5 Bias Current Monitor	AMUX Addr: 20
10	16	D[11:0] - Det_D6 Bias Current Monitor	AMUX Addr: 21
11	17	D[11:0] - Thin Det Bias Voltage Monitor	AMUX Addr: 14
12	18	D[11:0] - Thick Det Bias Voltage Monitor	AMUX Addr: 15
13	19	D[11:0] - ECAL Amplitude Monitor	AMUX Addr: 25
14	20	D[11:0] - Thin Det LLD Voltage Monitor	AMUX Addr: 10
15	21	D[11:0] - Thick Det LLD Voltage Monitor	AMUX Addr: 11
16	22	D[11:0] - Telescope Temperature	AMUX Addr: 27
17	23	D[11:0] - Analog Board Temperature	AMUX Addr: 26
18	24	D[11:0] - Digital Board Temperature	AMUX Addr: 5
19	25	D[11:0] - Power Supply Temperature	AMUX Addr: 6
1A	26	D[11:0] - Bulkhead Reference Temperature	AMUX Addr: 7
1B	27	D[11:0] - TDMON1	AMUX Addr: 22
1C	28	D[11:0] - TDMON2	AMUX Addr: 23
1D	29	D[11:0] - TDMON3	AMUX Addr: 24
1E	30	D[11:0] - PRT Reference	AMUX Addr: 4 (Ground Test Only)
1F	31	D[11:0] - Purge Flow Rate	AMUX Addr: 9 (Ground Test Only)

2.2.5 Primary Science Application Data

Primary Science application data consists of a stream of events. Each event consists of nine bytes, packetized in the following order:

Byte #	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	DET1-11	DET1-10	DET1-9	DET1-8	DET1-7	DET1-6	DET1-5	DET1-4
1	DET1-3	DET1-2	DET1-1	DET1-0	DET2-11	DET2-10	DET2-9	DET2-8
2	DET2-7	DET2-6	DET2-5	DET2-4	DET2-3	DET2-2	DET2-1	DET2-0
3	DET3-11	DET3-10	DET3-9	DET3-8	DET3-7	DET3-6	DET3-5	DET3-4
4	DET3-3	DET3-2	DET3-1	DET3-0	DET4-11	DET4-10	DET4-9	DET4-8
5	DET4-7	DET4-6	DET4-5	DET4-4	DET4-3	DET4-2	DET4-1	DET4-0
6	DET5-11	DET5-10	DET5-9	DET5-8	DET5-7	DET5-6	DET5-5	DET5-4
7	DET5-3	DET5-2	DET5-1	DET5-0	DET6-11	DET6-10	DET6-9	DET6-8
8	DET6-7	DET6-6	DET6-5	DET6-4	DET6-3	DET6-2	DET6-1	DET6-0

The application data segment, therefore, is always a multiple of the nine bytes. The maximum Primary Science Packet size is 444 bytes (6 bytes primary header, 6 bytes secondary header + 432 bytes of data), but in some cases smaller packets (down to the “no data” case of 12 bytes) are generated. Primary science data packetizing and control is detailed in Section 2.8 on page 14.

The 16-bit word forwarded to the 1553 I/F is formed with Byte 0 in the most significant position (bits 15:8) with byte 1 to the right (=> DET1-11 is the first bit transmitted on the serial 1553 Bus).

2.3 Housekeeping Data Controller

The housekeeping data controller is “awakened” by TK1S, at which time it activates the housekeeping ADCs and converts/reads all the analog channels, placing the results in 12-bit registers. Each measurement is converted 32 times (ADC conversions separated by 1.026ms) and accumulated. The average of these 32 readings is transferred into a 12-bit holding register, forwarded to the telemetry subsystem. Upon completion of each averaged measurement, the analog mux address is incremented. The next housekeeping channel measurement takes place 4ms following the mux address increment, which gives a period of 35.9ms between channel switches.

There are two housekeeping ADCs, resulting in a total collection time is approximately 570ms. Since data might be read out at anytime during the collection process, a value acquired by the Spacecraft may not reflect the most recent second, but will always be accurate to within 2 seconds.

2.4 Test Pulser Interface

Two timing pulses are forwarded to the Analog Board. One frequency control (command I/F: ECAL Rate) causes both pulses to operate at either the high (period = 512μs) or low (period = 131ms) rate. The Pulse Width is 128μs. Each pulse can be independently enabled (command I/F: ECAL High/Low On/Off). When disabled, the pulse output is held at logic one.

Additionally an “Electrical Cal Amplitude” voltage is generated by converting a Pulse Width Modulated (PWM) FPGA output to a DC voltage. The amplitude, set via the 8-bit command I/F register, ranges from 0 to approximately 4V-DC. (Default is 0x00 => 0V.)

PWM Operation: The PWM subsystem produces a bit stream that operates at 1MHz. The number of “high” bits is determined by the “DAC” register value. At the zero setting, the PWM output of the FPGA is always low. A setting of one results in a PWM output that is low for 255µs, and high for 1µs. At the 0x80 (halfway) setting, the PWM output produces a square wave (128µs high + 128µs low). At the 0xFF setting (full-scale), the PWM output is high for 255µs, and low for 1µs.

2.5 LLD Threshold Levels

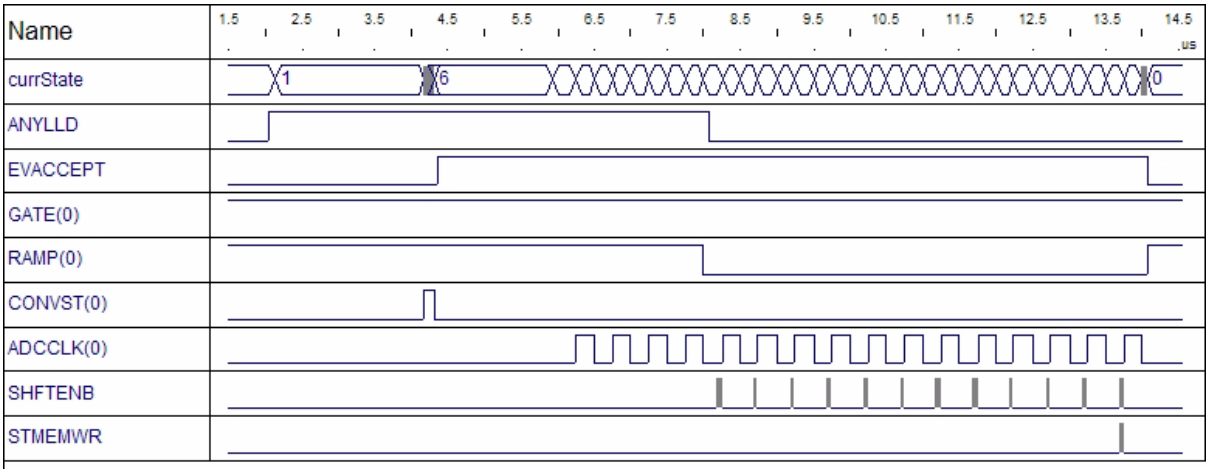
Two Low Level Discriminator (LLD) threshold voltages are generated by converting Pulse Width Modulated FPGA outputs to a DC voltages. The amplitude, set via the 8-bit command I/F registers, ranges from -0.047 to 0.141 V-DC. The Event Amplitude Discriminator - Thin Detector setting drives the detector 1, 3 and 5 comparators; the Event Amplitude Discriminator - Thick Detector drives the detector 2, 4 and 6 comparators. (Default setting for both LLD thresholds: 0x80 => 0.047V.) (See paragraph above, in Section 2.4, for a description of the PWM operation.)

2.6 Event Processing

Events arrive from the AE subsystem, six independent analog signals (Range: 0 - +3.0V, Peaking Time: 1µs +/- 20%), each received by a Peak-Hold Detector. The output of the Peak-Hold Detector is routed to both a comparator and an A/D converter (12 bits). The comparator outputs a “DetTrig” output per slice indicating whether the detector signal has crossed its preset LLD threshold (see Section 2.5).

Detectors can be selectively disabled (see “Detector Enables” register set via Command). Disabling a detector inhibits its ability to trigger event collection; the disabled chain energy, however, is still converted should an active chain cause an event.

Upon detection that any LLD threshold has triggered, the event handler activates. The sequencer actions, upon event detection, are shown below:



“ANYLLD” (comparator output of an enabled chain) causes the system to enter an event processing sequence. The “GATE” signal (which controls the passage of the signal from the Peak-

Hold Detector input) is no longer used. The “RAMP” signal discharges the Peak-Hold Detector. (The A/D samples, locking the signal in, at the falling edge of the second ADCCLK.)

An event is converted and written into memory if it passes the Discriminator Accept Mask test, which operates as follows: The Discriminator Accept Mask is a 64x1 bit memory (set by Command) that serves as a look-up table. Every event produces a 6-bit address formed by the Detector Triggers (LLD crossings). (Detector 6 is the most significant and Detector 1 is the least significant address bit.) If the Discriminator Accept Mask bit corresponding to the event is set, the EVACCEPT signal asserts. The LLD crossings are locked in at the end of “State 6” in the timing diagram shown above. The Discriminator Accept Mask is therefore based on the LLD crossings 4μs after the event trigger, and 2μs prior to the RAMP (Peak-Hold Detector discharge). Assertion of EVACCEPT triggers the 9-byte event write (Section 2.2.5 details the 9-byte event record) following A/D conversion.

As can be seen, total event processing time is approximately 12μs. Subsequent events may be registered when the RAMP signal returns to the logic high state (approximately 12μs after an event processing cycle begins). Secondary events that occur prior to this point may be missed. These missed events, however, may be registered by the “Singles Counters” (see below). The 12μs window applies whether an event is accepted or rejected, resulting in a deterministic “dead-time” that can be derived from the Total Event Count.

2.7 Event Counters

Event counters, detailed below, are all 16-bit counters that “freeze” at the maximum count until reset. Every second (upon TK1S) the current-count value is transferred to a holding register (which is inserted into the Secondary Science Telemetry) and the counter is cleared.

2.7.1 Event Reject Counter

A 16-bit counter is clocked every time an event is rejected by the Discriminator Accept Mask test.

2.7.2 Total Event Counter

A 16-bit counter is clocked every time an event is processed. This includes rejected events, events written into memory, as well as accepted events that aren’t written (due to buffer overflow).

2.7.3 Good Event Counter

A 16-bit counter which is clocked every time an qualifying event is processed. This counter is clocked for all events, even if they are not written into SRAM (due to buffer overflow) or read-out of SRAM the following second (telemetry overflow).

2.7.4 Singles Counter(s)

For each detector: a 16-bit counter which is clocked by the “Singles Count” signals received from the AE subsystem. Since these inputs are asynchronous, they are sampled and filtered. Singles “incidents” with pulse widths < approximately 200ns may not be recognized.

2.8 Primary Science Packet Generation

Event writes and primary science telemetry reads share a common memory (32Kx8 SRAM). This EV-SRAM is split into two buffers (determined by the most significant address bit), with one buffer always allocated to event writes, the other to telemetry reads. The buffer select is toggled every second, so that events written during the Nth second are read-out during the (N+1)th second

The “Event Write” subsystem requests EV-SRAM (for 9-byte writes) whenever a qualified event has been converted (assuming that the buffer hasn’t overflowed) and tracks the buffer address. When a buffer swap occurs (at the TK1S or the first opportunity following an event group write after a TK1S), the Nth memory pointer is latched and passed to the “Telemetry Read” subsystem. This is used to generate the packet size in the CCSDS header, as well as to control how many Primary Science packets are supplied during the (N+1)th second.

The Telemetry Read subsystem, responsible for header generation, requests words (2 bytes at a time) from the SRAM Controller on an as-needed basis. Words are read in advance: the first word-read is initiated by a buffer-swap -- subsequent reads occur as the telemetry I/F transmits the previous word. When the buffer empties, the data is zero-filled.

The S/C provides eight RT-Subaddresses for the reading of Primary Science. Address 0x0A (corresponding to block 0) signifies the start of a message, and generates a CCSDS header if either of the following conditions are met: (1) this is the first RT-Addr 0x0A message requested following a one-second tick or (2) there is event data remaining in the Ev-Read Buffer. Addresses 0x0B through 0x10 (corresponding to blocks 1 through 6) always read out the next event word if there is one remaining, or zero if the Ev-Read Buffer is empty. RT-Addr 0x11 (block end flag) has no effect, and returns one word of diagnostic data (i.e. the telemetry buffer read pointer).

To allow for operation in “Internal Clock Mode” (1553 bus reads may be asynchronous to the 1Hz tick) the Telemetry Buffer swap mechanism has a certain amount of “elasticity”. The read buffer swaps when a “Start of Packet” (read from RT-Addr 0x0A) is detected, while the write buffer swaps just after the 1 Hz tick. In same cases, therefore, the read and write pointers access the same SRAM buffer. During these transition states, in the unlikely event that the write pointer catches up to the read pointer, the telemetered data is “zero-filled” for the remainder of the packet.

2.9 Test Mode

Test Mode is used to exercise/verify the on-board Static RAM.

Setting the “Data Test Mode” bit of the Discrete Commands Register invokes Test Mode. When in test mode, all systems operate nominally, except for the event reception circuitry. The Detector Triggers are ignored. SRAM is written every second according to the following settings of the CMDECHO[3:0] field:

CMDECHO[3:0]	SRAM Data
0	all 0xAA
1	all 0x55
2	all 0xFF
3	all 0x00
4	alternating 0xAA and 0x55
5	alternating 0x00 and 0xFF

CMDECHO[3:0]	SRAM Data
6	data <= address
7	data <= not(address)
8-15	continuously circulate through all eight patterns - test number is incremented every two seconds.

Buffering and memory readout is exactly the same during test mode as it is during normal operation. (Data must be verified via the primary science 1553 bus interface.) Operation during one second fills half of the 32K SRAM memory space; each second toggles writes between the two halves of SRAM. As long is testmode is set, the selected data patterns are written to SRAM following each buffer swap.

2.10 Analog Voltage Monitor

An FPGA input (AVMON) is connected to the analog +5V supply via a voltage divider, resulting in a signal that is a solid logic high when the analog +5V is present. This signal, sampled and filtered, is used to gate the outputs/activity of those subsystems that appear at the interfaces between the two power domains. The following actions are taken if the AVMON is low:

- RAMP and GATE outputs to the Peak and Hold Detectors are held at 0 V.
- CONVST and ADCCLK (normally low) are kept at 0 V.
- Analog Housekeeping is suppressed.
- The Detector Trigger input latches are held in a reset state (which holds event processing in a dormant state).
- The Pulse Width Modulator outputs are held at 0V.
- Bias Voltage Enable and Control are deasserted. The Bias Voltage will stay off until explicitly commanded on after the analog +5V has been restored (AVMON = 1).

When AVMON=0, the upper nibble of the +5V analog housekeeping will read as all ones. All other Housekeeping Values “stick” at the last value read when the analog +5V was present.

The analog voltage monitor subsystem is inactive following a power-on reset. It samples AVMON at the one-second tick, and enters an active state upon the detection of two consecutive assertions of (AVMON AND TK1S). Similarly, if the monitor reverts to an inactive state (due to an analog voltage drop-out), two instances of (AVMON AND TK1S) are required to restore activity.