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Lunar Reconnaissance Orbiter Project

Field Programmable Gate Array Review Plan

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National Aeronautics and Space Administration

Goddard Space Flight Center
Greenbelt, Maryland

CM FOREWORD

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Questions or comments concerning this document should be addressed to:

LRO Configuration Management Office
Mail Stop 431
Goddard Space Flight Center
Greenbelt, Maryland 20771

Signature Page

Prepared by:

Philip J. Luers LRO Avionics Systems Engineer GSFC/561	Date

Reviewed by:

David Everett Mission Systems Engineer GSFC / Code 599	Date	Michael Pryzby Spacecraft Systems Engineer Swales / Code 431	Date

Approved by:

Craig Tooley Project Manager GSFC / Code 431	Date

LUNAR RECONNAISSANCE ORBITER PROJECT

DOCUMENT CHANGE RECORD

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REV LEVEL	DESCRIPTION OF CHANGE	APPROVED BY	DATE APPROVED

List of TBDs/TBRs

Item No.	Location	Summary	Ind./Org.	Due Date

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1.0 INTRODUCTION

1.1 PURPOSE

The purpose of this plan is to ensure that each Field Programmable Gate Array (FPGA) developed and designed for LRO is reviewed thoroughly and consistently. This document establishes a methodology for having independent reviewers, holding specific meetings at a minimum, and content of presentations in an effort to avoid known pitfalls of designing with FPGAs on LRO. It is the responsibility of the Product Design Lead (PDL) to ensure that these reviews and meetings are held at an appropriate phase of development to provide the most insight, while ensuring that there is time available to resolve any issues uncovered during the reviews.

1.2 SCOPE

This plan applies to the in-house development of FPGAs for the LRO Command and Data Handling (C&DH), Power System Electronics (PSE), Demisable Integrated Reaction Wheel Assembly (DIRWA), and Propulsion Deployment Electronics (PDE) subsystems.

This plan may optionally be applied to the development of FPGAs for the LRO instruments, at the discretion of the LRO Payload Manager.

This plan may optionally be applied to the development of FPGAs within procured items, at the discretion of the subsystem PDL.

1.3 DEFINITIONS AND TERMINOLOGY

In this document, a requirement is identified by “shall”, a good practice by “should”, permission by “may”, or “can”, expectation by “will”, and descriptive material by “is”.

2.0 DOCUMENTATION

2.1 APPLICABLE DOCUMENTS

None

2.2 REFERENCE DOCUMENTS

431-RVW-000694 LRO FPGA Review Checklist

3.0 PEER REVIEW

3.1 PEER REVIEW OVERVIEW

The goal for the peer review is for the FPGA design engineer to demonstrate to the review panel that the design meets all its requirements, has been designed properly, and all analyses and simulations have been performed to verify it will work in the intended application, over the temperature range and for the life of the mission.

The PDL will be responsible for insuring that every single FPGA design under his purview is peer reviewed. He will each review in coordination with the LRO Avionics Systems Engineer, the Electrical Engineering Division (EED) person responsible for this function, or the EED Chief Engineer if applicable. Together they will select a peer review panel. The panel should include at least:

- One FPGA designer from outside the project, who will serve as the chairperson for the review team, with experience using the same part type.
- One FPGA designer from the project, preferably one who designs a chip interfacing with the one being reviewed.
- Other reviewers as needed, as described below.

Due to the nature of FPGA devices, the review process will involve other engineers to verify relevant aspects of the design. This group will normally include:

- All owners of requirements that are flowed down must review the FPGA requirements.
- The board-level designer and box lead must review all interfaces.
- Software engineers must review the functional interfaces and test requirements.
- Printed Wiring Board designers must review requirements relevant to layout.
- Thermal engineers should be advised as to expected power dissipation.

The Peer Review will be held in several stages including, but not limited to:

- Initial Meeting – Requirements, Design Overview, Interfaces, Implementation, Analysis Results
- Independent Analysis – Individual Reviewers will independently review aspects of the design
- Final Peer Review Meeting – Review Chairperson will communicate summary of issues, resolutions, and any Requests For Actions (RFAs) generated
- End of Peer Review

The FPGA Peer Review will use the FPGA Review Checklist (431-RVW-000694) to verify that all materials have been presented and adequately reviewed.

3.2 PEER REVIEW PREPARATION

The FPGA Design Engineer will bring to the Initial Peer Review Meeting:

- Printed copies of VHDL code (4 copies)
- Requirements and Specifications Documentation (4 copies)
- Testing and Verification Documentation (4 copies)
- Compact Disk with all code, synthesis, and place and route files, testbenches, fuse maps, Actel Databases (ADB) and other results files (4 copies)
- Computer to show simulations and analysis as needed

3.3 FPGA PEER REVIEW CHECKLIST

The panel will use the LRO FPGA Review Checklist (431-RVW-000694) to verify that the following items have been addressed:

- Requirements are met
- Simulations successfully completed for 4 conditions:
    - Best Case Beginning of Life (BCBOL)
    - Worst Case Beginning of Life (WCBOL)
    - Best Case End of Life (BCEOL)
    - Worst Case End of Life (WCEOL)
- Simulation adequately tests design (tests all sections of code and circuitry)
- Timing analysis completed successfully
- Resets handled properly
- Clocking handled properly
- Input/Output (I/O) pins properly selected (Simultaneously Switching Outputs (SSOs), levels, slew rates, etc.)
- Relevant manufacturer recommendations and app notes followed
- Asynchronous circuits clearly identified and analyzed for robust operation
- Board-level issues addressed (decoupling, routing, signal integrity, etc.)
- Margins have been demonstrated and are acceptable (timing, utilization)
- Other relevant issues

- Reviewer issues satisfied

3.4 INITIAL PEER REVIEW MEETING

At the Initial Peer Review Meeting, the FPGA Design Engineer shall present the following to the panel:

- Applicable Documents
    - Requirements, Specifications, Application Notes, Design Guidelines, Coding Guidelines
- Requirements Review.
    - Summary of Critical Requirements
- Design Overview.
    - Block Diagram of where FPGA fits in board/system
    - Block Diagram of FPGA
        - General description of device
        - Description of external interfaces
    - Clocking
        - Draw tree from oscillator source
        - Resources used, why and where
    - Reset
        - Draw tree from source
        - Show synchronization circuit as synthesized
    - Block Diagram of each section
        - Highlight clocks used
        - Show interfaces
        - Explain any State Machine implementations with state diagrams
    - Synchronization
        - Show how signals are synchronized over clock boundaries

        - Any time there is a signal crossing within the FPGA, entering the FPGA, and being sampled by a local clock

- Interface Descriptions. Discuss timing/ functionality of external interfaces.
- Code Structure – include block diagrams.
- Code Walkthrough – Discuss:
    - Reset handling
    - How illegal states in each Finite State Machine (FSM) are handled
    - Use of global vs. routed clock signals
    - Clock boundary signal resynchronization
- Implementation discussion:
    - Pinouts
    - I/O Selection
    - External clocks (draw clock tree for each oscillator)
    - Clocking(rates, routing resources)
    - Reset (source, location, duration)
    - Utilization percentage
- Verification
    - Discuss overall verification methods
    - Test Plan – Walk through test procedure document and test sequence flowchart.
- Functional Simulation – Dynamic Timing
    - List simulation files, including data and output files
    - Simulations with Standard Delay Format (SDF) (use 100 Kilorads, best and worst case)
- Static Timing
    - Show timing spreadsheet – be prepared to show how numbers were obtained
- Synthesis

  - Include constraint files if used
  - Explain any remaining warnings
  - Discuss attributes and directives used
- Place and Route
  - Include all input files
- Present results:
  - Simulation results
  - Timing Analysis. Show how margins are met
  - Interface Analysis (drive strengths, I/O levels, power supply levels, sampling of input signals, no bus left floating)
  - Board Implementation (power supply decoupling, signal integrity analysis, routing)
  - Synplify Report
    - Include a copy of .srr synthesis results file
    - Discuss any warnings listed
  - Actel Designer Reports
    - Timing Report
    - Pin Report
    - Status Report
    - Flip-Flop Report
  - Tool versions
    - List versions of all software used from Synplicity, Actel, Modelsim, and any others
  - Conclusions
    - Known issues, liens against the review
- Hand off CD with design package to the peer review team, all materials presented at the Initial Meeting including:

- Code
- Test Code
- Documents – board-level review charts
- List of design tools and version numbers
- Constraint files
- Vendor tool output files
- Anything else needed to understand and test the design

3.5 INDEPENDENT ANALYSIS

Individual reviewers independently review design aspect assigned to them by the chairman of the peer review team. This step will accomplish:

- Review of the schematics/code
- Review board implementation, including results of signal integrity analysis
- Verify critical interfaces and implementation details
- As needed, run simulations of critical sections of the design
- Develop questions and comments (informal RFA's) and communicate them to the other review team members for their consideration. The communication at this point can be via email or alternate agreed upon method.
- Each reviewer submits to the chairman his assessment of the review using the FPGA Review Checklist Form (431-RVW-000694)
- The chairperson ensures that all reviewers are satisfied that the flight implementation will work

3.6 FINAL PEER REVIEW MEETING

At the Final Peer Review meeting, held between the design team and the peer review panel members, the review chairperson will communicate the following:

- A summary of the issues that arose during review process and their resolutions
- The results of the peer review
- Any Requests for Action (RFA's) generated during the review
- Proposed plan for the resolution of open RFA's

3.7 END OF PEER REVIEW

Once all open issues are resolved, the chairperson will provide the PDL with:

- A memorandum indicating that the design has been successfully reviewed and is acceptable for flight
- A signed copy of the LRO FPGA Review Checklist Form (431-RVW-000694)

Appendix A. Abbreviations and Acronyms

Abbreviation/ Acronym	DEFINITION
ADB	Actel Databases
BCBOL	Best Case Beginning of Life
BCEOL	Best Case End of Life
C&DH	Command and Data Handling
CCB	Configuration Control Board
CM	Configuration Management
CMO	CM Office
DIRWA	Demisable Integrated Reaction Wheel Assembly
EED	Electrical Engineering Division
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
I/O	Input/Output
LRO	Lunar Reconnaissance Orbiter
PDE	Propulsion Deployment Electronics
PDL	Product Design Lead
PSE	Power System Electronics
RFA	Requests For Action
SDF	Standard Delay Format
SSO	Simultaneously Switching Outputs
VHDL	VHSIC Hardware Description Language
VHSIC	Very-High-Speed Integrated Circuit
WCBOL	Worst Case Beginning of Life
WCEOL	Worst Case End of Life