HARRIS SEMICONDUCTOR

HS-26C32RH

Radiation Hardened Quad Differential Line Receiver

August 1995

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total Dose Up to 300K RAD (Si)
- Latchup Free
- EIA RS-422 Compatible Outputs
- CMOS Compatible Inputs
- Input Fail Safe Circuitry
- High Impedance Inputs when Disabled or Powered Down
- Low Power Dissipation 138mW Standby (Max)
- Single 5V Supply
- Full -55°C to +125°C Military Temperature Range

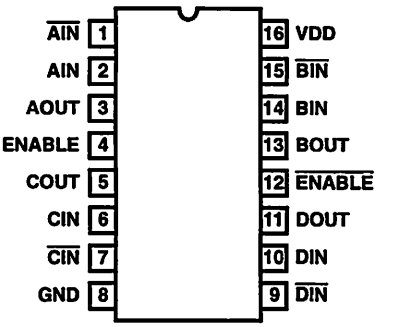
Description

The Harris HS-26C32RH is a differential line receiver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

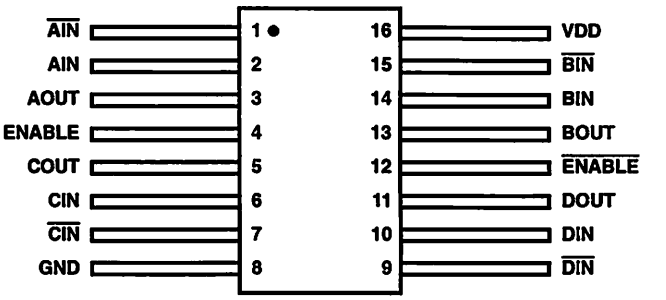
The HS-26C32RH has an input sensitivity typically of 200mV over the common mode input voltage range of ±7V. The receivers are also equipped with input fail safe circuitry, which causes the outputs to go to a logic "1" when the inputs are open. Enable and Disable functions are common to all four

Pinouts

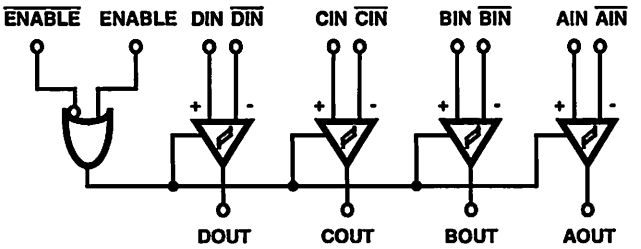
HS1-26C32RH 16 LEAD CERAMIC SIDEBRAZE DIP
MIL-STD-1835: CDIP2-T16
TOP VIEW



HS9-26C32RH 16 LEAD FLATPACK
MIL-STD-1835: CDFP4-F16
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT
	ENABLE	$\overline{\text{ENABLE}}$	INPUT	OUT
ON	0	1	X	HI-Z
ON	1	X	VID ≥ VTH (Max)	1
ON	1	X	VID ≤ VTH (Min)	0
ON	X	0	VID ≥ VTH (Max)	1
ON	X	0	VID ≤ VTH (Min)	0
ON	1	X	Open	1
ON	X	0	Open	1

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HS1-26C32RH-8	-55°C to +125°C	Harris Class B Equivalent	16 Lead Sideboard DIP
HS1-26C32RH-Q	-55°C to +125°C	Harris Class S Equivalent	16 Lead Sideboard DIP
HS9-26C32RH-8	-55°C to +125°C	Harris Class B Equivalent	16 Lead Flatpack
HS9-26C32RH-Q	-55°C to +125°C	Harris Class S Equivalent	16 Lead Flatpack
HS1-26C32RH/Sample	+25°C	Sample	16 Lead Sideboard DIP
HS1-26C32RH/Proto	-55°C to +125°C	Prototype	16 Lead Sideboard DIP
HS9-26C32RH/Sample	+25°C	Sample	16 Lead Flatpack
HS9-26C32RH/Proto	-55°C to +125°C	Prototype	16 Lead Flatpack

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

Spec Number 518790
File Number 3402.2

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Differential Input Voltage ..... ±12V
Common Mode Range ..... ±12V
Enable Pins Input Voltage ..... -0.5V to VDD+0.5V
DC Drain Current (Any One Output) ..... ±25mA
DC Diode Input Current Enable Pin ..... ±1µA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C
ESD Classification ..... Class 1

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	80°C/W	20°C/W
Ceramic Flatpack Package	103°C/W	26°C/W

Maximum Package Power Dissipation at +125°C
SBDIP Package 0.6W
Ceramic Flatpack Package 0.5W
Maximum Device Power Dissipation 0.3W
Note: Maximum device Power Dissipation is defined as VDD x ICC and must withstand the added PD due to output current test; IO at +125°C
Derating Requirements:
SBDIP Package ..... No Derating Required
Ceramic Flatpack Package ..... No Derating Required

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Common Mode Range ..... ±7.0V
Input Low Voltage (VIL) ..... 0V to 0.3VDD Max
Input High Voltage (VIH) ..... VDD to 0.7VDD Min
Input Rise and Fall Time ..... 500ns Max

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	(NOTE 2) LIMITS MIN	(NOTE 2) LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, VDIFF = 1.0V, IO = -6mA (Notes 2, 5)	1, 2, 3	-55°C, +25°C, +125°C	4.1	-	V
Low Level Output Voltage	VOL	VDD = 4.5V, VDIFF = -1.0V, IO = 6mA (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Differential Input Voltage	VTH	VDD = VIH = 4.5V, -7.0V < VCM < 7.0V	1, 2, 3	-55°C, +25°C, +125°C	-400	+400	mV
Enabled High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 4)	1, 2, 3	-55°C, +25°C, +125°C	0.7 VDD	-	V
Enabled Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 4)	1, 2, 3	-55°C, +25°C, +125°C	-	0.3 VDD	V
Input Current High (Differential Inputs)	IINH	VDD = 5.5, +V = 10V, -V = 0V and +V = 0V, -V = 10V	1, 2, 3	-55°C, +25°C, +125°C	-	1.8	mA
Input Current Low (Differential Inputs)	IINL	VDD = 5.5, +V = -10V, -V = 0V and +V = 0V, -V = -10V	1, 2, 3	-55°C, +25°C, +125°C	-	-2.7	mA
Input Leakage Enable Pins	IIN	VDD = 5.5V, VIN = 0V, 5.5V	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA
Three-State Output Leakage Current	IOZ	VDD = 5.5V, VO = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-5.0	5.0	µA
Standby Supply Current	IDDSB	VDD = 5.5V, VDIFF = 1.0V Outputs = Open	1, 2, 3	-55°C, +25°C, +125°C	-	25	mA
Enable Clamp Voltage	VIC	At -1mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
		At 1mA			-	1.5	
Input Hysteresis	VHYST		1	-55°C, +25°C, +125°C	20	100	mV
Input Resistance	RIN	-7V ≤ VCM ≤ 7V	1	-55°C, +25°C, +125°C	4	20	kΩ

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged.
3. These test condition are detailed in EIA specification RS-422.
4. This parameter tested as inputs for the VOL, VOH, IOZ tests.
5. VIL = 0.3VDD, VIH = 0.7VDD.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Propagation Delay Time	TPLH, TPHL	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	6	40	ns
Propagation Delay Time	TPZH, TPZL	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	3	18	ns
Propagation Delay Time	TPLZ, TPHZ	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	6	29	ns
Propagation Delay Time TRISE/TFALL	TTHL, TTLH	VDD = 4.5V, VDIFF = 2.5V	9, 10, 11	-55°C, +25°C, +125°C	2	12	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Fail Safe	FSAFE	+ and - Inputs are Open, VOUT = Logic "1"	1	-55°C, +25°C, +125°C	4.1	-	V

NOTE:

1. The parameters listed on Table 3 are controlled via design or process parameters. Min and Max limits are guaranteed but not directly tested. These parameters are characterized at initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in Tables 1, 2 and 3.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±4mA
Three-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIN	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Initial Test	100% 5004	1, 7, 9	1 (Note 2)	1, 7, 9	
Interim Test	100% 5004	1, 7, 9, Δ	1, Δ (Note 2)	1, 7, 9	
PDA 1 & 2	100% 5004	1, 7, Δ	-	1, 7	
Final Test	100% 5004	2, 3, 8A, 8B, 10, 11	-	2, 3, 8A, 8B, 10, 11	

TABLE 6. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUP	MIL-STD-883 METHOD	GROUP A SUBGROUPS			
		TESTED FOR -Q	RECORDED FOR -Q	TESTED FOR -8	RECORDED FOR -8
Group A (Note 1)	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Subgroup B5	Sample 5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3 (Note 2)	N/A	
Subgroup B6	Sample 5005	1, 7, 9	-	N/A	
Group C	Sample 5005	N/A	N/A	1, 2, 3, 7, 8A, 8B, 9, 10, 11	
Group D	Sample 5005	1, 7, 9	-	1, 7, 9	
Group E, Subgroup 2	Sample 5005	1, 7, 9	-	1, 7, 9	

NOTES:

1. Alternate Group A testing in accordance with MIL-STD-883 method 5005 may be exercised.
2. Table 5 parameters only

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

TABLE 8. BURN-IN TEST CONNECTIONS (VDD = 6V, ±0.5V)

TEST	OPEN	GROUND	POWER SUPPLY A VDD	POWER SUPPLY B 1/2 VDD	POWER SUPPLY C 1/2 VDD	50KHz
Static Burn-In I	3, 5, 11, 13	2, 4, 6, 8, 10, 12, 14	1, 7, 9, 15, 16	-	-	-
Static Burn-In II	3, 5, 11, 13	1, 7, 8, 9, 15	2, 4, 6, 10, 12, 14, 16	-	-	-
Dynamic Burn-In Option 1	-	8, 12	4, 16	1, 3, 5, 7, 9, 11, 13, 15 (Note 2)	-	2, 6, 10, 14
Dynamic Burn-In Option 2	-	12, 8	4, 16	1, 7, 9, 15	3, 5, 11, 13	2, 6, 10, 14

NOTES:

1. Each pin except for VDD and GND will have a series resistor. (For static BI, R = 10kΩ ±5%, for dynamic BI, R = 680Ω ±5%)
2. When connecting the - inputs and their associated outputs to the same supply, a power supply bypass capacitor of 22µF must be used.

TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VDD	1/2 VDD	50kHz	25kHz
Radiation Exposure	3, 5, 11, 13	2, 4, 6, 8, 10, 12, 14	1, 7, 9, 15, 16	-	-	-

NOTES:

1. Each pin except for VDD and GND will have a series resistor. (R = 47kΩ ±5%).
2. When connecting the - inputs and their associated outputs to the same supply, a power supply bypass capacitor of 22µF must be used.

Harris Space Level Product Flow -Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Die Attach (Note 1)

100% Nondestructive Bond Pull, Method 2023

Sample - Wire Bond Pull Monitor, Method 2011

Sample - Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition A

CSI and/or GSI Pre-Cap (Note 7)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% PIND, Method 2020, Condition A

100% External Visual

100% Serialization

100% Initial Electrical Test (T0)

100% Static Burn-In 1, Condition A or B, 24 Hours Min, +125°C Min, Method 1015

100% Interim Electrical Test 1 (T1)

100% Delta Calculation (T0-T1)

100% Static Burn-In 2, Method 1015, Condition A or B, 24 Hours Minimum, +125°C Minimum

100% Interim Electrical Test 1 (T2)

100% Delta Calculation (T0-T2)

100% PDA 1, Method 5004 (Note 2)

100% Dynamic Burn-In, Condition D, 240 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test 2(T3)

100% Delta Calculation (T0-T3)

100% PDA 2, Method 5004 (Note 2)

100% Final Electrical Test (T4)

100% Fine/Gross Leak, Method 1014

100% Radiographic (X-Ray), Method 2012 (Note 3)

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 4)

Sample - Group B, Method 5005 (Note 5)

Sample - Group D, Method 5005 (Notes 5 and 6)

100% Data Package Generation (Note 8)

CSI and/or GSI Final (Note 7)

NOTES:

1. Silver glass die attach shall be permitted.
2. Failures from subgroup 1, 7 and deltas are used for calculating PDA. The maximum allowable PDA = 5% with no more than 3% of the failures from subgroup 7.
3. Radiographic (X-Ray) inspection may be performed at any point after serialization as allowed by Method 5004. Per method 5004, 1 view only is supplied on flat packages and leadless chip carriers, 2 views are supplied in all other cases.
4. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
5. Group B and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group B Samples, Group D Test and Group D Samples.
6. Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group D Generic Data. Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
7. CSI and/or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI Final Inspection, GSI PreCap inspection, and/or GSI Final Inspection.
8. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - Wafer Lot Acceptance Report (Method 5007). Includes reproductions of SEM photos with percent of step coverage.
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - X-Ray report and film. Includes penetrometer measurements.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Lot Serial Number Sheet (Good units serial number and lot number).
   - Variables Data (All Delta operations). Data is identified by serial number. Data header includes lot number and date of test.
   - Group B and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

Harris Space Level Product Flow -8

GAMMA Radiation Verification (Each Wafer) Method 1019, 4 Samples/Wafer, 0 Rejects

100% Die Attach (Note 1)

Periodic- Wire Bond Pull Monitor, Method 2011

Periodic- Die Shear Monitor, Method 2019 or 2027

100% Internal Visual Inspection, Method 2010, Condition B

CSI and/or GSI Pre-Cap (Note 6)

100% Temperature Cycle, Method 1010, Condition C, 10 Cycles

100% Constant Acceleration, Method 2001, Condition per Method 5004

100% External Visual

100% Initial Electrical Test

100% Dynamic Burn-In, Condition D, 160 Hours, +125°C or Equivalent, Method 1015

100% Interim Electrical Test

100% PDA, Method 5004 (Note 2)

100% Final Electrical Test

100% Fine/Gross Leak, Method 1014

100% External Visual, Method 2009

Sample - Group A, Method 5005 (Note 3)

Sample - Group B, Method 5005 (Note 4)

Sample - Group C, Method 5005 (Notes 4 and 5)

Sample - Group D, Method 5005 (Notes 4 and 5)

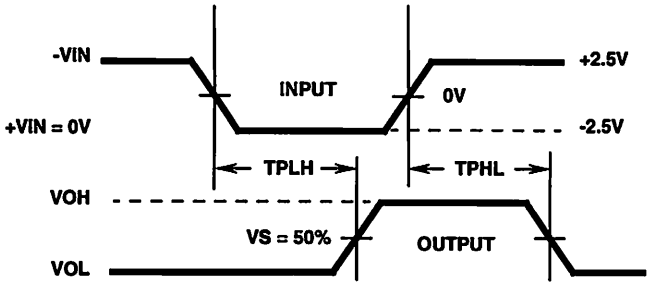
100% Data Package Generation (Note 7)

CSI and/or GSI Final (Note 6)

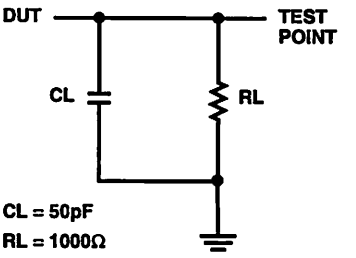
NOTES:

1. Silver glass die attach shall be permitted.
2. Failures from subgroup 1, 7 are used for calculating PDA. The maximum allowable PDA = 5%.
3. Alternate Group A testing may be performed as allowed by MIL-STD-883, Method 5005.
4. Group B, C and D inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for Group B Test, Group C Test, Group C Samples, Group D Test and Group D Samples.
5. Group C and/or Group D Generic Data, as defined by MIL-I-38535, is optional and will not be supplied unless required by the P.O. When required, the P.O. should include a separate line item for Group C Generic Data and/or Group D Generic Data. Generic data is not guaranteed to be available and is therefore not available in all cases.
6. CSI and/or GSI inspections are optional and will not be performed unless required by the P.O. When required, the P.O. should include separate line items for CSI PreCap inspection, CSI Final Inspection, GSI PreCap inspection, and/or GSI Final Inspection.
7. Data Package Contents:
   - Cover Sheet (Harris Name and/or Logo, P.O. Number, Customer Part Number, Lot Date Code, Harris Part Number, Lot Number, Quantity).
   - GAMMA Radiation Report. Contains Cover page, disposition, Rad Dose, Lot Number, Test Package used, Specification Numbers, Test equipment, etc. Radiation Read and Record data on file at Harris.
   - Screening, Electrical, and Group A attributes (Screening attributes begin after package seal).
   - Group B, C and D attributes and/or Generic data is included when required by the P.O.
   - The Certificate of Conformance is a part of the shipping invoice and is not part of the Data Book. The Certificate of Conformance is signed by an authorized Quality Representative.

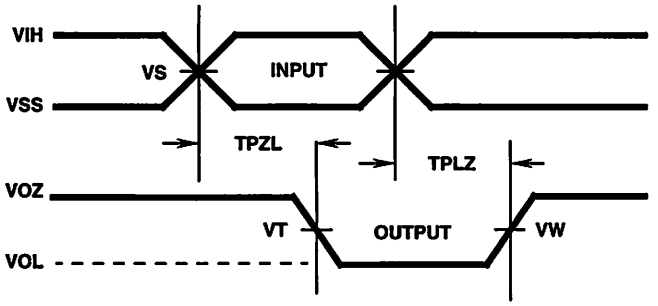
Propagation Delay Timing Diagram



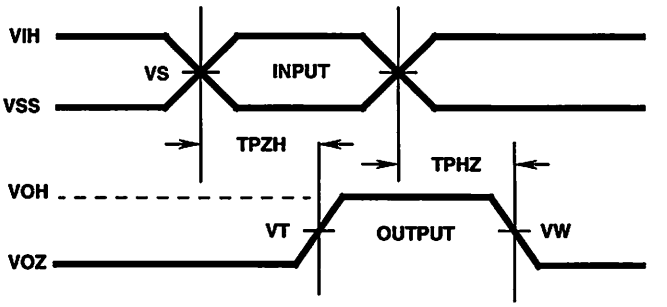
Propagation Delay Load Circuit



Three-State Low Timing Diagrams



Three-State High Timing Diagrams



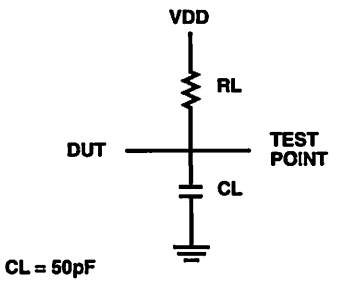
THREE-STATE LOW VOLTAGE LEVELS

PARAMETER	HS-26C32RH	UNITS
VDD	4.50	V
VIH	4.50	V
VS	2.25	V
VT	50	%
VW	VOL + 0.5	V
GND	0	V

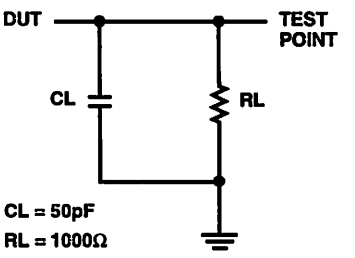
THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26C32RH	UNITS
VDD	4.50	V
VIH	4.50	V
VS	2.25	V
VT	50	%
VW	VOH - 0.5	V
GND	0	V

Three-State Low Load Circuit



Three-State High Load Circuit



Metallization Topology

DIE DIMENSIONS:
84mils x 130 mils
(2140µm x 3290µm)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å

M2: Al/Si/Cu
Thickness: 5800Å

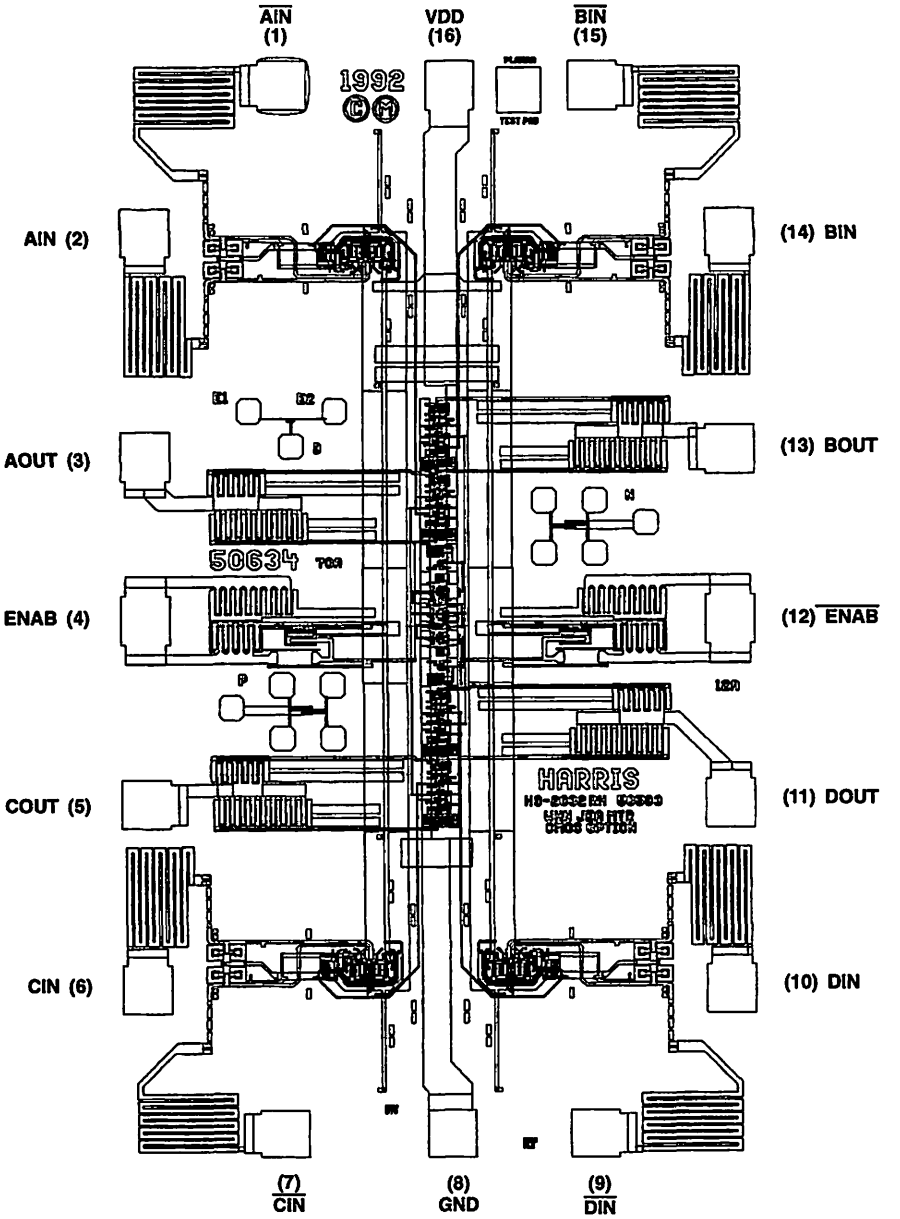
GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

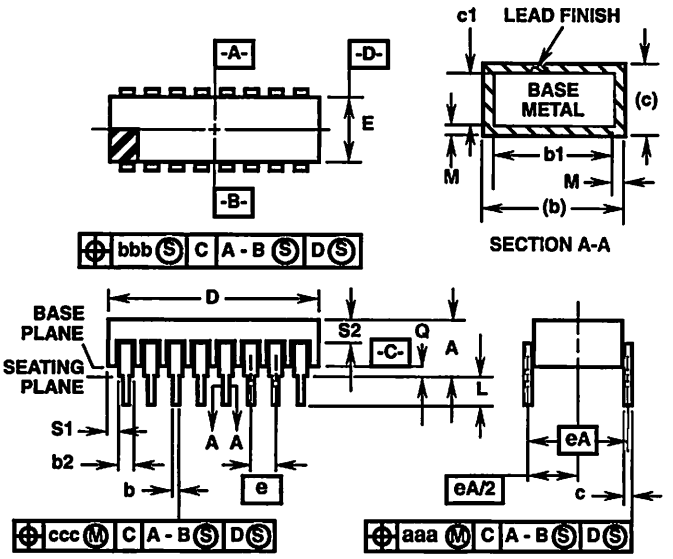
BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26C32RH



Packaging



D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

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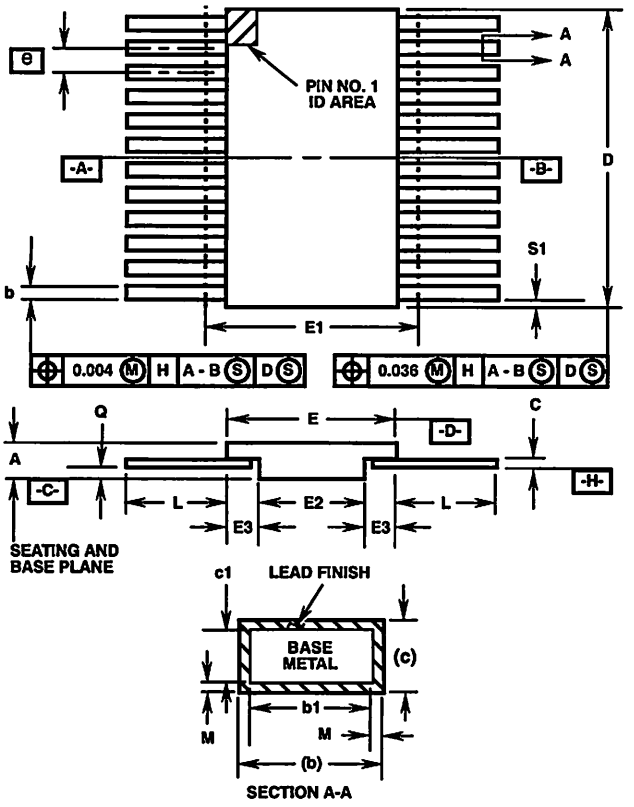
NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

Packaging (Continued)



K16.A MIL-STD-1835 CDFP4-F16 (F-5A, CONFIGURATION B)
16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.440	-	11.18	3
E	0.245	0.285	6.22	7.24	-
E1	-	0.315	-	8.00	3
E2	0.130	-	3.30	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	16		16		-

Rev. 1 2-20-95

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.