HARRIS SEMICONDUCTOR

HS-26C31RH

Radiation Hardened Quad Differential Line Driver

November 1995

Features

- 1.2 Micron Radiation Hardened CMOS
  - Total Dose Up to 300K RAD(Si)
  - Dose Rate Upset > $1x10^9$ RAD/Sec (20ns Pulse)
- Latchup Free
- EIA RS-422 Compatible Outputs (Except for IOS)
- CMOS Inputs
- High Impedance Outputs when Disabled or Powered Down
- Low Power Dissipation 2.75mW Standby (Max)
- Single 5V Supply
- Low Output Impedance 10Ω or Less
- Full -55°C to +125°C Military Temperature Range

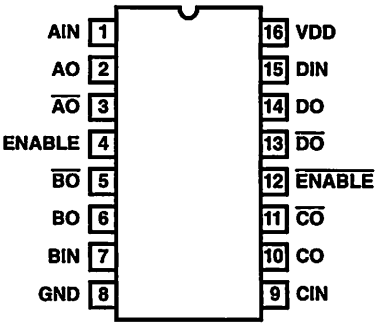
Description

The Harris HS-26C31RH is a quad differential line driver designed for digital data transmission over balanced lines and meets the requirements of EIA standard RS-422. Radiation hardened CMOS processing assures low power consumption, high speed, and reliable operation in the most severe radiation environments.

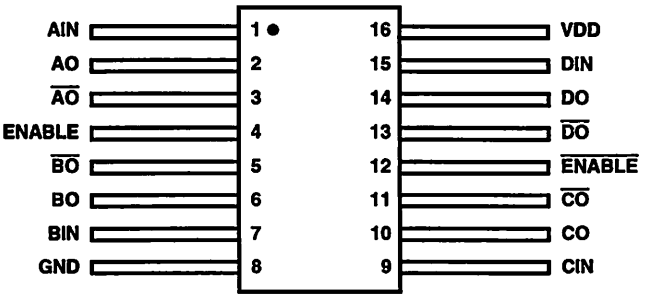
The HS-26C31RH accepts CMOS and converts them to RS-422 compatible outputs. This circuit uses special outputs that enable the drivers to power down without loading down the bus. Enable and disable pins allow several devices to be connected to the same data source and addressed independently.

Pinouts

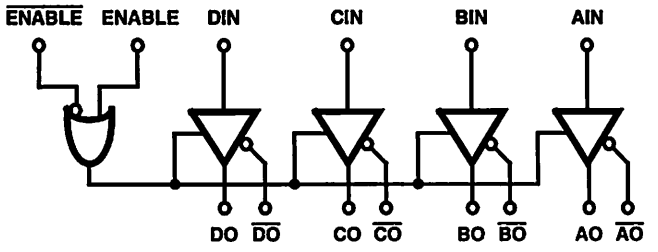
16 Lead Ceramic Dual-in-Line Metal Seal Package (SBDIP)
Mil-Std-1835 CDIP2-T16
TOP VIEW



16 Lead Ceramic Metal Seal Flatpack Package (Flatpack)
Mil-Std-1835 CDFP4-F16
TOP VIEW



Logic Diagram



TRUTH TABLE

DEVICE POWER ON/OFF	INPUTS			OUTPUT	
	ENABLE	$\overline{ENABLE}$	IN	OUT	$\overline{OUT}$
ON	0	1	X	HI-Z	HI-Z
ON	1	X	0	0	1
ON	X	0	0	0	1
ON	1	X	1	1	0
ON	X	0	1	1	0
OFF (0V)	X	X	X	HI-Z	HI-Z

Ordering Information

PART NUMBER	TEMPERATURE RANGE	SCREENING LEVEL	PACKAGE
HS1-26C31RH-8	-55°C to +125°C	Harris Class B Equivalent	16 Lead Sidebraze DIP
HS1-26C31RH-Q	-55°C to +125°C	Harris Class S Equivalent	16 Lead Sidebraze DIP
HS9-26C31RH-8	-55°C to +125°C	Harris Class B Equivalent	16 Lead Flatpack
HS9-26C31RH-Q	-55°C to +125°C	Harris Class S Equivalent	16 Lead Flatpack
HS1-26C31RH/Sample	+25°C	Sample	16 Lead Sidebraze DIP
HS1-26C31RH/Proto	-55°C to +125°C	Prototype	16 Lead Sidebraze DIP
HS9-26C31RH/Sample	+25°C	Sample	16 Lead Flatpack
HS9-26C31RH/Proto	-55°C to +125°C	Prototype	16 Lead Flatpack

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **3401.2**
Spec Number **518789**

Absolute Maximum Ratings

Supply Voltage ..... -0.5V to +7.0V
Input, Output or I/O Voltage ..... -0.5 to VDD+0.5V
Output Voltage with Power Off (0V) ..... -0.5V to +7.0V
DC Diode Input Current (Any Input) ..... ±20mA
DC Drain Current (Any One Input) 350mA
DC VDD or Ground Current 400mA
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10s) ..... +300°C

Reliability Information

Thermal Resistance	θ_{JA}	θ_{JC}
SBDIP Package	73°C/W	24°C/W
Ceramic Flatpack Package	114°C/W	29°C/W

Maximum Package Power Dissipation at +125°C Ambient:
SBDIP Package 0.68W
Ceramic Flatpack Package 0.44W
If device power exceeds package dissipation capability provide heat sinking or derate linearly at the following rate:
SBDIP Package ..... 13.7mW/°C
Ceramic Flatpack Package ..... 8.8mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Operating Temperature Range ..... -55°C to +125°C
Input Rise and Fall Time ..... 500ns Max
Input Low Voltage (VIL) ..... 0V to 0.3VDD Max
Input High Voltage (VIH) ..... VDD to 0.7VDD Min

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
High Level Output Voltage	VOH	VDD = 4.5V, and 5.5V IO = -20mA (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	2.5	-	V
Low Level Output Voltage	VOL	VDD = 4.5V and 5.5V, IO = 20mA (Notes 2, 6)	1, 2, 3	-55°C, +25°C, +125°C	-	0.5	V
Differential Output Voltage	VT, $\overline{VT}$	VDD = VIH = 4.5V, RL = R1 + R2, VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	2.0	-	V
Difference in Differential Output	IVTI - $\overline{VTI}$	VDD = VIH = 4.5V, RL = R1 + R2, VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
Common Mode Output Voltage	VOS, $\overline{VOS}$	VDD = VIH = 4.5V, RL = R1 + R2, VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	3.0	V
Difference in Common Mode Output	IVOS - $\overline{VOS}$I	VDD = VIH = 4.5V, RL = R1 + R2, VIL = 0V (Note 3)	1, 2, 3	-55°C, +25°C, +125°C	-	0.4	V
High Level Input Voltage	VIH	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	0.7 VDD	-	V
Low Level Input Voltage	VIL	VDD = 4.5V, 5.5V (Note 5)	1, 2, 3	-55°C, +25°C, +125°C	-	0.3 VDD	V
Standby Supply Current	IDDSB	VDD = 5.5V, Output = OPEN, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	500	µA
Three-State Output Leakage Current	IOZ	VDD = 5.5V, Force Voltage = 0V or VCC (Note 7)	1, 2, 3	-55°C, +25°C, +125°C	-	±5	µA
Input Leakage	IIN	VDD = 5.5V, VIN = VDD or GND	1, 2, 3	-55°C, +25°C, +125°C	-	±1.0	µA

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Leakage Current Power OFF	IOFF	VDD = 0V, VOUT = 6V, -250mV, Inputs = GND	1, 2, 3	-55°C, +25°C, +125°C	-100	100	µA
Input Clamp Voltage	VIC	At -1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	-1.5	V
		At +1.0mA	1, 2, 3	-55°C, +25°C, +125°C	-	+1.5	V

NOTES:

1. All voltages referenced to device ground.
2. Force/Measure functions may be interchanged.
3. These test conditions are detailed in EIA specification RS-422. R1 = R2 = 50Ω.
4. Only one input pin set up to VIN per test. All other pins set to VCC or GND.
5. This parameter tested as inputs levels in VOL/VOH, IOZ, functional test and/or discrete voltage level.
6. VIL = 0.3VDD, VIH = 0.7VDD.
7. The input is conditioned to have the output in the opposite state of the forcing IOZ condition.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Propagation Delay	TPLH, TPHL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	22	ns
Propagation Delay	TPZH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPZL	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	5	28	ns
Propagation Delay	TPHZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	22	ns
Propagation Delay	TPLZ	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	2	22	ns
Rise and Fall Times	TTHL, TTLH	VDD = 4.5V	9, 10, 11	-55°C, +25°C, +125°C	1	10	ns
Output Skew	TSKEW (Note 3)	VDD = 4.5V, RL = 100Ω, CL = 40pF	9, 10, 11	-55°C, +25°C, +125°C	-	3	ns

NOTES:

1. All voltages referenced to device ground.
2. See Table EIA RS-422
3. Skew is defined as the difference in propagation delays between complementary outputs at the 50% point.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Capacitance	CIN	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Output Capacitance	COUT	VDD = Open, f = 1MHz	1	-55°C, +25°C, +125°C	-	12	pF
Operating Short Circuit	IOS	VDD = 5.5V, VIN = VDD or GND, VOUT = 0V	2	-55°C, +25°C, +125°C	-30	-150	mA

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	NOTES	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
On-State Resistance	RON	VDD = 4.5V, VOUT = 1.5V, VIN = VDD or GND	1	-55°C, +25°C, +125°C	-	10	Ω
Dynamic Current	IDYN	VCC = 4.5V, FQ = 1MHz, VIN = VCC or GND	1, 5	+25°C, +125°C	Typical 3		mA
Power Dissipation Capacitance	CPD	VCC = 4.5V, FQ = 1MHz	1, 4	+25°C	Typical 170		pF

NOTES:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after major design or process changes that affect these parameters.
2. Only one output at a time may be shorted.
3. Power Up/Down Feature: Outputs will remain in the Hi-Z state with VDD ≤ 2.5V and become active at VDD ≥ 4.0V. The active output state will be determined by the input conditions.
4. This parameter is a per channel measurement.
5. This parameter is measured with a 100pF load, one channel only.

TABLE 4. POST IRRADIATION ELECTRICAL PERFORMANCE CHARACTERISTICS

The post irradiation electrical performance characteristics are the same as the parameters listed in Tables 1, 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C) AND GROUP B, SUBGROUP 5 DELTA PARAMETERS

PARAMETER	SYMBOL	DELTA LIMITS
Standby Supply Current	IDDSB	±100µA
Three-State Output Leakage Current	IOZ	±1.0µA
Low Level Output Voltage	VOL	±60mV
High Level Output Voltage	VOH	±150mV
Input Leakage Current	IIL, IIH	±150nA

TABLE 6. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS		METHOD	-Q SUBGROUPS	READ AND RECORD
Initial Test (Pre Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test I (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
Interim Test II (Post Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Interim Test III (Post-Burn-In)		100%/5004	1, 7, 9	See Table 5
PDA		100%/5004	1, 7, 9, Δ	-
Final Test		100%/5004	2, 3, 8A, 8B, 10, 11	-
Group A		Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11	-
Group B	B5	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11, Δ	Subgroups 1, 2, 3, 9, 10, 11
	B6	Samples/5005	1, 7, 9	-
Group D		Samples/5005	1, 7, 9	-

TABLE 6A. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Initial Test (Pre Burn-In)	100%/5004	1, 7, 9
Interim Test (Post-Burn-In)	100%/5004	1, 7, 9
PDA	100%/5004	1, 7, 9

TABLE 6A. APPLICABLE SUBGROUPS (Continued)

CONFORMANCE GROUPS	METHOD	-8 SUBGROUPS
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group C	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Group D	Samples/5005	1, 7, 9

TABLE 7. TOTAL DOSE IRRADIATION

CONFOMRANCE GROUPS	METHOD	TEST		READ AND RECORD	
		PRE-RAD	POST-RAD	PRE-RAD	POST-RAD
Group E Subgroup 2	5005	1, 7, 9	Table 4	1, 7, 9	Table 4

NOTE: Each pin except for VDD and GND will have a 47kΩ resistor ±5%.

TABLE 8. BURN-IN TEST CONNECTIONS (+125°C < T_A < 139°C, VCC = 6V, ±0.5V)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Static Burn-In I	2, 3, 5, 6, 10, 11, 13, 14	1, 4, 7, 8, 9, 12, 15	16	-	-	-
Static Burn-In II	2, 3, 5, 6, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-
Dynamic Burn-In	-	8, 12	4, 16	2, 3, 5, 6, 10, 11, 13, 14	1, 7, 9, 15	-

NOTE: Each pin except for VDD and Ground will have a series resistor as specified below:

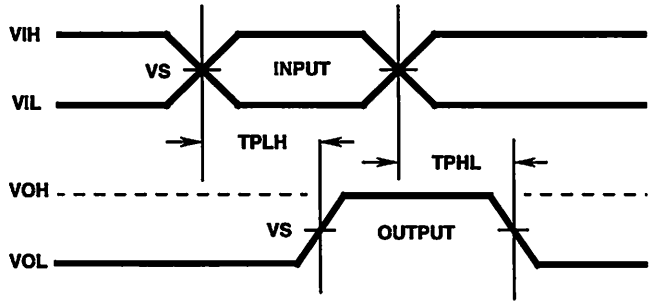
Static Burn-In	Dynamic Burn-In
10kΩ ±5%	200Ω ±5%

TABLE 9. IRRADIATION TEST CONNECTIONS (T_A = +25°C, ±5°C, VDD = 5V, ±10%)

TEST	OPEN	GROUND	VDD	1/2VDD	50KHz	25KHz
Radiation Exposure	2, 3, 5, 8, 10, 11, 13, 14	8	1, 4, 7, 9, 12, 15, 16	-	-	-

NOTE: Each pin except for VDD and Ground will have a series resistor.

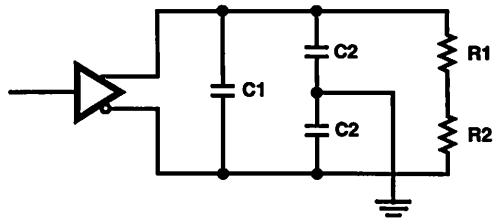
Propagation Delay Timing Diagram



AC VOLTAGE LEVELS

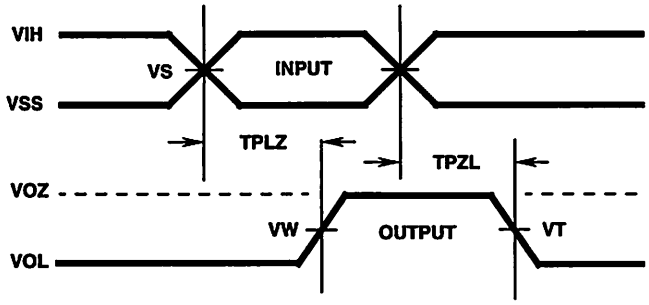
PARAMETER	HS-26C31	UNITS
VDD	4.50	V
VIH	4.50	V
VS	50	%
VIL	0	V
GND	0	V

Propagation Delay Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω

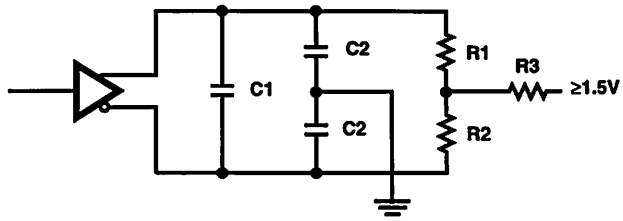
Three-State Low Timing Diagrams



THREE-STATE LOW VOLTAGE LEVELS

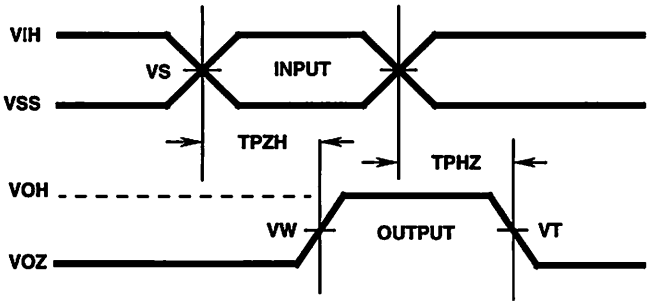
PARAMETER	HS-26C31	UNITS
VDD	4.50	V
VIH	4.50	V
VS	50	%
VW	VOL + 0.3	V
VT	0.80	V

Three-State Low Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

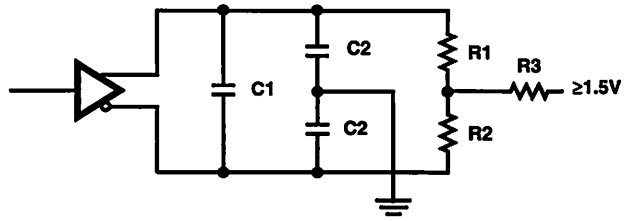
Three-State High Timing Diagrams



THREE-STATE HIGH VOLTAGE LEVELS

PARAMETER	HS-26C31	UNITS
VDD	4.50	V
VIH	4.50	V
VS	50	%
VT	VOH - 0.3	V
VW	2.00	V

Three-State High Load Circuit



C1 = C2 = C3 = 40pF
R1 = R2 = 50Ω
R3 = 500Ω

Harris - Space Level Product Flow - Q

Wafer Lot Acceptance (All Lots) Method 5007 (Includes SEM)

Radiation Verification (Each Wafer) Method 1019, 300k RAD (Si), 4 Samples/Wafer, 0 Rejects

100% Nondestructive Bond Pull Method 2023

100% Internal Visual Inspection Method 2010, Condition A

100% Temperature Cycling Method 1010, Condition C

100% Constant Acceleration

100% Particle Impact Noise Detection Testing

100% External Visual Inspection

100% Serialization

100% Initial Electrical Test

100% Static Burn-In1: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 1 (Note 1)

100% Static Burn-In 2: 24 Hour, +125°C Min, Method 1015

100% Interim Electrical Test 2 (Note 1)

100% Dynamic Burn-In 240 Hour, +125°C or Equivalent, Method 1015

100% Interim Electrical 3 (Note 1)

100% Final Electrical Test

100% Fine and Gross Seal Method 1014

100% Radiographics Method 2012

100% External Visual Method 2009

Group A (All Tests) Method 5005 (Class S)

Data Package Generation (Note 2)

NOTES:

1. Failure from interim electrical tests 1 and 2 are combined for determining PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures). Interim electrical tests 3 PDA (PDA = 5% for subgroups 1, 7, 9 and delta failures combined, PDA = 3% for subgroup 7 failures).
2. Data Package Contents:
   Cover Sheet (P.O. Number, Customer Number, Lot Date Code, Harris Number, Lot Number, Quantity).
   Certificate of Conformance (as found on shipper).
   Lot Serial Number Sheet (Good Unit(s) Serial Number and Lot Number).
   Variables Data (All Read, Record, and delta operations).
   Attribute Summary from Post Seal through Final Test.
   Group A Attributes Data Summary.
   Wafer Lot Acceptance Report (Method 5007) to include reproductions of SEM photos. NOTE: SEM photos to include % of step coverage.
   X-Ray Report and File(s), including penetrameter measurements.
   GAMMA Radiation Report with initial shipment of devices from the same wafer lot; containing a Cover Page, Disposition, Rad Dose, Lot Number, Test Package, Spec Number(s), Test Equipment, etc. Irradiation Read and Record data will be on file at Harris.

Harris -8 Product Flow

Internal Visual Inspection - Method 2010, Condition B or B-Alternate

Gamma Radiation Assurance Tests Method 1019

Temperature Cycling Method 1010, Condition C

Constant Acceleration Method 2001 Y1, Condition per Method 5004

Fine and Gross Leak Tests Method 1014

Marking

Initial Electrical Tests (T0)

Dynamic Burn-In 160 Hrs, +125°C Method 1015 or Equivalent, Condition D

NOTE:

1. '-8' Data package contains:
   Test Attributes (includes Group A) -55°C, +25°C, +125°C
   Radiation Testing Certificate of Conformance

Electrical Tests Subgroups 1, 7, 9 (T1) Method 5004

PDA Calculation 5% Subgroups 1, 7 Method 5004

Electrical Tests +125°C, -55°C Method 5004

Group A Inspection Method 5005

External Visual Inspection Method 2009

Data Package Generation (Note 3)

Metallization Topology

DIE DIMENSIONS:
87 mils x 188 mils
(2219 x 4770)

METALLIZATION:
M1: Mo/Tiw
Thickness: 5800Å

M2: Al/Si/Cu
Thickness: 10kÅ ±1kÅ

GLASSIVATION:
Type: SiO_2
Thickness: 10kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
$<2.0 \times 10^5 A/cm^2$

BOND PAD SIZE: 110µm x 100µm

Metallization Mask Layout

HS-26C31RH