REVISIONS

Letter	ECO No.	Description	Checked	Approved	Date
A	36-114	INITIAL RELEASE	D. G.	EAB	12-7-94

NAME	DATE
Drawn: BRIAN KLATT	11/23/94
Checked: D. Gordon	12/7/94
Approved: EA Boughton	12-7-94
Released: K. Tibbetts	12.7.94

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CENTER FOR SPACE RESEARCH

MICROCIRCUITS, CMOS, 1-MEGABIT, ELECTRICALLY ERASABLE PROGRAMMABLE READ ONLY MEMORY(EEPROM)

Size	Code Identification No.	Drawing No.	Rev.
T	80230	36-02306	A

Scale: NONE

1.0 SCOPE

1.1 Introduction This drawing describes device requirements for 1-Megabit Electrically Erasable Programmable Read Only Memories (EEPROM), used in flight hardware for a space experiment on the AXAF CCD Imaging Spectrometer (ACIS) Instrument. The part described herein is a Hitachi die, P/N HN58C1001, packaged in a 32 lead metal flat pack.

1.2 Part Number The complete MIT part number shall be 36-02306.

1.3 Absolute maximum ratings Absolute maximum ratings are listed on page 5-71 of Hitachi 1993 Nonvolatile Memory Data Book M13T028.

2.0 APPLICABLE DRAWINGS

2.1 Government Specifications and Standards Unless otherwise specified, the following specifications and standards, of the latest released issue, form a part of this drawing, to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	Microcircuits, General Specification for

STANDARDS

MIL-STD-883	Test Methods and Procedures for Microelectronics

INDUSTRY

Hitachi	1993 Nonvolatile Memory Data Book M13T028

NOTE: Pages 5-68 through 5-82 of Hitachi 1993 Nonvolatile Memory Data Book M13T028, are included herein for convenience.

2.2 Order of precedence In the event of conflict between the text of this drawing and the references cited herein, the text of this drawing shall govern.

3.0 REQUIREMENTS

3.1 General Requirements

3.1.1 Item Requirements The microcircuits described herein shall, in all respects, meet all the requirements of this specification and the intent of MIL-M-38510 for a class B microcircuit. These microcircuits shall be fabricated and tested using production and test facilities and a Reliability and Quality Assurance program adequate to assure successful compliance with this specification and the intent of MIL-M-38510, as modified herein.

3.1.2 Procuring Activity For the purposes of this specification and documents referenced herein, the procuring activity is the Massachusetts Institute of Technology (MIT), Center for Space Research (CSR).

3.1.3 Product Changes The supplier shall notify MIT of proposed changes to Microcircuits, including changes in design, materials, fabrication methods, or processes, and changes which may affect the quality or intended end use.

3.2 Part marking Microcircuit marking shall meet the intent of paragraph 3.6 of MIL-M-38510.

3.2.1 Part Identification Number (PIN) Microcircuits shall be marked with the MIT part number; 36-02306.

3.3 Electrical performance characteristics Unless otherwise specified, the electrical performance characteristics are as specified in Hitachi 1993 Nonvolatile Memory Data Book M13T028, for Capacitance (page 5-71), DC Electrical Characteristics (page 5-72), AC Electrical Characteristics for read operation (page 5-72), AC Electrical Characteristics for byte erase and byte write operation (page 5-73), AC Electrical Characteristics for page write operation (page 5-76), AC Electrical Characteristics for data not polling operation (page 5-79), and AC Electrical Characteristics for software data protection cycle operation (page 5-80), and apply over the full operating temperature range, at -55°C, +25°C, and +125°C.

3.4 Design and Construction Requirements

3.4.1 Package The package shall be a 32 terminal, hermetically sealed, metal flat pack. The package shall provide the maximum radiation shielding which is practical for a 100,000 Km orbit, for five (5) years. Leads shall be formed, after final electrical test, for surface mounting (flush to the board) on a printed circuit board. Device hermeticity shall be tested after lead forming.

3.4.2. Lead Finish The lead finish shall be "A" per MIL-H-38510.

3.4.3 Terminal connections The terminal connections shall be the same as that for the HN58C1001FP series per Hitachi 1993 Nonvolatile Memory Data Book M13T028 on page 5-69.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection Unless otherwise specified herein, the supplier is responsible for the performance of all examinations and tests as specified herein.

4.2 Screening All Microcircuits (100%) shall be subjected to and pass the screen tests and examinations defined in paragraph 4.6 of MIL-M-38510, for a class B device. Burn-in shall be performed at 125°C, for 160 hours minimum.

4.2.1 Xray All Microcircuits (100%) shall be subjected to and pass radiographic examination per MIL-STD-883, method 2012.

4.2.2 Particle Impact Noise Detection (PIND) All Microcircuits (100%) shall be subjected to and pass PIND examination per MIL-STD-883, method 2020, condition B.

4.3 Quality Conformance Inspection (QCI) Quality conformance inspection shall be in accordance with paragraph 4.5 of MIL-M-38510, for a class B device.

4.4 Destructive Physical Analysis (DPA) An internal destructive examination shall be performed in accordance with paragraph 3.5, of MIL-STD-883, method 5009. Sample size shall be two (2) for lot sizes greater than 200, and one (1) sample for lot sizes of 200 or less.

4.5 Inspection and Test Records The supplier shall maintain inspection and test records for 36 months after hardware delivery to MIT. Test data for all electrical tests, screening, DPA, and QCI inspections shall be submitted to MIT with the delivery of flight parts.

4.6 Source Inspection

4.6.1 Government Source Inspection (GSI) The government has the right to inspect any or all of the work included in this order at the supplier's plant. In the event that Government Source Inspection (GSI) is imposed, the Government quality representative who has been delegated NASA quality assurance functions for this procurement shall be notified immediately upon receipt of this order. The Government representative shall also be notified 48 hours in advance of the time that parts are ready for inspection or test.

4.6.2 MIT Source Inspection MIT Performance Assurance will impose mandatory inspection points (MIPs) at wire bonding (precap visual examination) and final test, and must be notified 2 weeks before parts are ready for MIT Inspection. (call area code 617, phone 253-7555).

5.0 PACKAGING

5.1 Packaging requirements Packaging shall be in accordance with paragraph 5.1 of MIL-M-38510.

6.0 NOTES

6.1 Approved Source of Supply

TBD

HN58C1001 Series — Preliminary

1M (128K x 8-bit) EEPROM

■ DESCRIPTION

The Hitachi HN58C1001 is a 1-Megabit CMOS Electrically Erasable Programmable Read Only Memory (EEPROM) organized as 131,072 x 8-bits. The HN58C1001 is capable of in-system electrical Byte and Page reprogrammability.

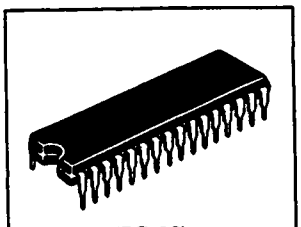
The HN58C1001 achieves high speed access, low power consumption, and a high level of reliability by employing advanced MNOS memory technology and CMOS process and circuitry technology.

The HN58C1001 has a 128-Byte Page Programming function to make its erase and write operations faster. The HN58C1001 features $\overline{\text{Data}}$ Polling and a Ready/$\overline{\text{Busy}}$ signal to indicate completion of erase and programming operations.

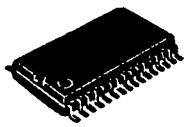
The HN58C1001 provides several levels of data protection. Hardware data protection is provided with the $\overline{\text{RES}}$ pin, in addition to noise protection on the $\overline{\text{WE}}$ signal and write inhibit on power on and off. Software data protection is implemented using the JEDEC Optional Standard algorithm.

The HN58C1001 is designed for high reliability in the most demanding applications. Data retention is specified for 10 years and erase/write endurance is guaranteed to a minimum of 100,000 cycles in the Page Mode.

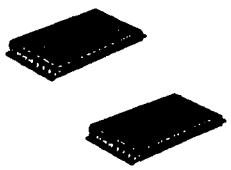
The HN58C1001 is offered in 32-pin Plastic DIP and 32-lead Plastic SOP and TSOP packages. The HN58C1001 TSOP is offered in both standard and reverse bend pinouts.



(DP-32)



(FP-32D)



(TFP-32DA and TFP-32DAR)

■ FEATURES

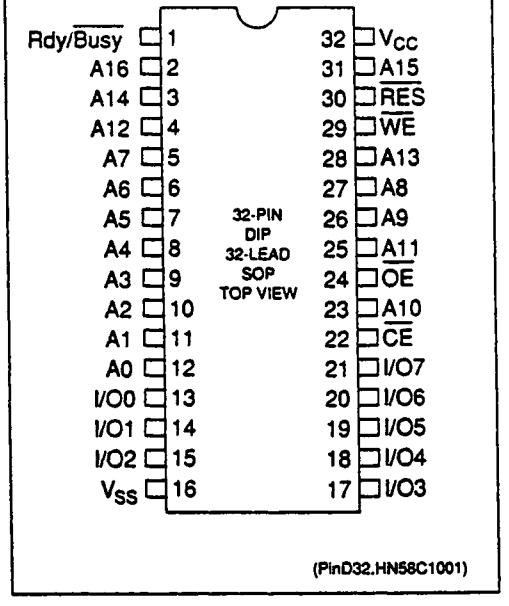
- Single Power Supply:
  V_{cc} = 5V ± 10%
- High Speed Access Times:
  150 ns (max)
- Low Power Dissipation:
  Active Current: 20 mW/MHz (typ)
  Standby Current: 100 µW (max)
- Automatic Programming:
  Automatic Page Write: 10 ms (max)
  128 Byte Page Size
  Automatic Byte Write: 10 ms (max)
- $\overline{\text{Data}}$ Polling and Ready/$\overline{\text{Busy}}$ Signals
- Hardware Data Protection with $\overline{\text{RES}}$ pin
- Data Protection Circuitry on Power On/Off
- Software Data Protection Algorithm
- Data Retention: 10 years
- Erase/Write Endurance:
  100,000 cycles in Page Mode
- Packages:
  32-pin Plastic DIP
  32-pin Plastic SOP
  32-lead Plastic TSOP (Type I)

■ ORDERING INFORMATION

Type No.	Access Time	Package
HN58C1001P-15	150 ns	32-pin Plastic DIP (DP-32)
HN58C1001FP-15	150 ns	32-lead Plastic SOP (FP-32D)
HN58C1001T-15	150 ns	32-lead Plastic TSOP (TFP-32DA)
HN58C1001R-15	150 ns	32-lead Plastic TSOP (TFP-32DAR) Reverse bend

■ PIN ARRANGEMENT

HN58C1001P Series
HN58C1001FP Series



(PinD32.HN58C1001)

■ PIN DESCRIPTION

Pin Name	Function
A_0 - A_{16}	Address
I/O_0 - I/O_7	Input/Output
$\overline{OE}$	Output Enable
$\overline{CE}$	Chip Enable
$\overline{WE}$	Write Enable
V_{CC}	Power Supply
V_{SS}	Ground
Rdy/$\overline{Busy}$	Ready/Busy
$\overline{RES}$	Reset

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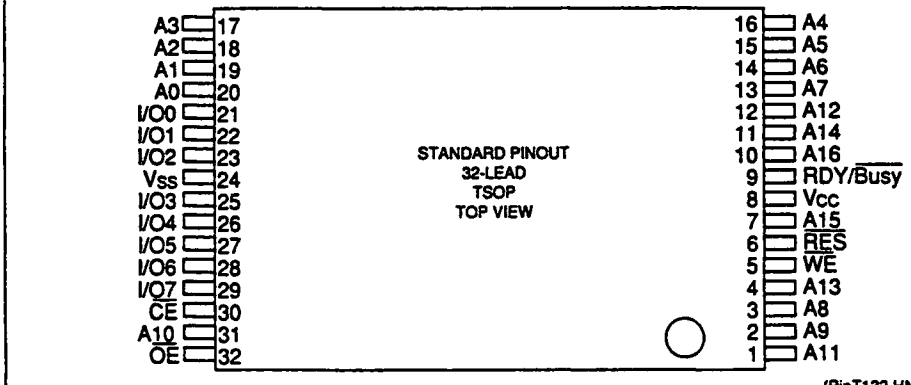
HN58C1001 Series

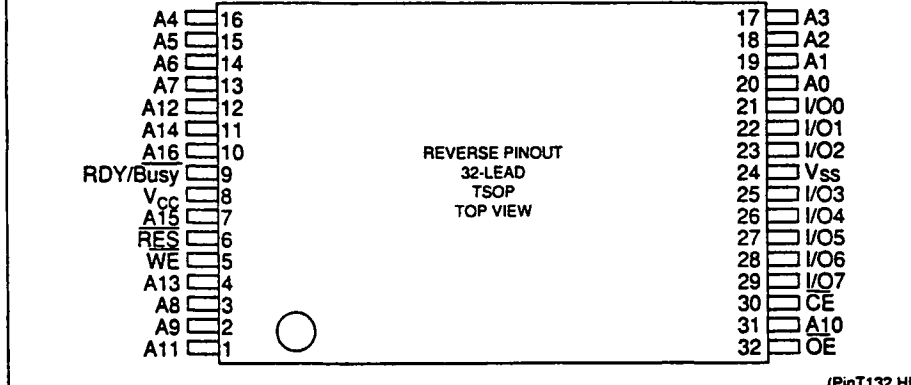
■ PIN ARRANGEMENT (cont.)

HN58C1001T Series



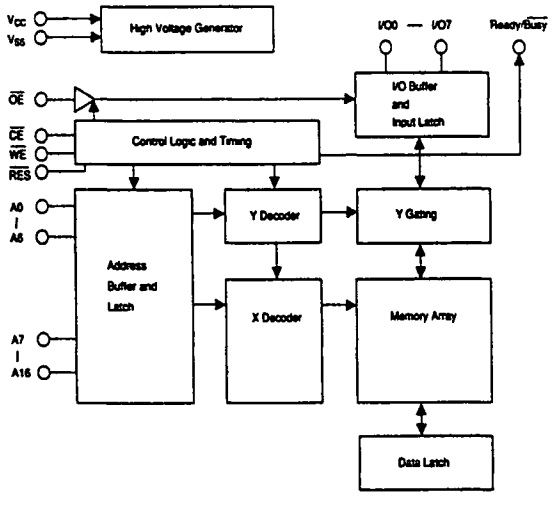
(PinT132.HN58C1001T)

HN58C1001R Series



(PinT132.HN58C1001R)

■ BLOCK DIAGRAM



(BD.HN58C1001)

■ MODE SELECTION

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$\overline{RES}$	RDY/$\overline{Busy}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	V_H	High-Z	D_{OUT}
Standby	V_{IH}	X	X	X	High-Z	High-Z
Write	V_{IL}	V_{IH}	V_{IL}	V_H	High-Z→V_{OL}	Din
Deselect	V_{IL}	V_{IH}	V_{IH}	V_H	High-Z	High-Z
Write Inhibit	X	X	V_{IH}	X	-	-
	X	V_{IL}	X	X	-	-
$\overline{Data}$ Polling	V_{IL}	V_{IL}	V_{IH}	V_H	V_{OL}	Data Out (I/O_7)
Program	X	X	X	V_{IL}	High-Z	High-Z

Note: 1. X = Don't Care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage [1]	V_{CC}	-0.6 to +7.0	V
Input Voltage [1]	V_{IN}	-0.5[2] to +7.0	V
Operating Temperature Range [3]	T_{OPR}	0 to +70	°C
Storage Temperature Range	T_{STG}	-55 to +125	°C

Notes: 1. Relative to V_{SS}.
2. V_{IN} min = -3.0V for pulse width ≤ 50 ns.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Capacitance	C_{IN}	-	-	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}	-	-	12	pF	V_{OUT} = 0V

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■ DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 10%, T_a = 0 to 70°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Input Leakage Current	I_{LI}	-	-	2	µA	V_{CC} = 5.5 V, V_{IN} = 5.5 V
Output Leakage Current	I_{LO}	-	-	2	µA	V_{CC} = 5.5 V, V_{OUT} = 5.5 V/0.4 V
Standby V_{CC} Current	I_{CC1}	-	-	20	µA	$\overline{CE}$ = V_{CC}
	I_{CC2}	-	-	1	mA	$\overline{CE}$ = V_{IH}
Operating V_{CC} Current	I_{CC3}	-	-	15	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 1 µs
		-	-	40	mA	I_{OUT} = 0 mA, Duty = 100%, Cycle = 200 ns
Input Voltage	V_{IL}	-0.3 [1]	-	0.8	V	
	V_{IH}	2.2	-	V_{CC} + 1	V	
	V_H	V_{CC}-1.0	-	V_{CC} + 1	V	
Output Voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2.1 mA
	V_{OH}	2.4	-	-	V	I_{OH} = -400 µA

Notes: 1. V_{IL} min = -1.0 V for pulse width ≤ 50 ns.
2. I_{LI} on $\overline{RES}$ = 100 µA Max.

■ AC ELECTRICAL CHARACTERISTICS FOR READ OPERATION

(T_a = 0 to 70°C, V_{CC} = 5V ± 10%)

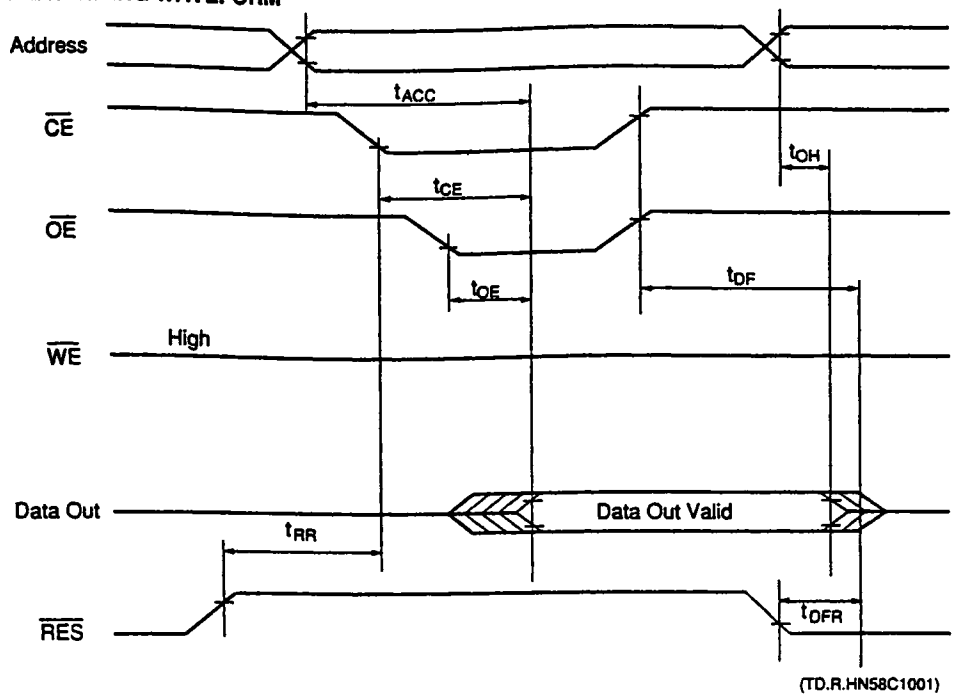
Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall times: ≤ 20 ns
- Output load: 1 TTL Gate + 100 pF (Including scope and jig)
- Reference levels for measuring timing: 0.8 V, 1.8 V

Item	Symbol	HN58C1001-15 Min.	HN58C1001-15 Max.	Unit	Test Condition
Address Access Time	t_{ACC}	-	150	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Chip Enable Access Time	t_{CE}	-	150	ns	$\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Enable Access Time	t_{OE}	10	75	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Hold to Address Change	t_{OH}	0	-	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
Output Disable to High-Z [1]	t_{DF}	0	50	ns	$\overline{CE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
	t_{DFR}	0	350	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}
$\overline{RES}$ to Output Delay	t_{RR}	0	450	ns	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}

Note: 1. t_{DF} is defined as the time at which the output becomes an open circuit and data is no longer driven.

■ **READ TIMING WAVEFORM**



(TD.R.HN58C1001)

■ **AC ELECTRICAL CHARACTERISTICS FOR BYTE ERASE AND BYTE WRITE OPERATIONS**

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{CW}[3]	250	-	-	ns	
	t_{WP}[2]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Note: 1. Use this device in a longer cycle than this value.
2. WE controlled operation.
3. CE controlled operation.

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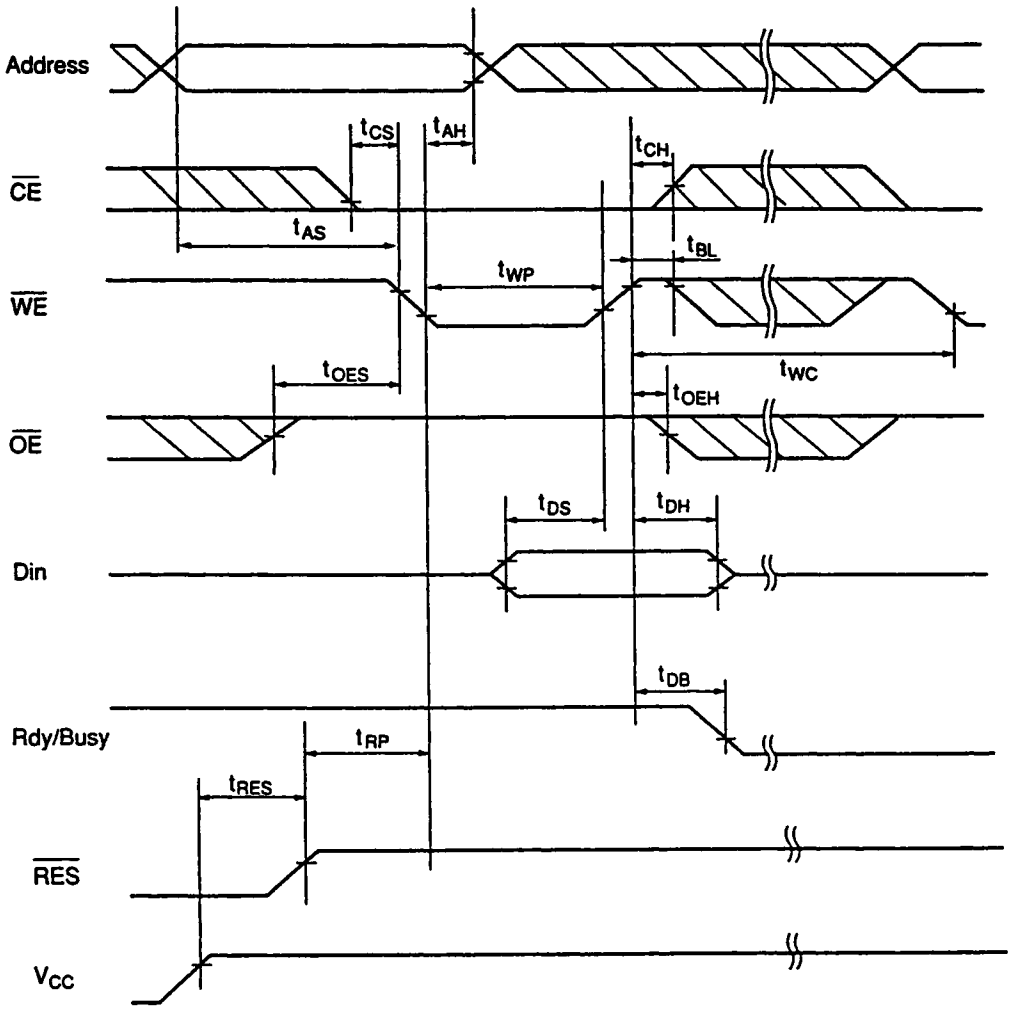
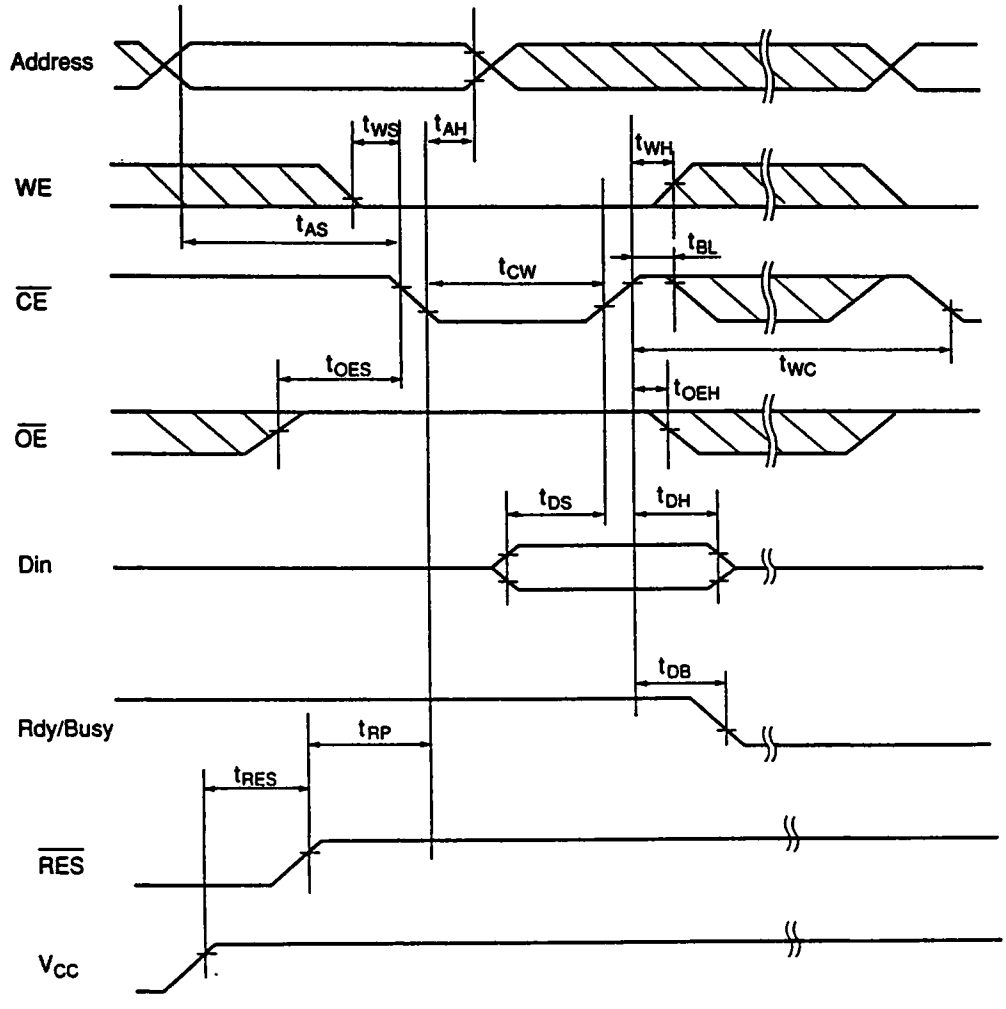
■ BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)



(TD.BE1.HN58C1001)

■ **BYTE ERASE AND BYTE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)**



(TD.BE2.HN58C1001)

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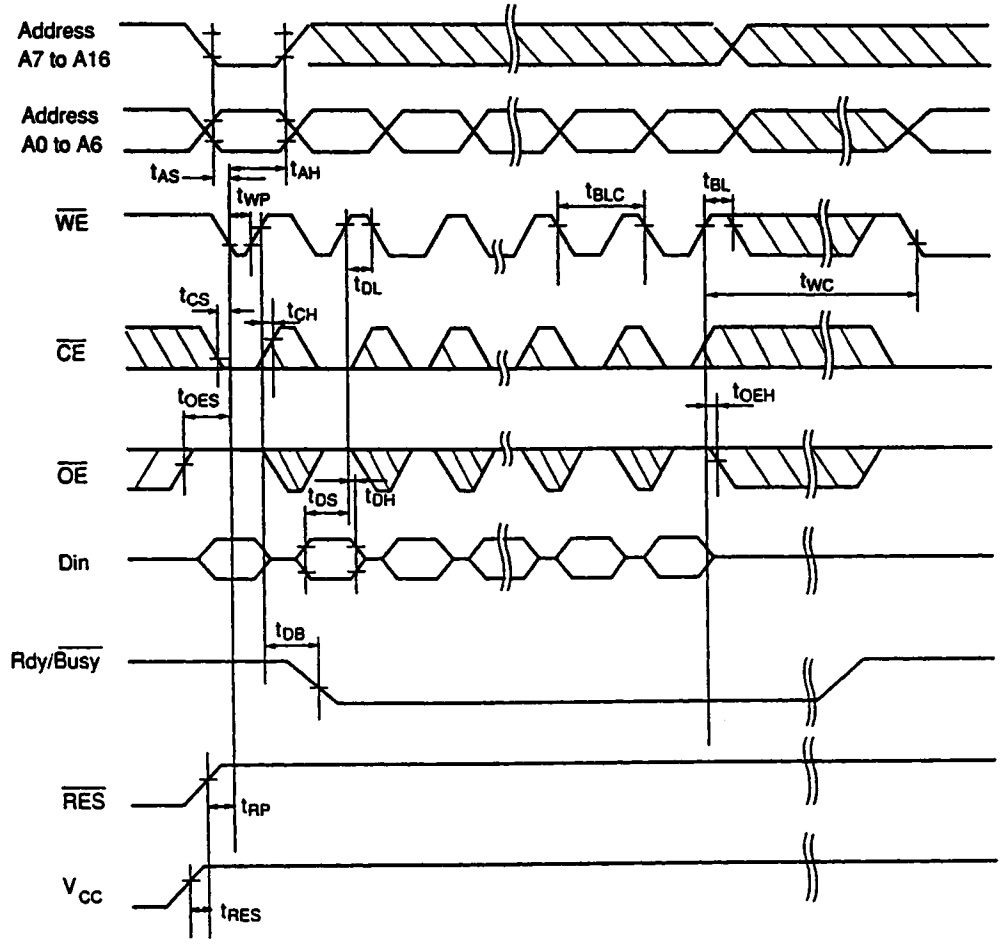
■ AC ELECTRICAL CHARACTERISTICS FOR PAGE ERASE AND PAGE WRITE OPERATIONS

Item	Symbol	Min.[1]	Typ.	Max.	Unit	Test Condition
Address Setup Time	t_{AS}	0	-	-	ns	
Write Enable to Write Setup Time	t_{WS}[3]	0	-	-	ns	
Chip Enable to Write Setup Time	t_{CS}[2]	0	-	-	ns	
Write Pulse Width	t_{WP}[2]	250	-	-	ns	
	t_{CW}[3]	250	-	-	ns	
Address Hold Time	t_{AH}	150	-	-	ns	
Data Setup Time	t_{DS}	100	-	-	ns	
Data Hold Time	t_{DH}	10	-	-	ns	
Write Enable Hold Time	t_{WH}[3]	0	-	-	ns	
Chip Enable Hold Time	t_{CH}[2]	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Data Latch Time	t_{DL}	200	-	-	ns	
Write Cycle Time	t_{WC}	10	-	-	ms	
Byte Load Window	t_{BL}	100	-	-	µs	
Byte Load Cycle	t_{BLC}	0.55	-	30	µs	
Time to Device Busy	t_{DB}	120	-	-	ns	
$\overline{RES}$ to Write Setup Time	t_{RP}	100	-	-	µs	
V_{CC} to $\overline{RES}$ Setup Time	t_{RES}	1	-	-	µs	

Notes: 1. Use this device in longer cycle than this value.
2. $\overline{WE}$ controlled operation.
3. $\overline{CE}$ controlled operation.

■ **PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{WE}$ Controlled)**



(TD.PE1.HN58C1001)

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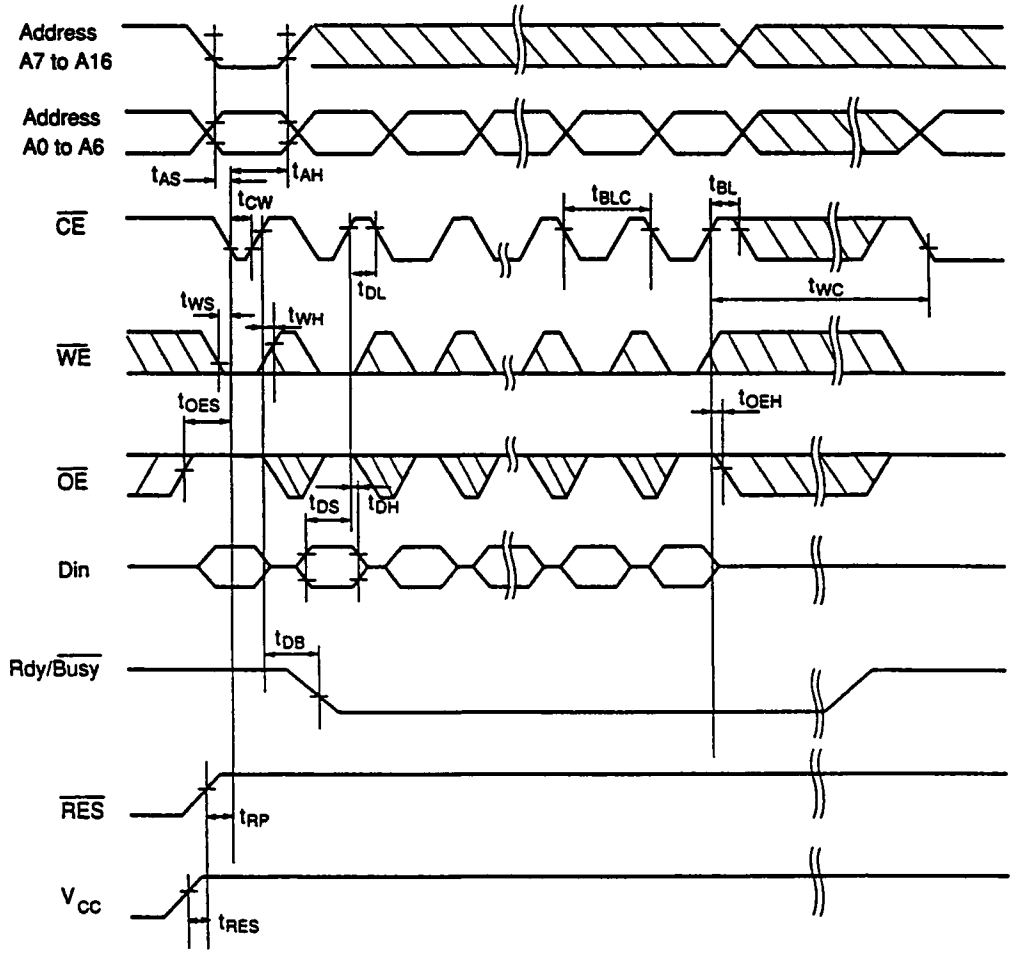
■ **PAGE ERASE AND PAGE WRITE TIMING WAVEFORM ($\overline{CE}$ Controlled)**

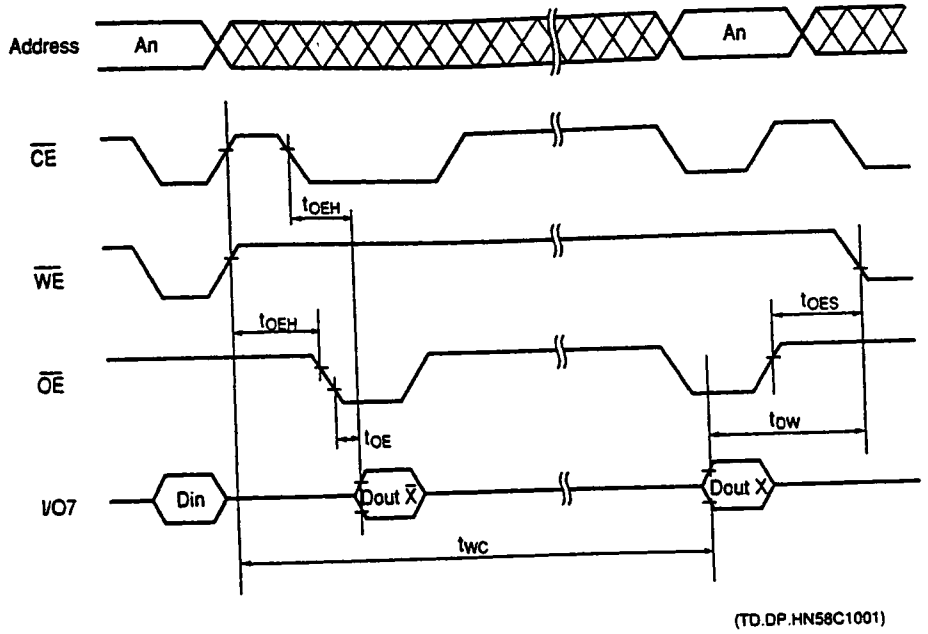


(TD.PE2.HN58C1001)

■ AC ELECTRICAL CHARACTERISTICS FOR $\overline{\text{DATA}}$ POLLING OPERATION

Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Output Enable Hold Time	t_{OEH}	0	-	-	ns	
Output Enable to Write Setup Time	t_{OES}	0	-	-	ns	
Write Start Time	t_{DW}	150	-	-	ns	
Write Cycle Time	t_{WC}	-	-	10	ms	

■ $\overline{\text{DATA}}$ POLLING TIMING WAVEFORM



(TD.DP.HN58C1001)

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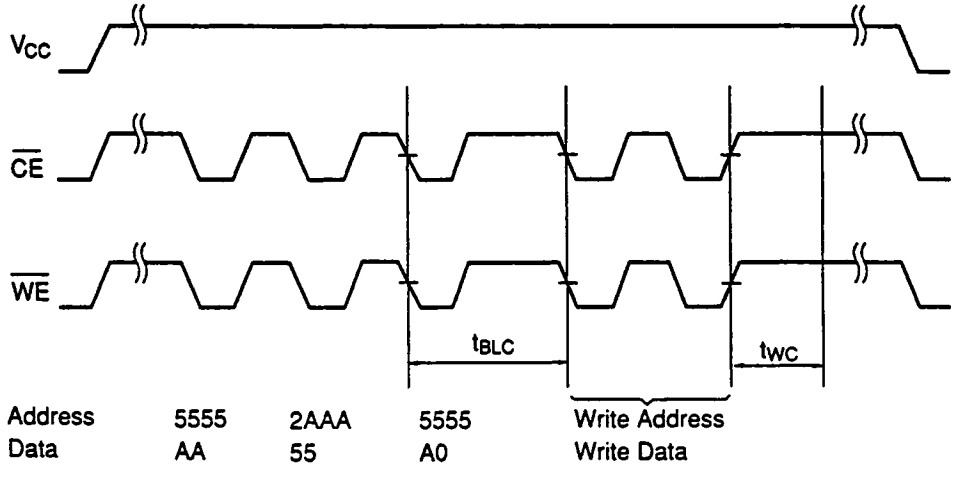
■ AC ELECTRICAL CHARACTERISTICS FOR SOFTWARE DATA PROTECTION CYCLE OPERATION

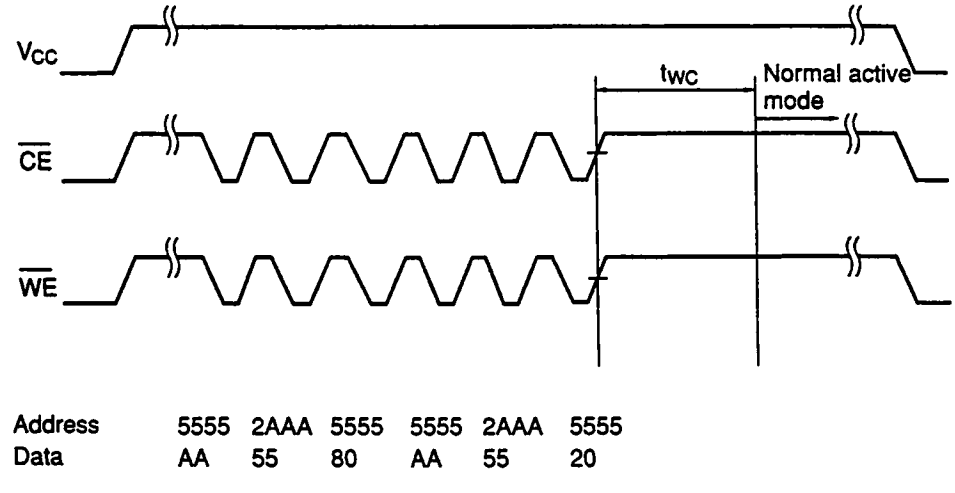
Item	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Byte Load Cycle Time	t_{BLC}	0.55	-	30	µs	
Write Cycle Time	t_{WC}	10	-	-	ms	

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Protection Mode)



(TD.SD1.HN58C1001)

■ SOFTWARE DATA PROTECTION TIMING WAVEFORM (Non-Protection Mode)



(TD.SD2.HN58C1001)

■ FUNCTIONAL DESCRIPTION

Automatic Page Write

The Page Write feature allows 1 to 128 Bytes of data to be written into the EEPROM in a single cycle and allows the undefined data within 128 Bytes to be written corresponding to the undefined address (A_0 to A_6). Loading the first Byte of data, the data load window of 30 µs opens for the second. In the same manner each additional Byte of data can be loaded within 30 µs. In case $\overline{CE}$ and $\overline{WE}$ are kept high for 100 µs after data input, the EEPROM enters erase and write automatically and only the input data are written into the EEPROM. In Page mode the data can be written and accessed 10^5 times per page, and in Byte mode 10^4 times per Byte.

$\overline{\text{Data}}$ Polling

$\overline{\text{Data}}$ Polling allows the status of the EEPROM to be determined. If the EEPROM is set to Read mode during a Write cycle, an inversion of the last Byte of data to be loaded outputs from I/O_7 to indicate that the EEPROM is performing a Write operation.

Write Protection

(1) Noise protection: Noise on a write cycle will not act as a trigger with a $\overline{WE}$ pulse of less than 20 ns.

(2) Write inhibit: Holding $\overline{OE}$ low, $\overline{WE}$ high, or $\overline{CE}$ high, inhibits a write cycle during power on/off.

$\overline{WE}$ and $\overline{CE}$ Pin Operation

During a write cycle, addresses are latched by the falling edge of $\overline{WE}$ or $\overline{CE}$, and data is latched by the rising edge of $\overline{WE}$ or $\overline{CE}$.

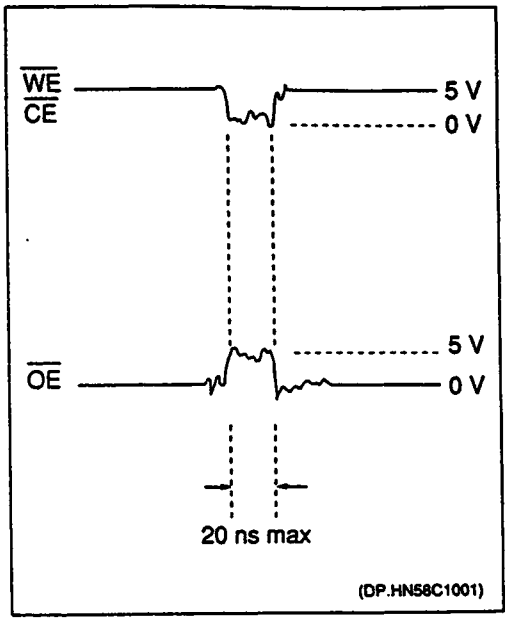
Write/Erase Endurance and Data Retention

The endurance with page programming is 10^5 cycles (1% cumulative failure rate) and the data retention time is more than 10 years when a device is programmed less than 10^4 cycles.

Data Protection

To protect the data during operation and power on/off, the HN58C1001 has:

1. Data protection against Noise on Control Pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) during Operation.
   During readout or standby, noise on the control pins may act as a trigger and turn the EEPROM to programming mode by mistake. To prevent this phenomenon, the HN58C1001 has a noise cancellation function that cuts noise if its width is 20 ns or less in programming mode. Be careful not to allow noise of a width of more than 20 ns on the control pins.



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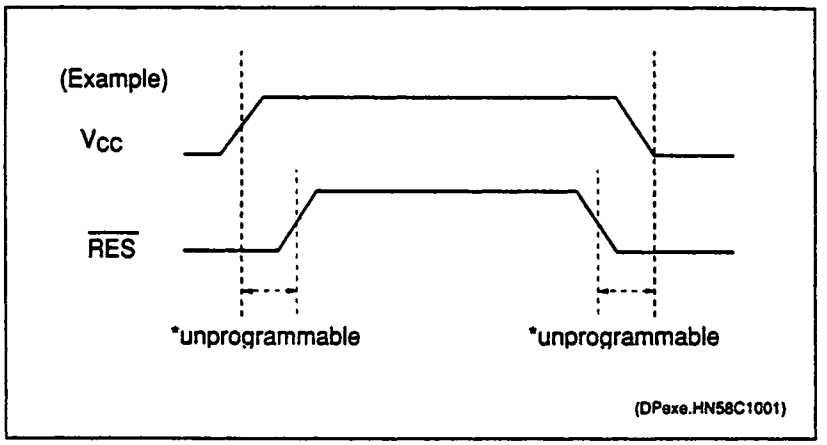

■ **FUNCTIONAL DESCRIPTION (continued)**

Data Protection (continued)

2. Data protection at V_{cc} on/off
   When $\overline{RES}$ is low, the EEPROM cannot be erased and programmed. Therefore, data can be protected by keeping $\overline{RES}$ low when V_{cc} is switched. $\overline{RES}$ should be high during programming because it does not provide a latch function.
   When V_{cc} is turned on or off, noise on the control pins generated by external circuits (CPU, etc) may turn the EEPROM to programming mode by mistake. To prevent this unintentional programming, the EEPROM must be kept in an unprogrammable, standby or readout state by using a CPU reset signal to $\overline{RES}$ pin.
   In addition, when $\overline{RES}$ is kept high at V_{cc} on/off timing, the input level of control pins ($\overline{CE}$, $\overline{OE}$, $\overline{WE}$) must be held as $\overline{CE}$=V_{cc} or $\overline{OE}$=Low or $\overline{WE}$=V_{cc} level.

3. Software data protection
   To prevent unintentional programming caused by noise generated by external circuits, HN58C1001 has a Software data protection function. In Software data protection mode, 3 Bytes of data must be input before the Write data. These Bytes can switch the Non-Protection mode to the Protection mode.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	A0
⇓	⇓
Write Address	**Write Data**

(Normal Data Input)

The Software data protection mode can be cancelled by inputting the following 6 Bytes. This changes the HN58C1001 turns to the Non-Protection mode and it can write data normally. When the data is input during the cancelling cycle, the data cannot be written.

Address	Data
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	80
⇓	⇓
5555	AA
⇓	⇓
2AAA	55
⇓	⇓
5555	20