REVISIONS

Letter	ECO No.	Description	Checked	Approved	Date
A	36-104	INITIAL RELEASE	DG	EAB	8/15/94
B	36-111	INCORPORATE MSFC AND VENDOR COMMENTS	DG	KT/EAB	11/7/90
C	36-154	ADD PINOUTS AND PACKAGE DRAWING	DG	RFG	3/30/95
D	36-460	Altered AC/DC limits; Changed some delta limits; Sampled some tests	DG	RFG	1/20/96
E	36-603	CORRECT CAPACITANCE SAMPLE TEST CONDITIONS	DG.	[illegible]	4/24/96

NAME	DATE
Drawn: BRIAN KLATT	8/5/94
Checked: D. Gordon	8/19/94
Approved: Ed Boughan	8/19/94
Released: K Tibbetts	8/19/94

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CENTER FOR SPACE RESEARCH

MICROCIRCUIT MODULE (MCM), 1M X 12-BIT MEMORY ARRAY, FB MODULE

Size	Code Identification No.	Drawing No.	Rev.
T	80230	36-02303	E

Scale: NONE

Sheet: 1 of 11

1.0 SCOPE

1.1 Introduction This drawing describes device requirements for a radiation tolerant processed, 1M X 12 bit memory array, microcircuit module, used in flight hardware for a space experiment on the AXAF CCD Imaging Spectrometer (ACIS) Instrument. The part described herein utilizes twelve (12) Micron MT5C1005 dice, packaged in a 42 lead metal flat pack. This device is called the FB Module.

1.2 Part Number The complete MIT part number shall be 36-02303

1.3 Absolute Maximum Ratings *

Supply voltage range (V_{DD}).......-0.5 Vdc to +7.0 Vdc
DC input voltage range (V_{IN}).......-0.5 Vdc to V_{DD}
DC output voltage range ($V_{of\ data\ 0\text{-}11}$).......-0.5 Vdc to V_{DD}
Storage temperature range.......-65°C to +150°C
Output voltage applied to high Z state.......-0.3 Vdc to V_{DD}
Maximum junction temperature.......+150°C

1.4 Recommended operation conditions *

Supply voltage range (V_{DD}).......+4.5 Vdc to +5.5 Vdc
Ground (V_{SS}).......0.0 Vdc
High level input voltage range (V_{IH}).......3.5 Vdc to V_{CC}
Low level input voltage range (V_{IL}).......-0.3 Vdc to 0.8 Vdc
Case operating temperature range (T_C).......-55°C to +125°C

* All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified

2.0 APPLICABLE DRAWINGS

2.1 Government Specifications and Standards Unless otherwise specified, the following specifications and standards, of the latest released issue, form a part of this drawing, to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-H-38534 Hybrid Microcircuits, General Specification for

STANDARDS

MIL-STD-883 Test Methods and Procedures for Microelectronics
5962-92153 Microcircuit, Digital CMOS, 32K X 8 Static Random Access Memory (SRAM), Monolithic Silicon

2.2 Order of precedence In the event of conflict between the text of this drawing and the references cited herein, the text of this drawing shall govern.

3.0 REQUIREMENTS

3.1 General Requirements

3.1.1 Item Requirements The microcircuits described herein shall, in all respects, meet the requirements of this specification. Processes and procedures per MIL-H-38534, level H, option 1, shall be as specified herein. These microcircuits shall be fabricated and tested using production and test facilities and a Reliability and Quality Assurance program adequate to assure successful compliance with this specification and the intent of MIL-H-38534. Alternate element evaluation per paragraph 4.3.5 of MIL-H-38534 is acceptable.

3.1.2 Procuring Activity For the purposes of this specification and documents referenced herein, the procuring activity is the Massachusetts Institute of Technology (MIT), Center for Space Research (CSR).

3.1.3 Product Changes The supplier(s) shall notify MIT of proposed changes to Microcircuits, including changes in design, materials, fabrication methods, or processes, and changes which may affect the quality or intended end use.

3.2 Part marking Microcircuit marking shall meet the requirements of paragraph 3.6 of MIL-H-38534, excluding subparagraph "i".

3.2.1 Part Number Microcircuits shall be marked with the MIT part number; 36-02303.

3.4 Design and Construction Requirements

3.4.1 Package The package shall be a 42-lead metal flat pack. Leads shall be formed, after final electrical test, for surface mounting on a printed circuit board. Device hermeticity shall be tested after lead forming.

3.4.2. Lead Finish The lead finish shall be "A" per paragraph 3.6.2.4 of MIL-H-38534.

3.4.3 Terminal connections The terminal connections shall be per figure 2 herein.

3.4.4 Electrical Performance The electrical performance shall be as detailed in tables 1, 2, and 3 herein.

3.5 Electrical circuit Design The circuit design shall be in accordance with figure 1 herein.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection Unless otherwise specified herein, the assembly/packaging manufacturer is responsible for the performance of all examinations and tests as specified herein.

4.2 Screening All Microcircuits (100%) shall be subjected to and pass the screen tests and examinations defined in paragraph 4.5 of MIL-H-38534. Burn-in shall be performed at +125°C for 160 hours minimum.

4.2.1 Electrical Performance Tests All Microcircuits (100%) shall be subjected to and pass the electrical performance tests detailed in tables 1, 2, and 3 herein.

4.2.2 Xray All Microcircuits (100%) shall be subjected to and pass radiographic examination per MIL-STD-883, method 2012.

Table 1

DC ELECTRICAL PERFORMANCE

TEST	SYMBOL	CONDITIONS T_C = -55°C, 25°C, +125°C	LIMITS		UNITS
			MIN	MAX	
Input High Voltage	V_{IH}	V_{DD} = 5.0V	2.2		Volts
Input Low Voltage	V_{IL}	V_{DD} = 5.0V		0.8	Volts
Output high Voltage	V_{OH}	V_{DD} = 5.0V, I_{OH} = -4mA	2.4		Volts
Output Low Voltage	V_{OL}	V_{DD} = 5.0V, I_{OL} = 8mA		0.4	Volts
Dynamic Operating Current	I_{DD}	f_{RC} = 1 MHz, all inputs switching; V_{DD} = 5.0V		200	mA
Standby Supply Current	I_{SB}	V_{DD} = 5.0V; All Inputs at 0.2 V below V_{DD}		20	mA
Input Capacitance	C_{IH} 1/	V_{DD} = 5.0V, V_I = 0 V		200	pF
Output Capacitance	C_{OUT} 1/	V_{DD} = 5.0V, $V_{I/O}$ = 0 V		200	pF

NOTE: Run DC Electrical Performance Tests while applying checkerboard algorithm or equivalent.

1/ These parameters may be sample tested at 25°C only. The sample size is 5 parts or 10%, whichever is greater

Table 2

READ CYCLE AC ELECTRICAL PERFORMANCE *

See figure 5 of 5962-92153 for timing waveforms

TEST	SYMBOL	CONDITIONS T_C = -55°C, 25°C, +125°C	LIMITS		UNITS
			MIN	MAX	
Address Access Time	T_{AVQV}	V_{DD} = 4.5V, 5.0V, & 5.5V		35	ns
Chip Select Access Time	T_{SLQV}	V_{DD} = 4.5V, 5.0V, & 5.5V		35	ns
Output Enable Access Time	T_{GLQV}	V_{DD} = 4.5V, 5.0V, & 5.5V		12	ns
Output Hold after Address Change	T_{AXQX} 2/	V_{DD} = 4.5V, 5.0V, & 5.5V	5		ns
Chip Select to Output Disable	T_{SHQZ} 2/	V_{DD} = 4.5V, 5.0V, & 5.5V		15	ns
Output Enable to Output Disable	T_{GHQZ} 2/	V_{DD} = 4.5V, 5.0V, & 5.5V		12	ns

2/ These parameters may be sample tested. The sample size is 5 parts or 10%, whichever is greater

Table 3

WRITE CYCLE AC ELECTRICAL PERFORMANCE *

TEST	SYMBOL	CONDITIONS T_C = -55°C, 25°C, +125°C	LIMITS MIN	LIMITS MAX	UNITS
Chip Select to End of Write	T_{SLWH}	V_{DD} = 4.5V, 5.0V, & 5.5V	20		n s
Address Setup to End of Write	T_{AVWH}	V_{DD} = 4.5V, 5.0V, & 5.5V	20		n s
Address Setup to Start of Write	T_{AVWL}	V_{DD} = 4.5V, 5.0V, & 5.5V	0		n s
Write Pulse Width	T_{WLWH}	V_{DD} = 4.5V, 5.0V, & 5.5V	20		n s
Data Hold after End of Write	T_{WHDX}	V_{DD} = 4.5V, 5.0V, & 5.5V	0		n s
Data Setup to End of Write	T_{DVWH}	V_{DD} = 4.5V, 5.0V, & 5.5V	15		n s

* **NOTE:** Run Write Cycle AC Electrical Performance Tests while applying checkerboard, march, X-Y march, and CEDES-CE algorithms. See figure 5 of 5962-92153 for timing waveforms.

Table 4

Parameter Delta Limits

TEST	SYMBOL	CONDITIONS T_C = 25°C,	Δ LIMITS MAX	UNITS
Dynamic Operating Current	I_{DD}	f_{RC} = 1 MHz, all inputs switching; V_{DD} = 5.0V	5	%
Standby Supply Current	I_{SB}	All Inputs at 0.2 V below V_{DD} V_{DD} = 5.0V	5% or 50 µA, whichever is greater	% or µA
Output high Voltage	V_{OH}	V_{DD} = 5.0V	.1	Volts
Output Low Voltage	V_{OL}	V_{DD} = 5.0V	.1	Volts

4.2.3 Particle Impact Noise Detection (PIND) All Microcircuits (100%) shall be subjected to and pass PIND examination per MIL-STD-883, method 2020, condition B.

4.3 Quality Conformance Inspection (QCI) Quality conformance inspection shall be in accordance with paragraph 4.7 of MIL-H-38534, level H, option 1.

4.4 Destructive Physical Analysis (DPA) An internal destructive examination shall be performed in accordance with paragraph 3.5, of MIL-STD-883, method 5009. An electrical reject shall be used for DPA. Sample size shall be one (1) piece.

4.5 Inspection and Test Records The supplier shall maintain inspection and test records for 36 months after hardware delivery to MIT. Test data for all electrical tests, screening, DPA, and QCI inspections shall be submitted to MIT with the delivery of flight parts.

4.6 Source Inspection

4.6.1 Government Source Inspection (GSI) The government has the right to inspect any or all of the work included in this order at the supplier's plant. In the event that Government Source Inspection (GSI) is imposed, the Government quality representative who has been delegated NASA quality assurance functions for this procurement shall be notified immediately upon receipt of this order. The Government representative shall also be notified 48 hours in advance of the time that parts are ready for inspection or test.

4.6.2 MIT Source Inspection MIT Performance Assurance will impose mandatory inspection points (MIPs) at wire bonding (precap visual examination) and final test, and must be notified 2 weeks before parts are ready for MIT Inspection. (call area code 617, phone 253-7555).

5.0 PACKAGING

5.1 Packaging requirements Packaging shall be in accordance with paragraph 5.1 of MIL-H-38534.

6.0 NOTES

6.1 Approved Source of Supply

Teledyne Electronic Technologies
12964 Panama Street
Los Angeles, CA 90066

Cage Code 16170

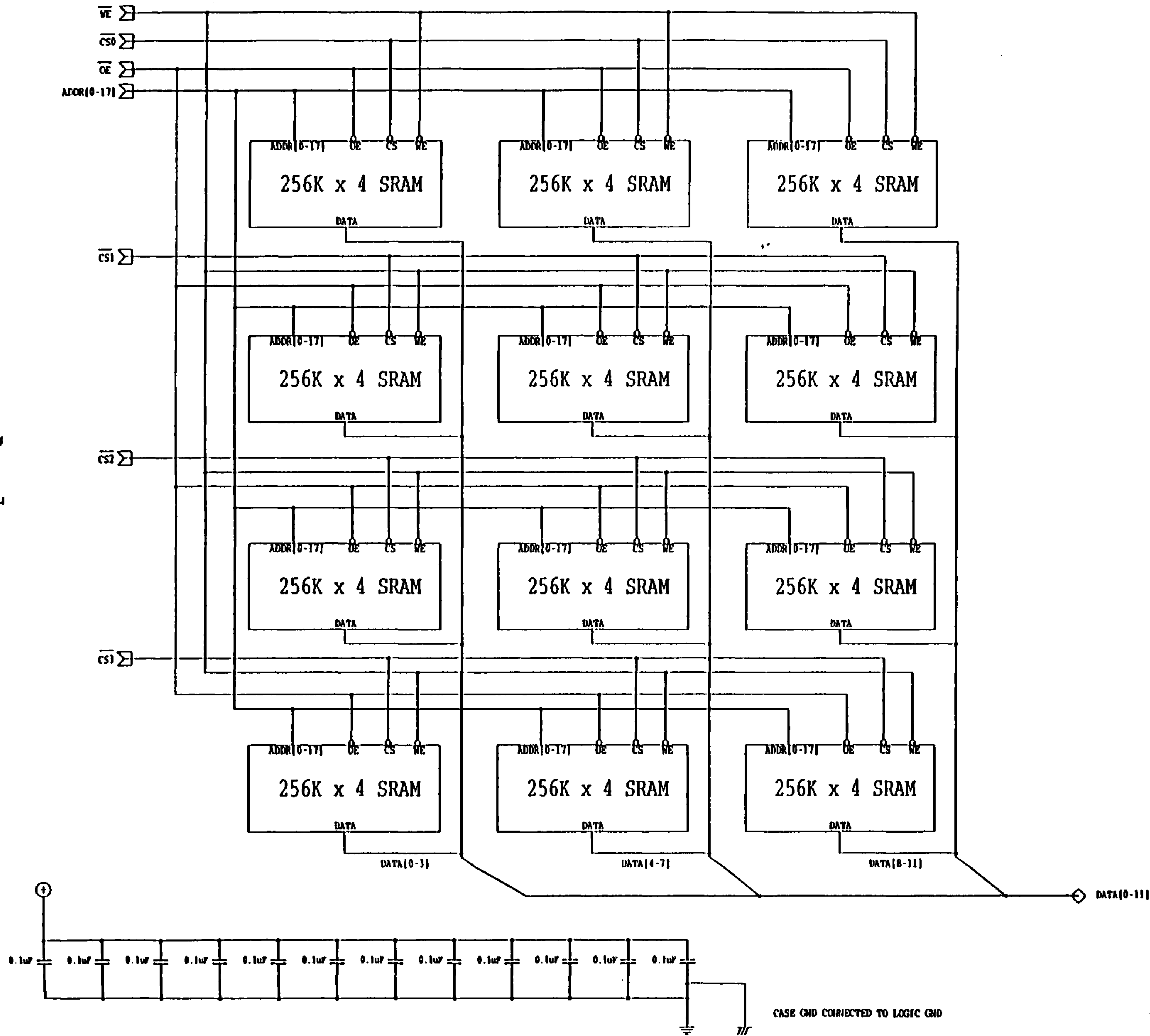
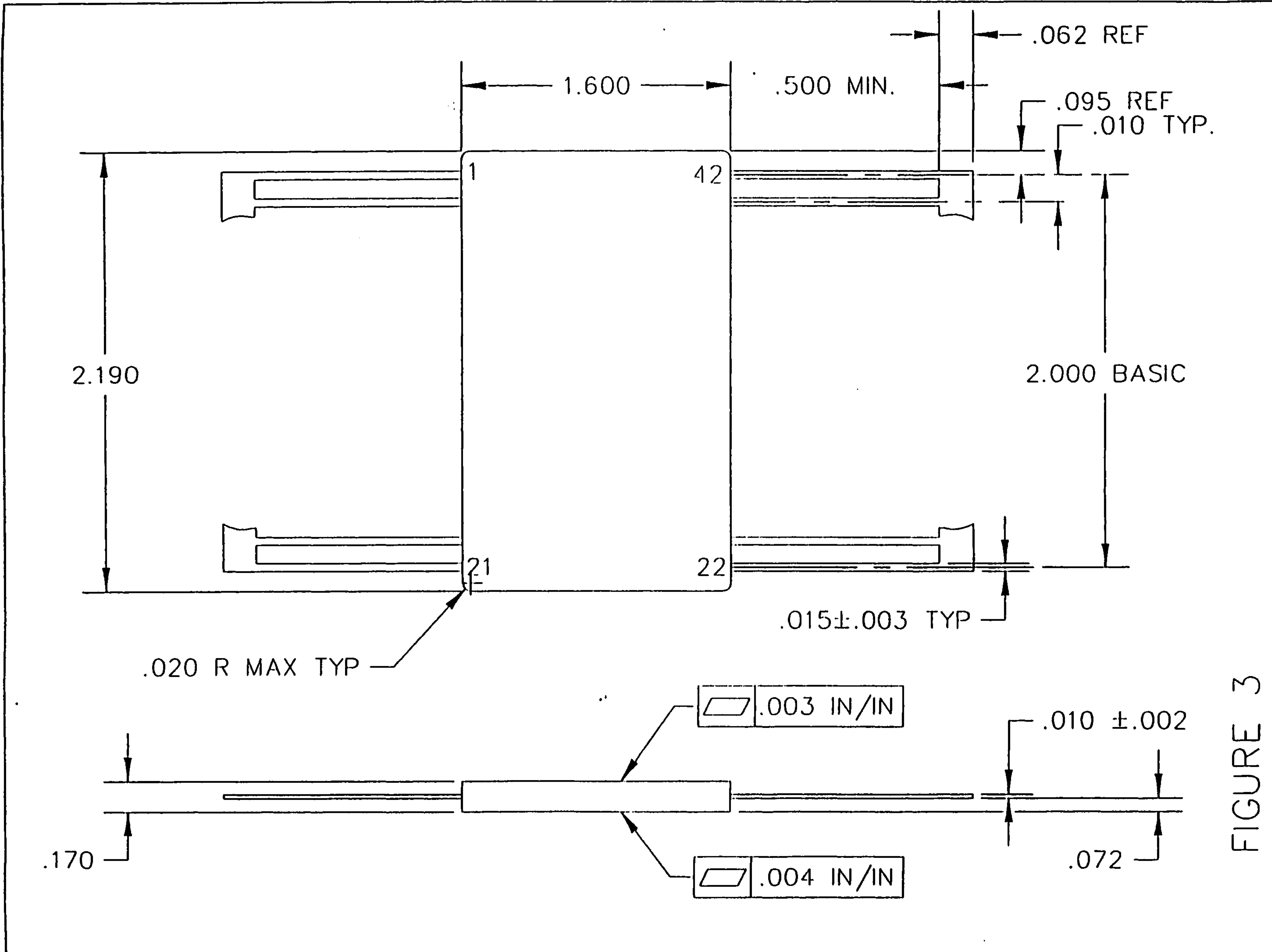


FIGURE 1
CIRCUIT SCHEMATIC

FIGURE 2

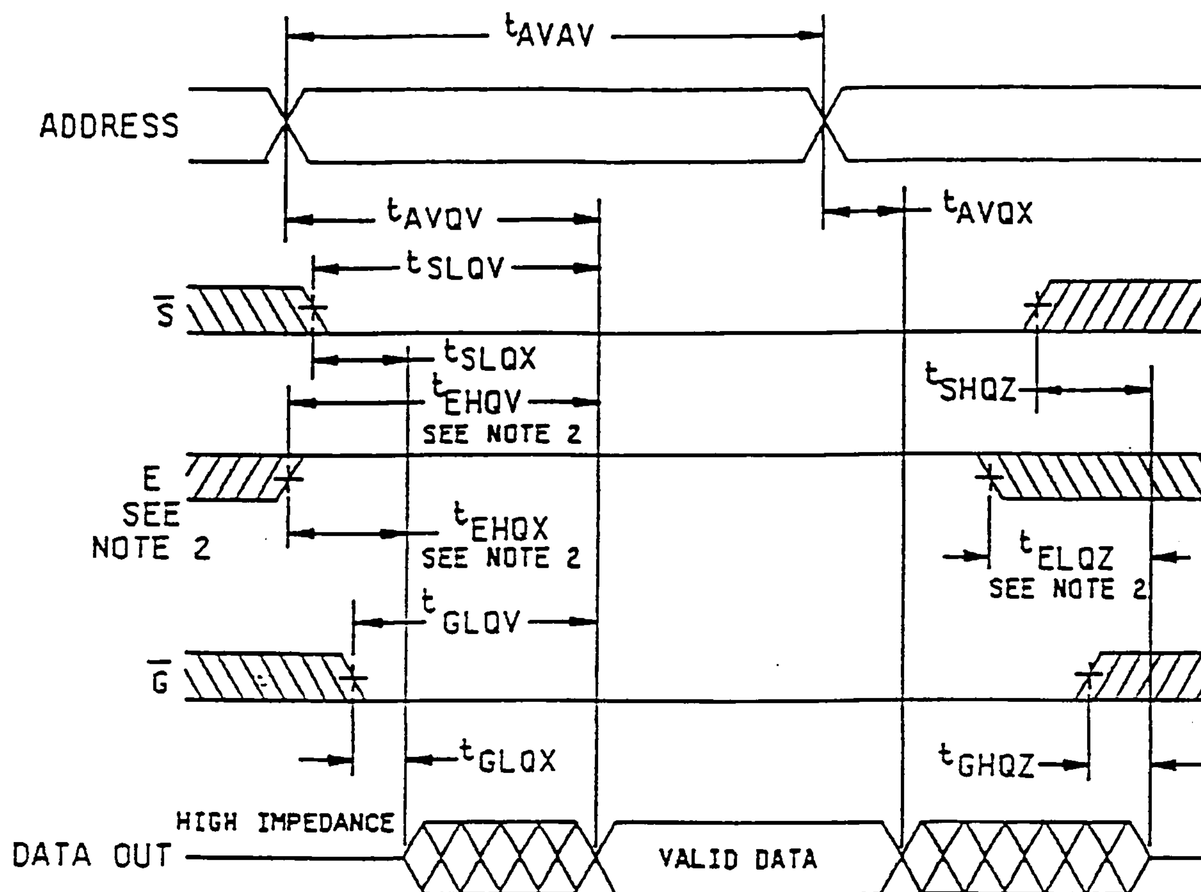
TERMINAL CONNECTIONS

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1	CASE GND	22	GND
2	A00	23	D00
3	A01	24	D01
4	A02	25	D02
5	A03	26	D03
6	A04	27	CE0N
7	A05	28	CE1N
8	A06	29	0EN
9	A07	30	D04
10	A08	31	D05
11	GND	32	GND
12	VDD	33	VDD
13	A09	34	D06
14	A10	35	D07
15	A11	36	WEN
16	A12	37	CE3N
17	A13	38	CE2N
18	A14	39	D08
19	A15	40	D09
20	A16	41	D10
21	A17	42	D11



.062 REF
1.600
.500 MIN.
.095 REF
.010 TYP.
1
42
2.190
2.000 BASIC
21
22
.015±.003 TYP
.020 R MAX TYP
.003 IN/IN
.010 ±.002
.004 IN/IN
.170
.072
REV.
SHEET 9
DWG. NO.
36-02303
SIZE
A
FSCM NO.
80230
SCALE
NONE
FIGURE 3
PACKAGE OUTLINE

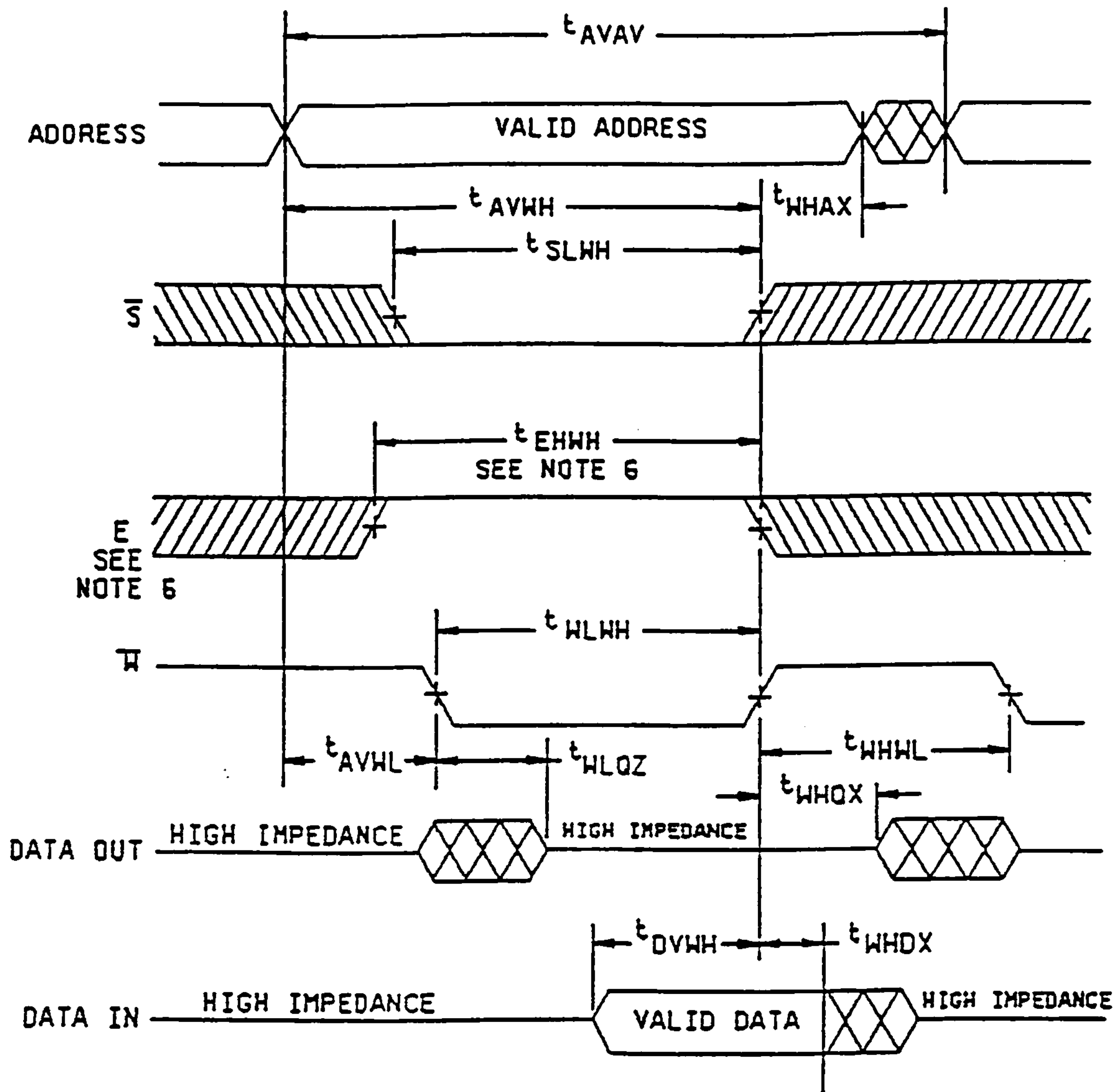
Read cycle (see note 1)



NOTE:
1. $\overline{W}$ is high for read cycle.
2. E and timing parameters t_{EHQV}, t_{EHQX}, t_{ELQZ} do not apply to device types 09 and 10.

FIGURE 5. Timing waveforms.

Write cycle (see notes 1, 2, 3, 4, and 5)



NOTES:

1. Write cycle data is latched by the first occurrence of $\overline{S}$ high, E low or $\overline{W}$ high.
2. S high, E low, or W high must occur while address transitions.
3. Write cycle time is guaranteed for toggling $\overline{S}$ and E or holding $\overline{S}$ or E, or both, in active state.
4. The worst case timing sequence of $t_{WLQZ} + t_{DVWH} + t_{WHWL}$ = the write cycle time (t_{AVAV}).
5. G high will eliminate the I/O output from becoming active (t_{WLQZ}).
6. E and timing parameter t_{EHWH} do not apply to device types 09 and 10.

FIGURE 5. Timing waveforms - continued.