

REVISIONS

Letter	ECO No.	Description	Checked	Approved	Date
A	36-103	INITIAL RELEASE	DG	EAB	8/15/94
B	36-110	INCORPORATE MSFC AND VENDOR COMMENTS	DG	KT/EAB	11/7/94
C	36-154	ADD PINOUTS AND PACKAGE DRAWING	DG	RFG	3/30/95
D	36-460	Altered AC/DC limits; Changed some delta limits; Sampled some tests	DG	RFG	1/20/96
E	36-603	CORRECT CAPACITANCE SAMPLE TEST CONDITIONS	<i>JG</i>	<i>07/26/94</i>	<i>4/24/94</i>

NAME	DATE	MASSACHUSETTS INSTITUTE OF TECHNOLOGY CENTER FOR SPACE RESEARCH			
Drawn: BRIAN KLATT	8/4/94	MICROCIRCUIT MODULE (MCM), 32K X 32-BIT MEMORY ARRAY, CA MODULE			
Checked: D. Gordon	8/9/94				
Approved: Ed Boughan	8/19/94				
Released: K Tibbetts	8/19/94				
		Size	Code Identification No.	Drawing No.	Rev.
		T	80230	36-02302	E
		Scale: NONE		Sheet: 1 of 11	

1.0 SCOPE

1.1 Introduction This drawing describes device requirements for a radiation hard processed, 32K X 8 bit memory array, microcircuit module, used in flight hardware for a space experiment on the AXAF CCD Imaging Spectrometer (ACIS) Instrument. The part described herein utilizes four (4) Honeywell H6856 dice or equivalent, packaged in an 82 lead metal flat pack. This device is called the CA Module.

1.2 Part Number The complete MIT part number shall be 36-02302

1.3 Absolute Maximum Ratings *

Supply voltage range (V_{DD}).....	-0.5 Vdc to +7.0 Vdc
DC input voltage range (V_{IN})	-0.5 Vdc to V_{DD}
DC output voltage range ($V_{of\ data\ 0-31}$).....	-0.5 Vdc to V_{DD}
Storage temperature range	-65°C to +150°C
Output voltage applied to high Z state	-0.3 Vdc to V_{DD}
Maximum junction temperature.....	+150°C

1.4 Recommended operation conditions *

Supply voltage range (V_{DD}).....	+4.5 Vdc to +5.5 Vdc
Ground (V_{SS})	0.0 Vdc
High level input voltage range (V_{IH})	3.5 Vdc to V_{DD}
Low level input voltage range (V_{IL})	-0.3 Vdc to 0.8 Vdc
Case operating temperature range (T_C).....	-55°C to +125°C

* All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified

2.0 APPLICABLE DRAWINGS

2.1 Government Specifications and Standards Unless otherwise specified, the following specifications and standards, of the latest released issue, form a part of this drawing, to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-H-38534 Hybrid Microcircuits, General Specification for

STANDARDS

MIL-STD-883 Test Methods and Procedures for Microelectronics
5962-92153 Microcircuit, Digital CMOS, 32K X 8 Static Random Access Memory (SRAM), Monolithic Silicon

2.2 Order of precedence In the event of conflict between the text of this drawing and the references cited herein, the text of this drawing shall govern.

3.0 REQUIREMENTS

3.1 General Requirements

3.1.1 **Item Requirements** The microcircuits described herein shall, in all respects, meet the requirements of this specification. Processes and procedures per MIL-H-38534, level H, option 1, shall be as specified herein. These microcircuits shall be fabricated and tested using production and test facilities and a Reliability and Quality Assurance program adequate to assure successful compliance with this specification and the intent of MIL-H-38534. Alternate element evaluation per paragraph 4.3.5 of MIL-H-38534 is acceptable.

3.1.2 **Procuring Activity** For the purposes of this specification and documents referenced herein, the procuring activity is the Massachusetts Institute of Technology (MIT), Center for Space Research (CSR).

3.1.3 **Product Changes** The supplier(s) shall notify MIT of proposed changes to Microcircuits, including changes in design, materials, fabrication methods, or processes, and changes which may affect the quality or intended end use.

3.2 **Part marking** Microcircuit marking shall meet the requirements of paragraph 3.6 of MIL-H-38534, excluding subparagraph "i".

3.2.1 **Part Number** Microcircuits shall be marked with the MIT part number; 36-02302.

3.4 Design and Construction Requirements

3.4.1 **Package** The package shall be an 82 lead metal flat pack. Leads shall be formed, after final electrical test, for surface mounting on a printed circuit board. Device hermetically shall be tested after lead forming.

3.4.2. **Lead Finish** The lead finish shall be "A" per paragraph 3.6.2.4 of MIL-H-38534.

3.4.3 **Terminal connections** The terminal connections shall be per figure 2 herein.

3.4.4 **Electrical Performance** The electrical performance shall be as detailed in tables 1, 2, and 3 herein.

3.5 **Electrical circuit Design** The circuit design shall be in accordance with figure 1 herein.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 **Responsibility for Inspection** Unless otherwise specified herein, the assembly/packaging manufacturer is responsible for the performance of all examinations and tests as specified herein.

4.2 **Screening** All Microcircuits (100%) shall be subjected to and pass the screen tests and examinations defined in paragraph 4.5 of MIL-H-38534. Burn-in shall be performed at +125°C for 160 hours minimum.

4.2.1 **Electrical Performance Tests** All Microcircuits (100%) shall be subjected to and pass the electrical performance tests detailed in tables 1, 2, and 3 herein.

4.2.2 Xray All Microcircuits (100%) shall be subjected to and pass radiographic examination per MIL-STD-883, method 2012.

Table 1
DC ELECTRICAL PERFORMANCE

TEST	SYMBOL	CONDITIONS $T_C = -55^\circ\text{C}, 25^\circ\text{C}, +125^\circ\text{C}$	LIMITS		UNITS
			MIN	MAX	
Input High Voltage	V_{IH}	$V_{DD} = 5.0\text{V}$	2.2		Volts
Input Low Voltage	V_{IL}	$V_{DD} = 5.0\text{V}$		0.8	Volts
Output high Voltage	V_{OH}	$V_{DD} = 5.0\text{V}, I_{OH} = -5\text{mA}$	4.2		Volts
Output Low Voltage	V_{OL}	$V_{DD} = 5.0\text{V}, I_{OL} = 10\text{mA}$		0.4	Volts
Dynamic Operating Current	I_{DD}	$f_{RC} = 1\text{ MHz}$, all inputs switching; $V_{DD} = 5.0\text{V}$		100	mA
Standby Supply Current	I_{SB}	$V_{DD} = 5.0\text{V}$; All Inputs at 0.2 V below V_{DD}		5.0	mA
Input Capacitance	C_{IH} 1/	$V_{DD} = 5.0\text{V}, V_I = 0\text{V}$		90	pF
Output Capacitance	C_{OUT} 1/	$V_{DD} = 5.0\text{V}, V_{IO} = 0\text{V}$		90	pF

NOTE: Run DC Electrical Performance Tests while applying checkerboard algorithm or equivalent.

1/ These parameters may be sample tested at 25°C only. The sample size is 5 parts or 10%, whichever is greater

Table 2

READ CYCLE AC ELECTRICAL PERFORMANCE *

See figure 5 of 5962-92153 for timing waveforms

TEST	SYMBOL	CONDITIONS $T_C = -55^\circ\text{C}, 25^\circ\text{C}, +125^\circ\text{C}$ $V_{DD} = 4.5\text{V}, 5.0\text{V}, \& 5.5\text{V}$	LIMITS		UNITS
			MIN	MAX	
Address Access Time	T_{AVOQ}			35	n s
Chip Select Access Time	T_{SLOV}			35	n s
Output Enable Access Time	T_{GLOV}			13	n s
Output Hold after Address Change	T_{AXQX} 2/		3		n s
Chip Select to Output Disable	T_{SHOZ} 2/			10	n s
Output Enable to Output Disable	T_{GHQZ} 2/			10	n s

2/ These parameters may be sample tested. The sample size is 5 parts or 10%, whichever is greater

Table 3

WRITE CYCLE AC ELECTRICAL PERFORMANCE *

TEST	SYMBOL	CONDITIONS $T_C = -55^\circ\text{C}, 25^\circ\text{C}, +125^\circ\text{C}$ $V_{DD} = 4.5\text{V}, 5.0\text{V}, \& 5.5\text{V}$	LIMITS		UNITS
			MIN	MAX	
Chip Selection to End of Write	T_{SLWH}		35		n s
Address Setup to End of Write	T_{AVWH}		35		n s
Address Setup to Start of Write	T_{AVWL}		0		n s
Write Pulse Width	T_{WLWH}		35		n s
Data Hold after end of Write	T_{WHDX}		0		n s
Chip Setup to End of Write	T_{DVWH}		30		n s

* **NOTE:** Run Write Cycle AC Electrical Performance Tests while applying checkerboard, march, X-Y march, and CEDES-CE algorithms. See figure 5 of 5962-92153 for timing waveforms.

Table 4

Parameter Delta Limits

TEST	SYMBOL	CONDITIONS $T_C = 25^\circ\text{C}, V_{DD} = 5.0\text{V}$	Δ LIMITS	UNITS
			MAX	
Dynamic Operating Current	I_{DD}	$f_{RC} = 1\text{ MHz}$, all inputs switching;	4	%
Standby Supply Current	I_{SB}	All Inputs at 0.2 V below V_{DD}	4% or 50 μA , whichever is greater	% or μA
Output high Voltage	V_{OH}		.1	Volts
Output Low Voltage	V_{OL}		.1	Volts

- 4.2.3 Particle Impact Noise Detection (PIND) All Microcircuits (100%) shall be subjected to and pass PIND examination per MIL-STD-883, method 2020, condition B.
- 4.3 Quality Conformance Inspection (QCI) Quality conformance inspection shall be in accordance with paragraph 4.7 of MIL-H-38534, level H, option 1.
- 4.4 Destructive Physical Analysis (DPA) DPA is not required on this part provided that the CA Module is fabricated by the same manufacturer, using the same processes as the FB Module, and DPA results on the FB Module are acceptable.
- 4.5 Inspection and Test Records The supplier shall maintain inspection and test records for 36 months after hardware delivery to MIT. Test data for all electrical tests, screening, DPA, and QCI inspections shall be submitted to MIT with the delivery of flight parts.

4.6 Source Inspection

4.6.1 Government Source Inspection (GSI) The government has the right to inspect any or all of the work included in this order at the supplier's plant. In the event that Government Source Inspection (GSI) is imposed, the Government quality representative who has been delegated NASA quality assurance functions for this procurement shall be notified immediately upon receipt of this order. The Government representative shall also be notified 48 hours in advance of the time that parts are ready for inspection or test.

4.6.2 MIT Source Inspection MIT Performance Assurance will impose mandatory inspection points (MIPs) at wire bonding (precap visual examination) and final test, and must be notified 2 weeks before parts are ready for MIT Inspection. (call area code 617, phone 253-7555).

5.0 **PACKAGING**

5.1 Packaging requirements Packaging shall be in accordance with paragraph 5.1 of MIL-H-38534.

6.0 **NOTES**

6.1 Approved Source of Supply

Teledyne Electronic Technologies
12964 Panama Street
Los Angeles, CA 90066

Cage Code 16170

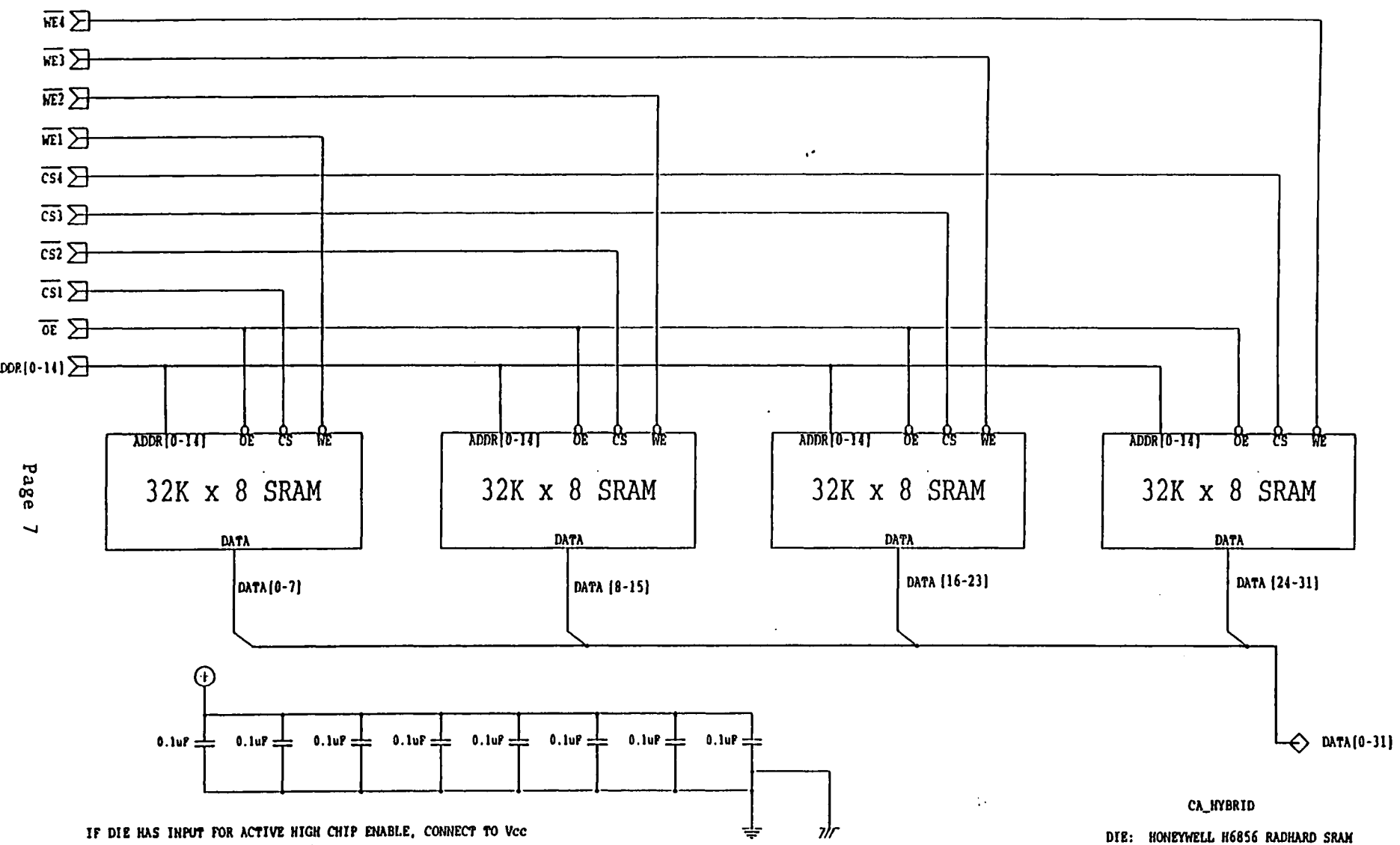


FIGURE 1
CIRCUIT SCHEMATIC

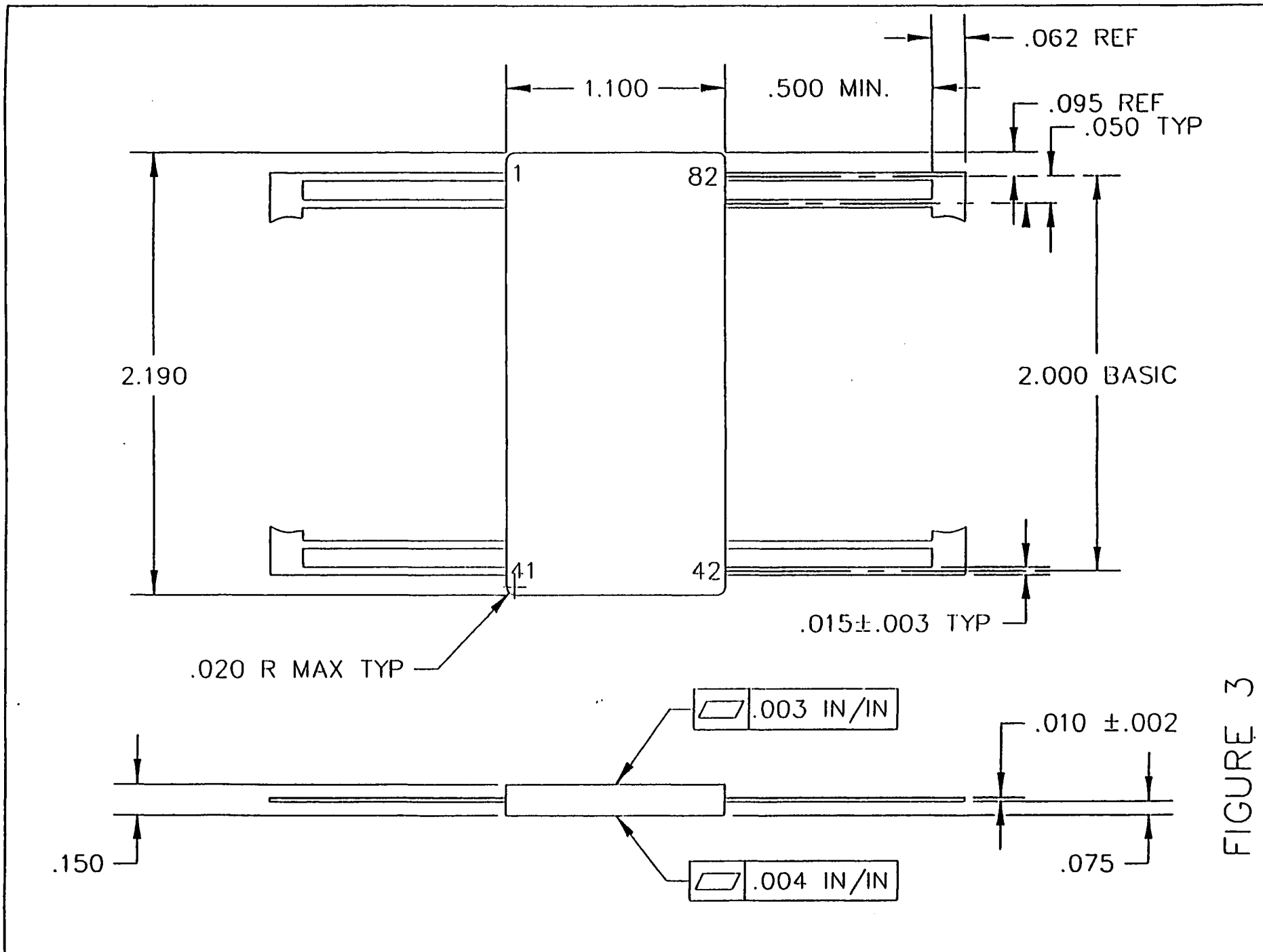
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IF DIE HAS INPUT FOR ACTIVE HIGH CHIP ENABLE, CONNECT TO Vcc
BRING OUT ACTIVE LOW CHIP SELECT
CASE GND CONNECTED TO LOGIC GND

CA_HYBRID
DIE: HONEYWELL H6856 RADHARD SRAM

**FIGURE 2
TERMINAL CONNECTIONS**

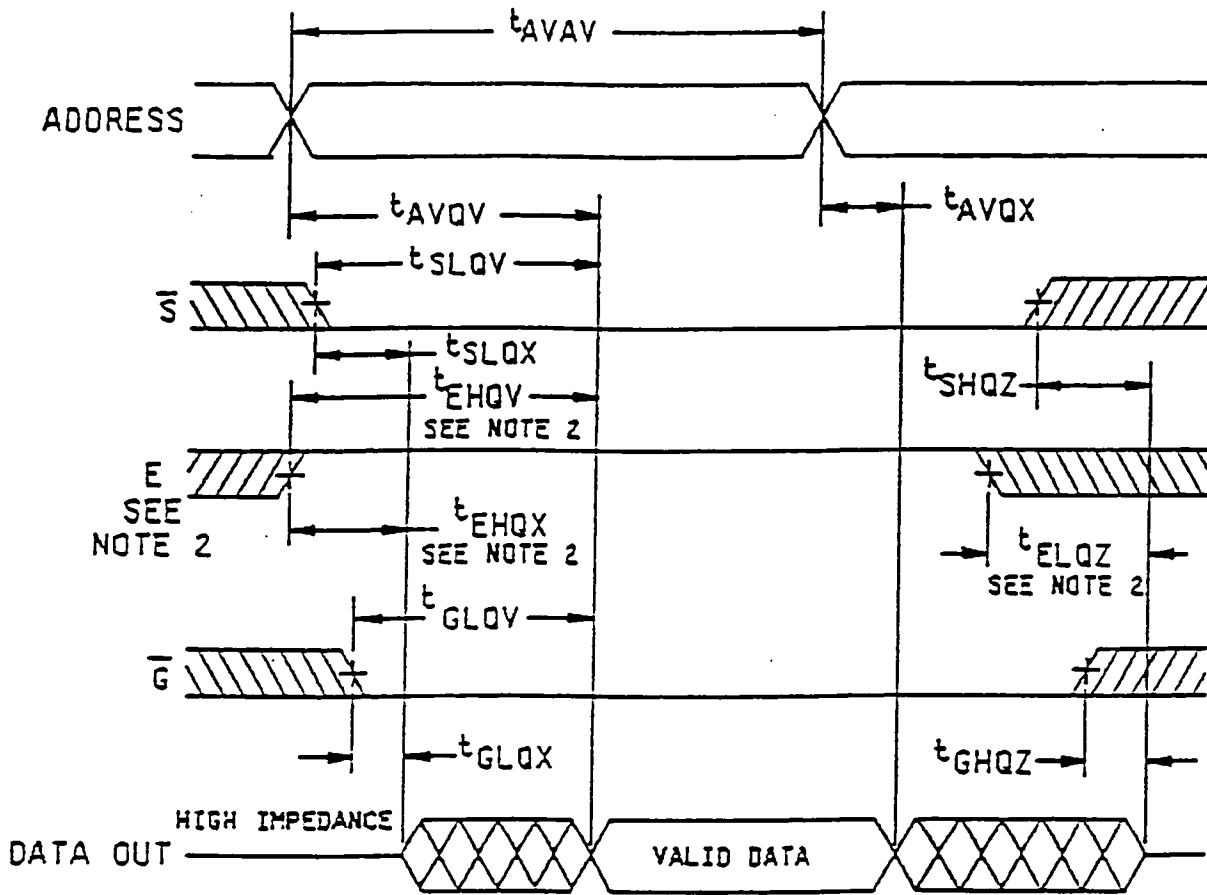
PIN No.	SIGNAL NAME	PIN No.	SIGNAL NAME
1	CASE GND	42	GND
2	+5V	43	+5V
3	NC	44	NC
4	D00	45	NC
5	D01	46	WE4N
6	D02	47	CS4N
7	D03	48	NC
8	D04	49	NC
9	D05	50	CS3N
10	D06	51	WE3N
11	D07	52	NC
12	D08	53	OEN
13	D09	54	A14
14	D10	55	A13
15	D11	56	A12
16	D12	57	A11
17	D13	58	A10
18	D14	59	A09
19	D15	60	A08
20	GND	61	GND
21	+5V	62	+5V
22	NC	63	A07
23	D16	64	A06
24	D17	65	A05
25	D18	66	A04
26	D19	67	A03
27	D20	68	A02
28	D21	69	A01
29	D22	70	A00
30	D23	71	NC
31	D24	72	WE2N
32	D25	73	CS2N
33	D26	74	NC
34	D27	75	WE1N
35	D28	76	CS1N
36	D29	77	NC
37	D30	78	NC
38	D31	79	NC
39	NC	80	NC
40	+5V	81	+5V
41	GND	82	GND



REV.	
DWG. NO.	36-02302
FSCM NO.	A 80230
SCALE	NONE
SHEET	9

FIGURE 3
PACKAGE OUTLINE

Read cycle (see note 1)



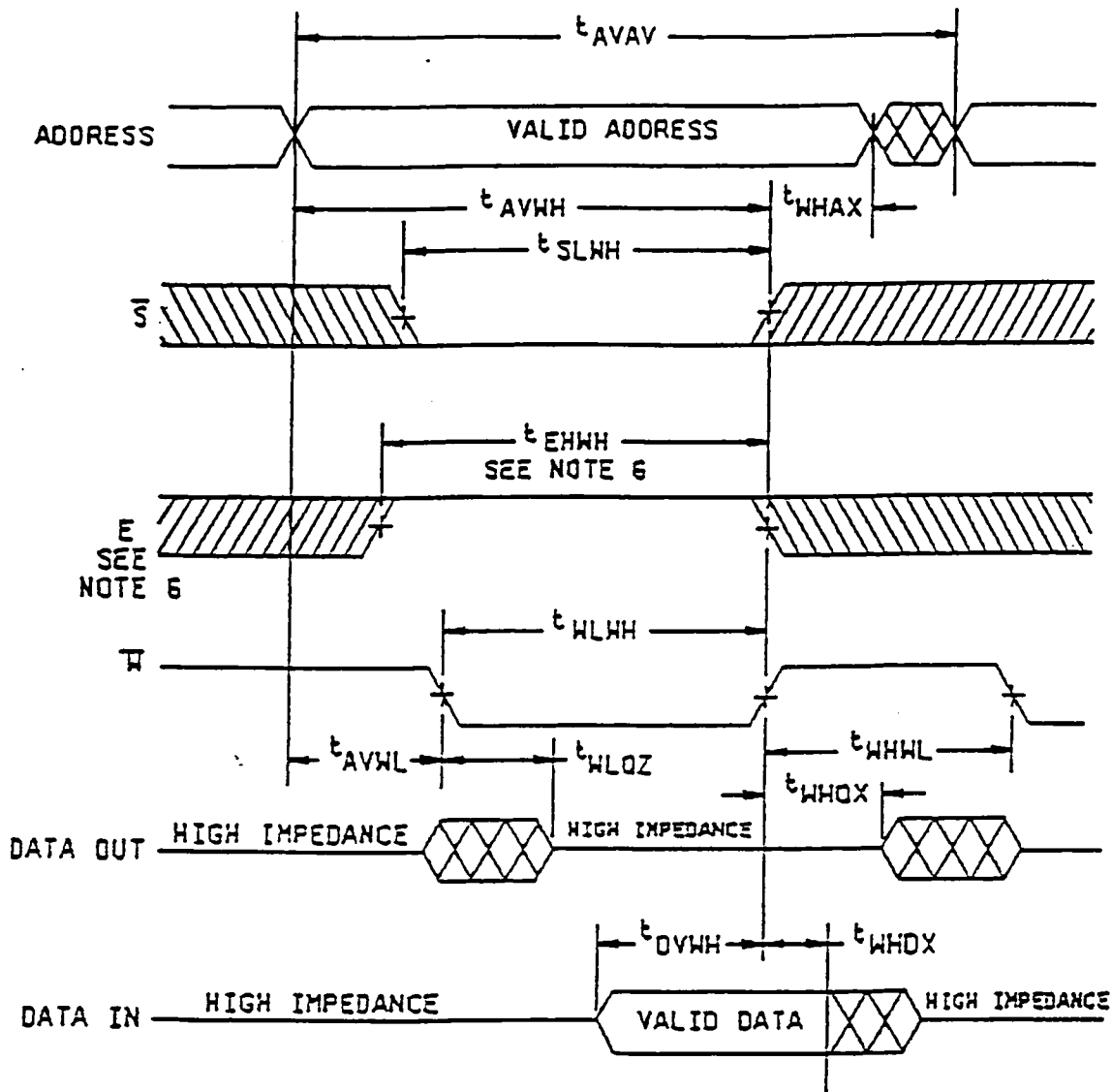
NOTE:

1. \bar{W} is high for read cycle.
2. E and timing parameters t_{EHQV} , t_{EHQX} , t_{ELQZ} do not apply to device types 09 and 10.

FIGURE 5. Timing waveforms.

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Write cycle (see notes 1, 2, 3, 4, and 5)



NOTES:

1. Write cycle data is latched by the first occurrence of \bar{S} high, \bar{E} low or \bar{W} high.
2. \bar{S} high, \bar{E} low, or \bar{W} high must occur while address transitions.
3. Write cycle time is guaranteed for toggling \bar{S} and \bar{E} or holding \bar{S} or \bar{E} , or both, in active state.
4. The worst case timing sequence of $t_{WLQZ} + t_{DVWH} + t_{WHHL} =$ the write cycle time (t_{AVAV}).
5. \bar{G} high will eliminate the I/O output from becoming active (t_{WLQZ}).
6. \bar{E} and timing parameter t_{EHWH} do not apply to device types 09 and 10.

FIGURE 5. Timing waveforms - continued.

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