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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CENTER FOR SPACE RESEARCH

BEP/FEP Interface Control Document

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BEP/FEP Interface Control Document

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Rev. A

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1.0 Introduction

This document is used within MIT to define the electrical interfaces which exist between the Backend Processor and the Frontend Processor, both computing systems resident in the DPA (Digital Processor Assembly) of the ACIS experiment.

The DPA is composed of nine printed circuit boards: six frontend processors (FEPs) overseen by a backend processor (BEP). Prime and redundant BEPs, powered by separate supplies, are housed in the DPA. In addition, the DPA contains a PREP board which houses two "virtual boards", each containing a bank of nonvolatile memory (the flight ROM) and differential receivers (the DEA to DPA video signal receivers).

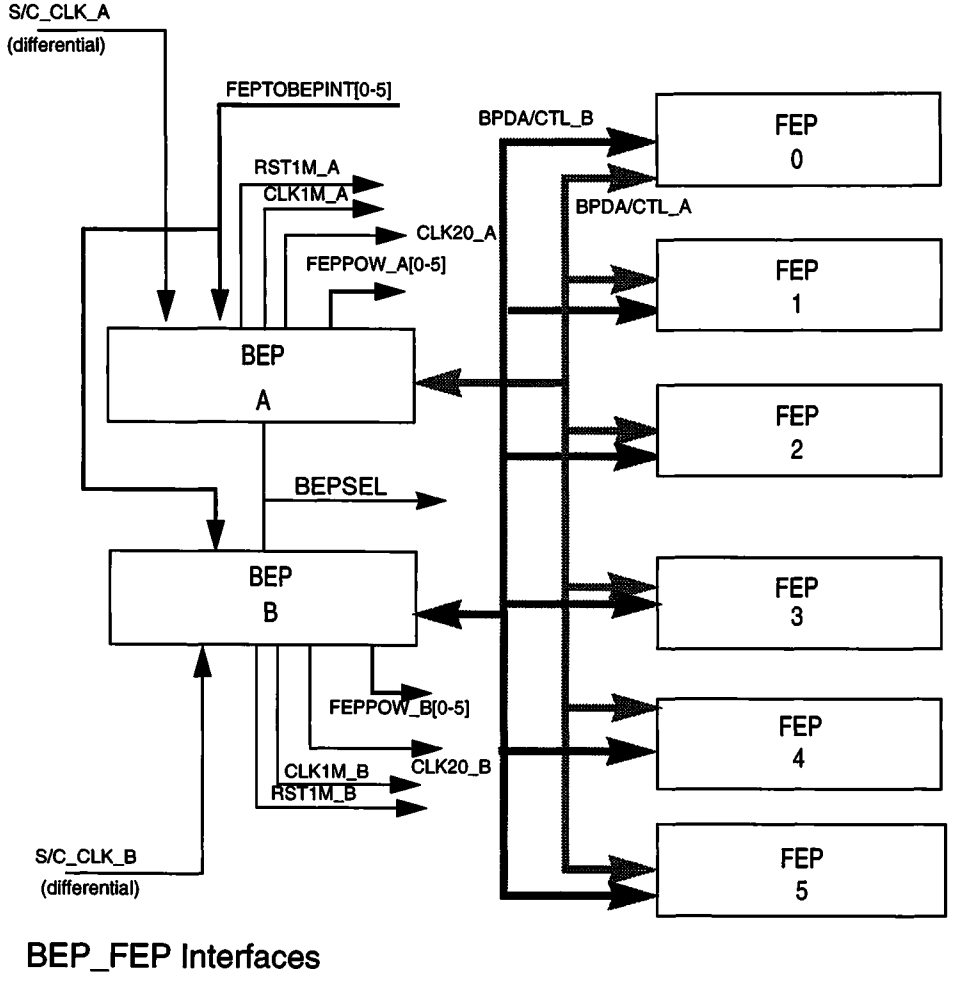


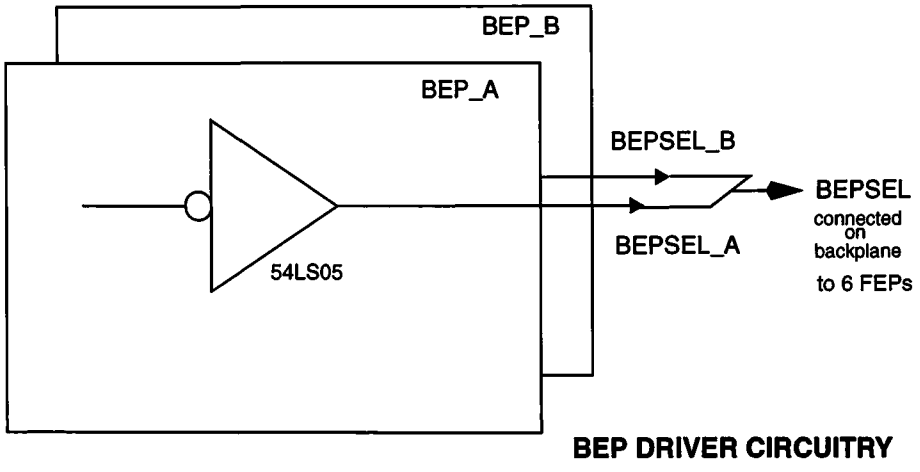
FIGURE 1. BEP/FEP Interfaces

As shown in Figure 1, the BEP/FEP Interface is comprised of the following sections: CPU/shared memory (MCLK, BPDA/CTL, FEPTOBEPINT), a master/slave counter (CLK1M, RST1M), and a power control interface (FEPPOW). A global signal (BEPSEL), driven by (wire-ORed) both BEPs, determines which BEP is the designated interface driver.

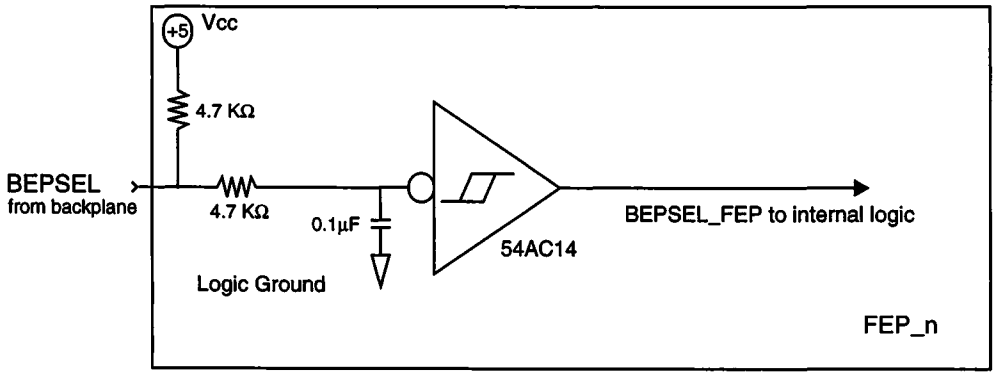
2.0 Active BEP Selection (BEPSEL)

BEPSEL, a signal driven by both BEPs, determines which BEP actively drives the interfaces. BEPSEL gates (gated internally by the BEP) telemetry data sent to the RCTU, DEA command/status and clocks (gated by the DEA), and the following BEP to FEP interfaces (gated on the FEP boards): the Master/Slave counter interface, the master clock, and the BEP-FEP shared memory interface.

The following circuit is used for transmission of BEPSEL within the DPA:



BEP DRIVER CIRCUITRY



FEP RECEIVER CIRCUITRY
(replicated on each FEP)

NOTE: BEPSEL is set via the Hardware Command Port on each BEP. See the DPA Hardware Specification & System Description (drawing number 36-02104) for further details.

The polarity of BEPSEL is defined as follows: "asserted high" on the boards and "asserted low" on the backplane. Therefore, an on-board (FEP or BEP) signal level of +5 V. indicates that BEP_B is selected; 0 V. selects BEP_A. Conversely, a backplane BEPSEL of 0 V. would indicate that BEP_B is selected; while backplane BEPSEL = 5 V. would select BEP_A.

3.0 Master Slave Counter Interface

Both the BEP and FEP contain counters which are clocked by the Spacecraft (S/C) supplied clock (1.024 MHz). The counter on the BEP spans 32 bits; the FEP counter contains 26 bits. (See the DPA System Description and Specification, document 36-02104, for further information about the use of these counters.) Both counters wrap once their terminal count is passed. In order to synchronize the BEP and FEP counts, every ~32 seconds the BEP sends a reset pulse to the FEP counters. (This corresponds to the assertion of the 25th bit of the BEP.) Signal definitions for this interface are shown below:

Signal Name	Description
CLK1M	1.024 MHz Spacecraft Clock - received differentially by the BEPs which drive single ended version to the FEPs
RST1M	~1 us active low reset pulse, period of ~32 seconds

TABLE 1. Master/Slave Counter Interface Signals

Each signal has an A and a B version, corresponding to BEP_A and BEP_B. See the discussion on BEPSEL (Section 2.0 on page 4) for further details regarding selection between A and B on the FEPs.

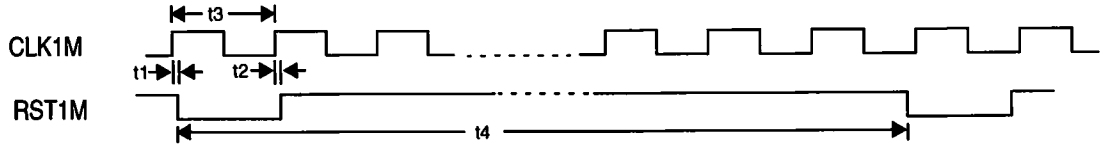
3.1 Master Slave Counter Driver Receiver Circuitry

A single-ended version of CLK1M is driven by each BEP onto the backplane (CLK1M_A and CLK1M_B). RST1M is derived by a clock divider resident on the BEP and driven out via the backplane connector to the FEPs (RST1M_A and RST1M_B).

Both CLK1M and RST1M are driven and received by TTL "LS" family parts. DC characteristics and risetimes shall conform to the Standard TTL Data books.

3.2 Master Slave Counter Signal Protocol/Timing

The signal relationships are shown below:



Timing characterization:

Parameter		Minimum	Typical	Maximum	Units
CLKup-RSTdown	t1	10	-	50	ns
CLKup-RSTup	t2	10	-	50	ns
CLK1M-period & RST1M pulse width	t3	927	977	1025	ns
RST1M-period	t4	t3 X 2^{25}	t3 X 2^{25}	t3 X 2^{25}	ns

Signals are referenced to the output of the BEP LS buffers.

NOTE: Minimum and maximum clock periods, based on S/C clock of 5% accuracy, are stated just as a reference. The FEP and BEP hardware will be able to handle arbitrary S/C clock frequencies up to 2 MHz.

4.0 BEP_FEP Shared Memory/CPU Interface

The BEP_FEP CPU interface consists of three functional units: the master clock distributed by the BEP, the multiplexed address/data bus via which the BEP can read/write FEP registers and memory, and the FEP to BEP interrupt lines.

4.1 Distributed CPU Clock

The system clock (CLK20) is a 19.2 MHz clock which is generated by the BEP clock divider circuitry from a BEP resident fundamental 38.4 MHz clock. Each FEP routes CLK20 through a delay circuit to its CPU 2X clock input pin. The delay circuit, included in order to minimize the instantaneous AC demand on the power supply, generates a time delay dependent on FEP_ID (set by the backplane slot).

CLK20 is driven/received with 54LS244 buffers. Selection between CLK20_A and CLK20_B is performed on each FEP, with BEPSEL used to enable the appropriate receiver.

4.2 Shared Memory Interface

The shared memory interface consists of a 32-bit multiplexed address/data and control bus, and asynchronous handshaking signals.

The following control signals define the BEP/FEP shared memory interface:

Signal Field	Field Width	Description
Data/Address (BPDA)	32	During the initial section of the transaction this field is a combination of address and a Read/Write bit (unidirectional, driven by BEP); during the later portion, it is a bi-directional data bus.
BEPtoFEPStrobe (BEPSTR)	1	Strobes Address Control portion of the Data/Addr-Cntl field onto the FEPs (Active Low). Driven by BEP when instigating access to an FEP. The FEP is selected by Address bits A24-A26 (BPDA positions 22-24)
FEPtoBEPGnt (FEPSTR)	1	An open collector output, driven by all active FEPs onto the backplane. The selected FEP drives FEPtoBEPGnt low to signal that a requested transaction has been accepted. It drives it high to signal that the transfer in progress is complete (signaling to the BEP to generate an internal "READY" to the CPU.) There are separate (identical) A and B versions of FEPGNT driven by each FEP.

TABLE 2. BEP/FEP Shared Memory Interface - Signal Fields

The Address-Cntl field includes:

Signal Field	Field Width	Description
F-Idx	25	MA(2)-MA(26), (MA(24) - MA(26) select the FEP being accessed.) These signals appear on the data bus positions 0-24.
R/W	1	Direction of transfer - 1=Read FEP, 0=Write FEP - appears on data bus position 25.

TABLE 3. BEP/FEP Data/Addr Field Breakdown

NOTE: all polarities are referenced to the DPA backplane, the interface between the BEP and FEP.

For details regarding the memory mapping and register functionality, see the DPA Hardware Specification & System Description (drawing number 36-02104).

4.2.1 Addresss/Data Bus Protocol

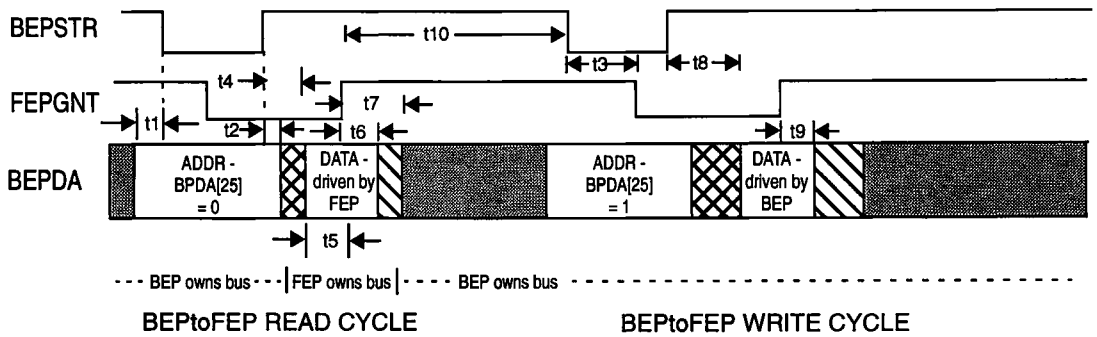
BEPSTR (controlled by the backend processor) initiates a transfer. The selected FEP responds by latching address-cntl and asserting FEPGNT. The BEP then deasserts BEPSTR and supplies data (for a write) or turns off its drivers (for a read). Upon completion of a cycle, the FEP deasserts FEPGNT, supplying data for a read and strobing in the data for a write. The deassertion of FEPGNT causes the generation of a "READY" signal by the

BEP to its CPU control circuitry. All six FEPs generate unique (A and B) FEPGNT lines which are connected on the DPA backplane. The wire-ORed versions of FEPGNT are pulled-up and bufferred on their respective BEPs.

(NOTE: FEPID is determined by the FEP backplane slot and ranges from 0-5. FEPID 7 is reserved for "single-board" mode.)

4.2.2 Addresss/Data Bus Timing

The following describes the BEP/FEP parallel interface:



Timing characterization:

Parameter		Minimum	Typical	Maximum	Units
Addr-Cntl valid to BEPSTRdown (t_{su})	t1	50	-	-	ns
Addr-Cntl valid from BEPSTRup (t_{hold})	t2	0	-	-	ns
BEPSTRdown to FEPGNTdown (t_{del})	t3	300	400	5500[1]	ns
Turnoff time (BEP) from BEPSTRup (t_{off}) (BEPtoFEP READ CYCLE)	t4	-	-	50	ns
Data valid to FEPGNTup (t_{su}) (BEPtoFEP READ CYCLE)	t5	50	-	-	ns
Data valid from FEPGNTup (t_{hold}) (BEPtoFEP READ CYCLE)	t6	40	-	-	ns
Turnoff time (FEP) from FEPGNTup (t_{off}) (BEPtoFEP READ CYCLE)	t7	50	-	100	ns
Data valid from BEPGNTup (t_{del}) (BEPtoFEP WRITE CYCLE)	t8	-	-	100	ns
Data valid from FEPGNTup (t_{hold}) (BEPtoFEP WRITE CYCLE)	t9	0	-	-	ns
FEPGNTup (cycle *n*) to BEPSTRdown (cycle *n*+1) (Cycle to cycle recovery time)	t10	200	-	-	ns

NOTE 1: 5.5 µs represents the maximum bus arbitration delay if the BEP and FEP are accessing image memory while image acquisition in progress.

Signal timing and polarity are referenced to the DPA backplane.

Note that the signal transfer between the BEP and FEP must be considered asynchronous, as the internal board clocks may in fact be significantly skewed with respect to each other.

All drivers/receivers are standard TTL LS family buffers. FEPGNT lines are driven by the FEP with 54LS05 open collector drivers. All other signals are received or driven with either 54LS244 or 54LS245s.

4.3 FEP to BEP Interrupt

Six independent interrupts (pulsed) from the FEPs to the BEP (latched and reset internal to the BEP). (An OR of these lines creates an interrupt to the BEP CPU). Each FEP drives a unique interrupt line to both BEPs (no A and B versions provided) via 54LS05 open collector drivers. The BEP must pull-up and resynchronize the interrupt lines before forwarding them to its CPU.

The minimum interrupt pulse width shall be 25 ns; maximum pulse width shall be 75 ns.

Interrupt lines are asserted high local to the FEP and BEP CPUs and asserted low on the backplane.

5.0 BEP to FEP Power Control Interface

Each FEP contains solid state switch circuitry which either BEP can energize via a transistor implemented wire-OR.

The implementation is shown in Figure 2:

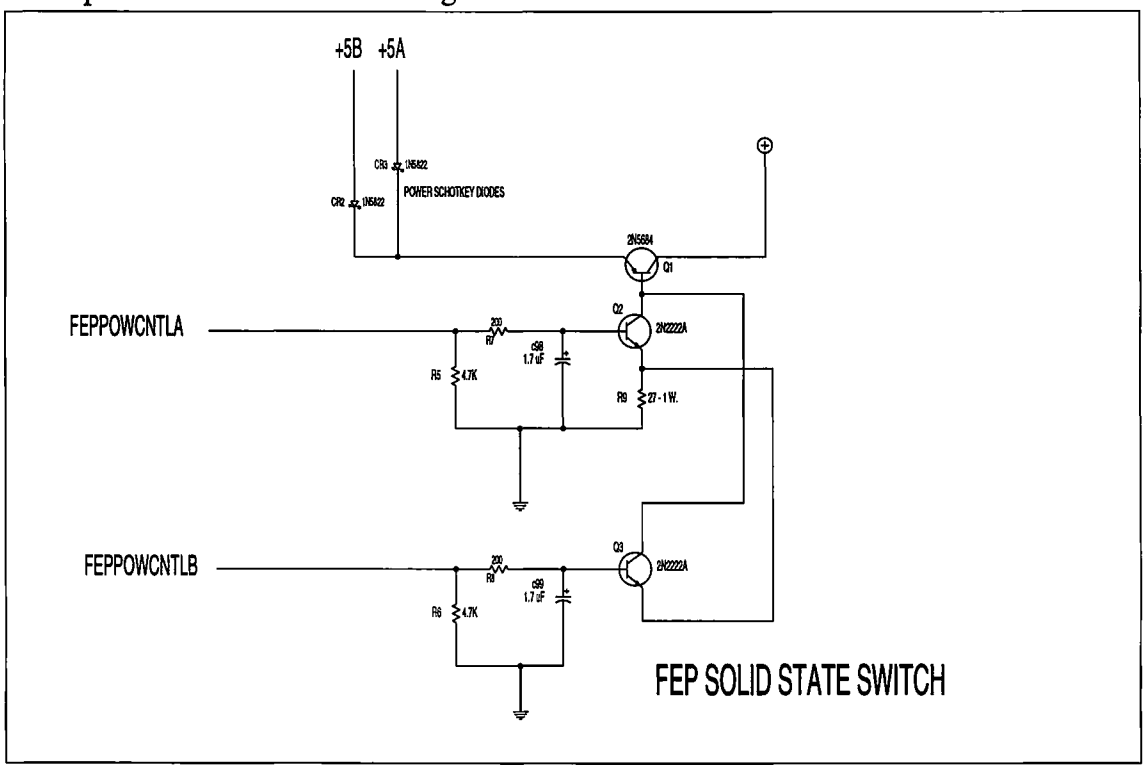


FIGURE 2. Solid State Switch and Control

Each BEP drives six unique FEP power control signals onto the backplane (asserted high), driven by LS family gates resident on the BEP. These bits are controlled via the BEP control register (see DPA Hardware Specification & System Description, document # 36-02104) for further details.