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A	36-161	Initial Release			
B	36-735	Update to Conform to Existing Hardware			8/23/96
C	36-814	Added Information in Tables			11/14 1996

NAME		DATE
Drawn:	D. Gordon	3/10/95
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MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CENTER FOR SPACE RESEARCH

DPA/DEA Interface Control Document

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DPA/DEA Interface Control Document

Drawing Number 36-02205

Rev. C

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1.0 Introduction

This document is used within MIT to define the electrical interfaces which exist between the Detector Electronics Assembly (DEA) and the Digital Processor Assembly (DPA).

The DEA is composed of ten identical Video Cards and two, redundant (though not identical) Interface/Focal Plane Temperature Control subsystems. Each Video Card is autonomous from the others; but all, including the Interface boards, share a common backplane. The backplane carries power, command signals, *etc.* from the Interface Cards to the Video Cards. Pixel data outputs from each Video Card are sent *via* the back-plane directly to the DPA. A single analog housekeep line on the backplane carries multiplexed analog signals from a selected Video Card to the Interface Card. Similarly, a single multiplexed path exists on the backplane for (diagnostic) high speed data from the Video Cards to be sent to the DEA test connector.

To avoid possible confusion, one must keep in mind the following nomenclature. Various ACIS subsystems have redundant "A" and "B" sections. For instance the Power Supply for both the DEA and DPA, the PSMC (supplied by Martin Marietta), has two identical "A" and "B" sections. The "-A" and "-B" Labels on sections or signals in one subsystem like this do not suggest references to "-A" and "-B" labels in other subsystems.

The DEA Interface consists out of two (somewhat identical) sections A (board 11) and B (board 12). The system cabling is made such that section A is turned on when the PSMC DEA power supply A is turned on, and B when power B is turned on. If both A and B section of the power are accidentally commanded on at the same time, the Interface will react and shut off it's B side regulators. The DEA Video Cards receive their power *via* the Interface Cards. The Interface Cards, by use of latching relays, selects power from either the PSMC side A or side B supply.

The DPA is composed of eight printed circuit boards: six front-end processors (FEPs) overseen by two, fully redundant, back end processors (BEP).

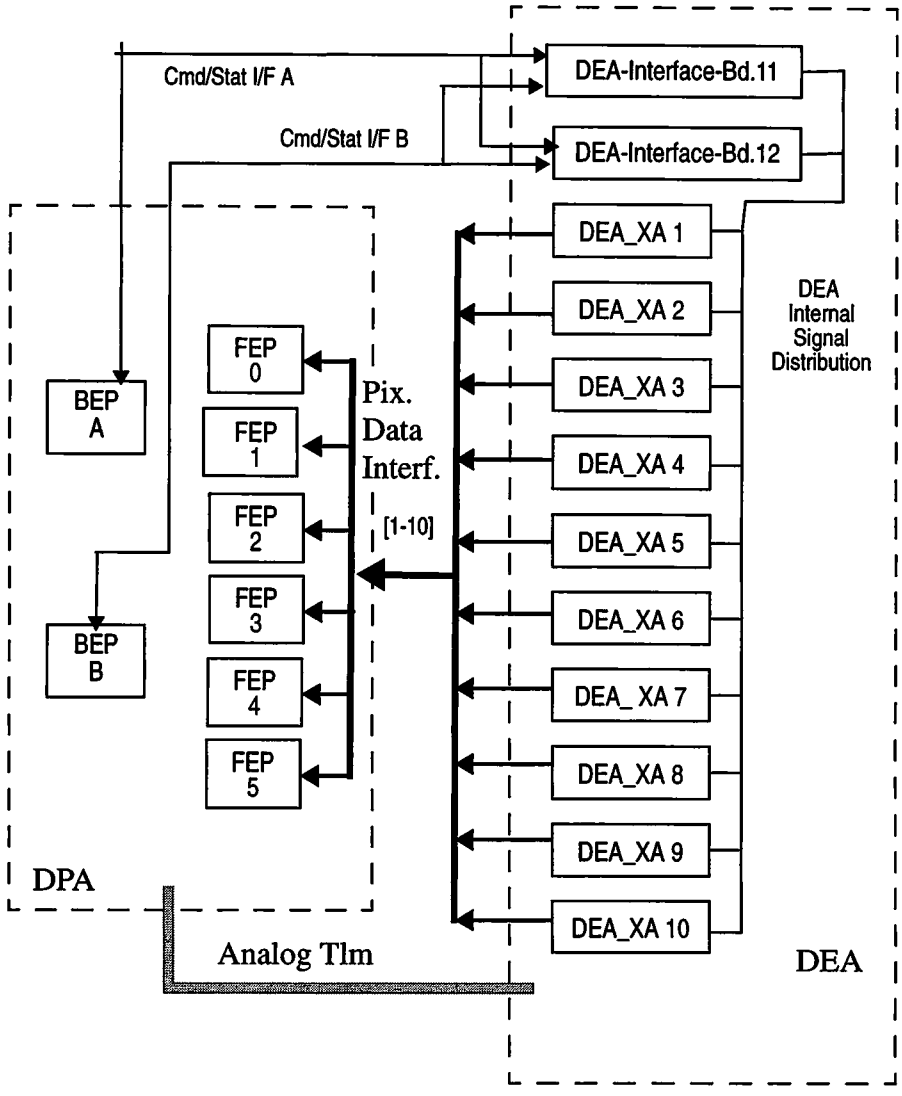


FIGURE 1. DEA/DPA Interfaces

As shown in Figure 1, the DEA/DPA Interface is comprised of two functional sections: Command Status (Cmd/Stat) and Pixel Data (PixDat). The (redundant) command channel from each BEP goes to the two Interface Cards for redistribution (*via* the backplane) to all of the Video Cards. All cards in the DEA share this single party-line command and status interface. Pixel data, on the other hand, is routed separately from each of the 10 Video Cards to the DPA backplane; each FEP can independently select one of the 10 pixel data streams to process.

.

2.0 Command/Status Interface

CCD control and housekeeping is performed on the DPA by the BEP. Two redundant sets of wires run between the DEA (received on isolated sections of the DEA-Interface Boards.) and DPA (connecting to the two BEPs). The signal BEPSEL, sent by the DPA to the DEA, identifies which BEP is active. Figure 2 shows the driver/receiver configuration of the command interface; Figure 3 shows the status interface.

The Command/Status expected wire length is on the order of 5 feet.

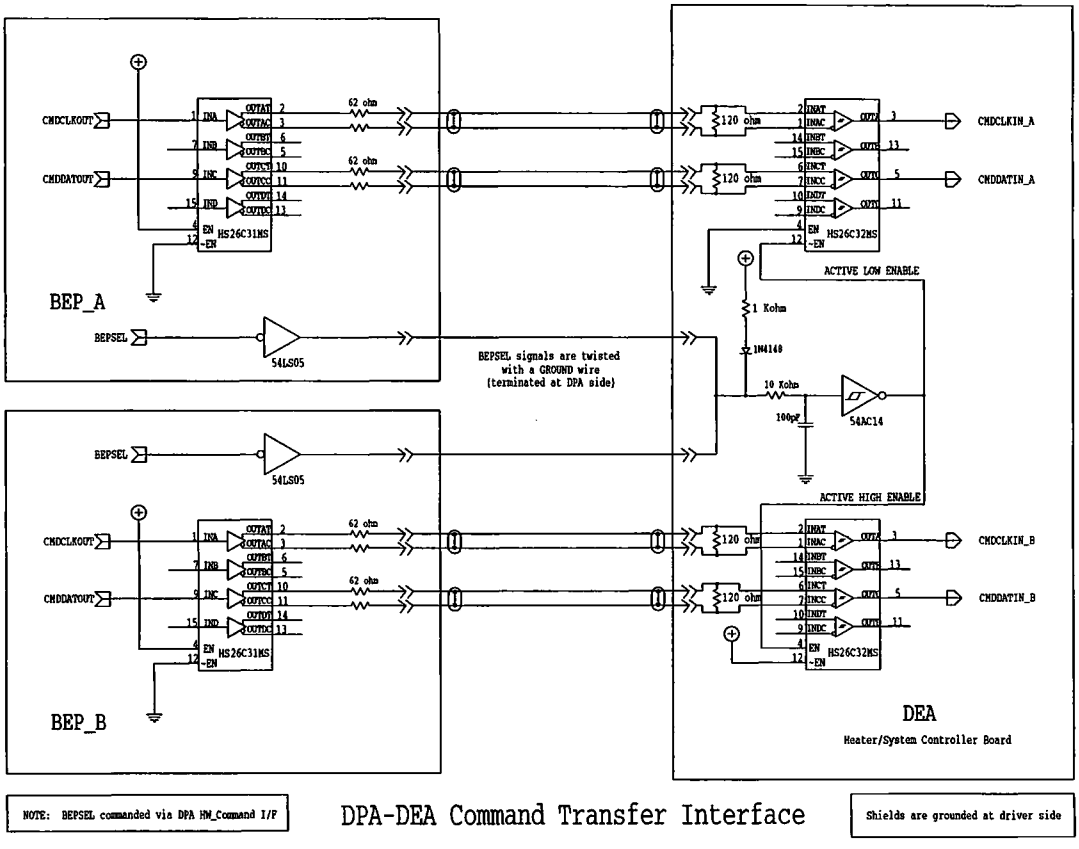
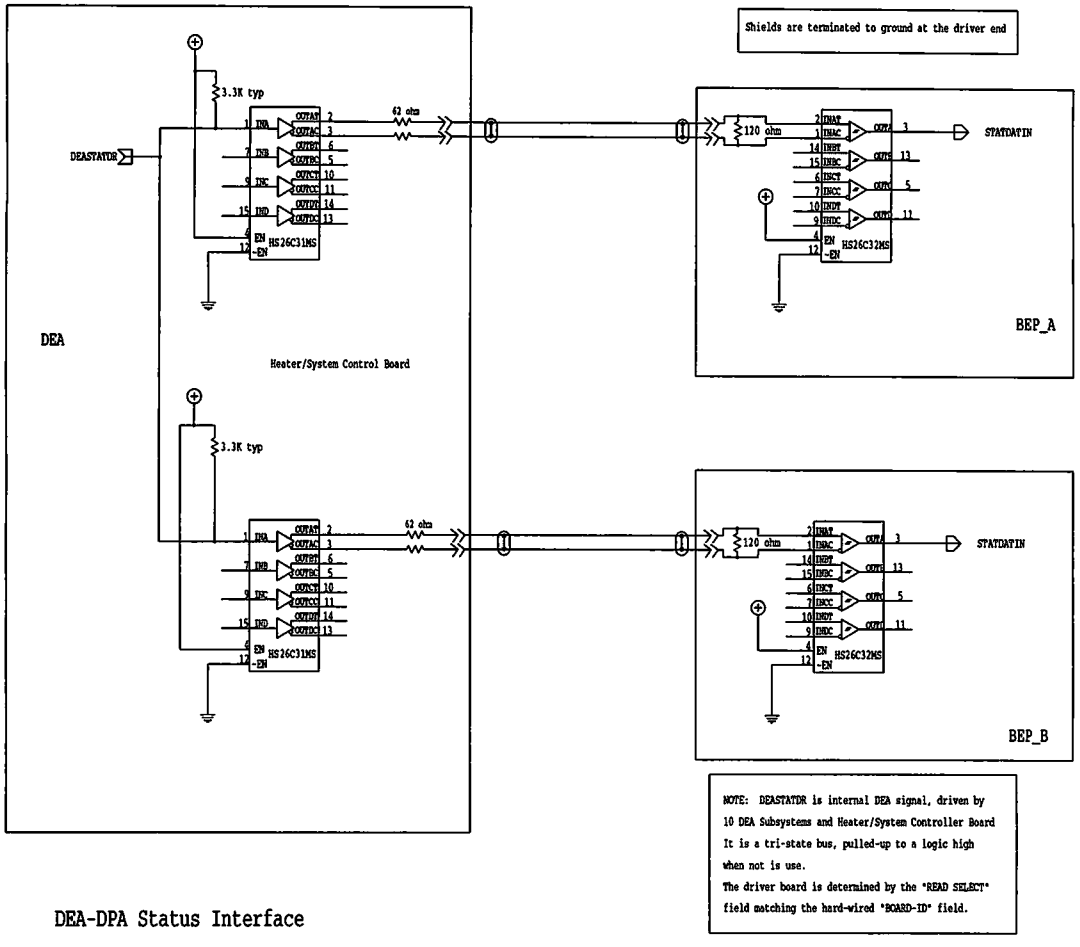


FIGURE 2. Command Interface



DEA-DPA Status Interface

FIGURE 3. Status Interface

Global command signals connecting the DPA to the DEA are shown below:

Signal Name (At DPA)	Driven by	Description	Transmission
DEACLK.	DPA	1.6MHz Command Clock. The duty cycle is 50% +/- 10%	A and B, Each Differential.
DEADAT.	DPA	Command Data, synch to CSCLK, 24 bits/word, leading startbit (0), trailing stopbit (1), data active low, MSB first	A and B, Each Differential.
DEASTAT.	DEA	Status Data, synch to CSCLK, 24 bits/word, leading startbit (0), trailing stopbit (1), data active low, MSB first	A and B, Each Differential.
DEARST.	DPA	Master Reset (reset level, common to all Video Card boards)	A and B, Each Differential.

TABLE 1. Command/Status Interface Signals

Signal Name (At DPA)	Driven by	Description	Transmission
DEABEPSEL	DPA	BEP Select A and B. Used to select differential receivers on DEA to receive A or B set of Command signals	A and B, Wire-OR single ended
DEACK100K	DPA	100 KHz clock, synchronous with ADC Start of Conversion (SOC) pulse, but shifted in phase.	A and B, Each Differential.
DEACLK6M	DPA	A 6 MHz. clock, used for SRAM Major Cycle timing, Video Output timing and A/D Converter Clock	A and B, Each Differential.

TABLE 1. Command/Status Interface Signals

2.1 Serial Command/Status Signal Protocol/Timing

Both command (DEADAT) and status (DEASTAT) transfer are serviced by a 1.6 MHz. clock (DEACLK).
During idle, the outputs of the differential receivers as well as the inputs of the differential transmitters, used for DEADAT and DEASTAT transfer, will be at a high level.
A low level here is defined as a "true".
The start of a transfer is marked by a start bit, e.g. a true condition with the duration of one cycle of the DEACLK. Transfer of the 24 bit wide word (DEASDAT or DEASTAT) follows the start bit at the speed of one bit per clock cycle. The M.S.B. is transferred first. (B23 in figure 4.)

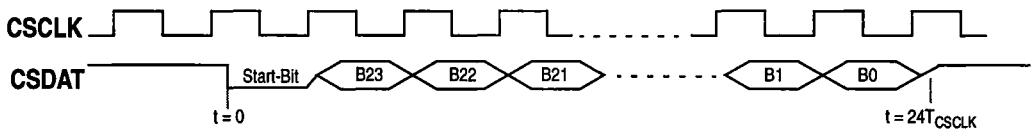


FIGURE 4. Command Signal Protocol

Also shown in Figure 4, the 24 bit word is clocked out of the DPA on the rising edge of the 1.6 MHz (DEACLK) clock. The DEA clocks the data in on the falling edge of DEACLK. (It is assumed that clock to data propagation delay on the DPA < 100 ns.) The onset of any command data transmission on the DPA shall be synchronized to the 100 KHz ADC (DEACK100K) clock. This is to insure that a "Sequencer Start" command receipt at the DEA can be deterministically timestamped by the DPA.

The status data interface is identical to the command data interface, but with the DEA driving the DEASTAT line. (The combined clock propagation delay and the clock to data propagation delay on the DEA shall be < 150 ns.) The status data line is driven only by the selected Video Card or by the DEA interface., and only in response to a DPA readback or housekeeping request command.The maximum reply time for returned status words from the DEA shall be < 100 μsec.

2.2 DEA Video Board Command Formats.

There are basically two sets of command formats: The DEA Video Boards Command Data set, and the DEA Interface Command Data set.
There is also a small subgroup, a sort of hybrid, of the two basic ones.

The DEA Video Command Data appears to the DPA CPU as a writable (24-bit) register. The basic format is as follows:

24 Bit Command Word				
23	22	21	20	19.....Argument.....0
CS	R/W	A/D	0	Argument (Address or Data. see table 2)

Where: Bit **20** always is 0 for DEA Video Board Commands.

Bit **21** is the Address/Data bit. If this is "1", The argument is an Address. If "0", it is data. The number of meaningful bits in the data field depends on the register that is being addressed.

Bit **22**, the Read/Write bit is always a "1" for read accesses and a "0" for writes.

CS-write and CS-Read:

Bit **23**: A "1" in this bit specifies a card select (CS) function. e.g. CS-Write when bit 22 is "0", and CS-Read, when bit 22 is "1".
Bits 16-19 and bit 21 are "don't cares" for the CS function. They have no effect on writes; readback will give indeterminate values.
At any time, one of the Video Cards can be selected to respond to any and all following housekeep read request commands.
This is done by CS-Write command using the argument field shown just below.

Argument Field															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Select				X	X	Write Mask									

By placing the card ID of this Video Card in the read select bits 12-15.
The ID (1 through 10) of a Video Card is determined by it's place on the back-plane.

Each of the single bits in the Write Mask of the same command is assigned to one Video Card. Bit 0 to bit 9 correspond to ID 1 through ID 10. The write mask determines which DEA board or boards will execute any write command that may follow.
At power-up, the subsystem write mask will default to all zeros and none of the boards will be written to until a CS-write command is issued with a "1" in the mask bits for the selected boards.

NOTE: CS-write is the only command directed to all DEA Video boards.

The Cs-Read function (Bit 23 = 1, Bit 22= 1)returns the following data format.:

Argument Field															
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Read Select				SI	Selected Card ID			X							

Bit 11 (SI - Select Indicator) will be returned "1" by the card which has been selected by last CS-write command. It also repeats the Read Select code on bits 7-10.
This command is basically for diagnostic use.

There are 4 more basic commands. These are identified by bit 23 = 0.

A summary of all six command codes and the basic tasks are shown below:

CS	R/W	A/D		DEA Video board Command Descriptions.
23	22	21	20	
0	0	0	0	Write data to device/memory location indexed by address register
0	0	1	0	Write address to address register
0	1	0	0	Read data from device/memory location indexed by address register
0	1	1	0	Read address from address register
1	0	X	0	CS-Write: Select one board for housekeep, select all boards
1	1	X	0	CS-Read: Diagnostic. Card, selected by CS-Write responds.

Using Memory Mapping allows identification of specific tasks by knowledge of the Register Address. See table above, and table 2 below.

TABLE 2. Video Card Memory Map.

Device/Memory Section	Reg. Add. (hex)	Definition/Notes
SRAM Sequencer RAM	0 - 7FFF	Sequencer RAM -random R/W, Do not try to access when the sequencer is active. Data is 16 Bits wide.
PRAM Program RAM	8000 - FFFF	Same as above.
Video Card Registers	10000 - 1003F	Details in Table 3. 8 Bit argument for data.
Video Card DACs	10040 - 1005F	8 Bit argument for data. A read command from a DAC is meaningless. DEA will return latest received data word instead.
Video Card Housekeep	10080 - 100FF	The Housekeep function uses a set of hybrid commands as mentioned at start of this paragraph. Do not use a write, as this will cause all write-enabled boards to select an analog channel, causing analog bus contention.

2.3 DEA Video Board Control/DAC/Housekeep Registers.

Video Cards register descriptions are shown below.

Register Name --- **Reset State (hex)**	**Reg. Add. (hex)**	**Bit #**	**Data Bit Definition**
Sequencer Control Register --- 00	10000	0	Sequencer Start. When a command is issued to change bit 0 to "1", the offset delay counter is started. The sequencer than starts after time-out of this counter. A value "0"does not change existing state of sequencer.
		1	Sequencer Stop. A "1" in bit 1 causes the sequencer to halt. (Shutdown occurs after completion of the current SRAM major cycle.) A value "0" does not change existing state of sequencer.
		2-7	Offset delay count.: The Sequencer Offset Delay Count is a number, 0 to 63, which specifies the delay after the 0 to 1 level transition of the 100 KHz. Sync. signal.before the sequencer is allowed to start.
		Note: Loading this register with the correct code is the actual start command for a data acquisition program. Contents of register should not be changed during the data acquisition.	
Video A/D Converter Register --- 00	10001	0	A/D-Cycle Start. Writing "1"in bit 0, together with the desired A/D offset code in bits 2-7, will start the calibration and synchronization program of the 4 A/D converters. (bit 1=X).
		1	A/D-Cycle Stop. Writing "1"in bit 1, with"0" in bit 0, Stops the A/D Conversion cycle.
		2-7	A/D-cycle offset delay count. This number,0 to 63, determines the count in the A/D Conversion cycle where the 0 to 1 transition of the 100 KHz. Sync signal will occur. This number should not be changed during data acquisition.!
		Notes: 1) Code 00 in bits 01 does not change existing state of A/D cycling. 2) Calibration and synchronization procedure lasts about 10 mSec. for a video clock frequency of 6.4MHz. 3) Contents of register should not be changed during the data acquisition.	

TABLE 3. Video Card Control Register Definitions

Register Name --- Reset State (hex)	Reg. Add. (hex)	Bit #	Data Bit Definition
Test aid Register. --- 00	10002	0	When set to 1, Video output A is set to 0.
		1	When set to 1, Video output B is set to 0.
		2	When set to 1, Video output C is set to 0.
		3	When set to 1, Video output D is set to 0.
		6	Set this bit to "1". This allows for sufficient settling time on the housekeep common connection.
		7	High z.:No longer used!
		note: Bit 6 may be set to "1" on one board at a time only! (to prevent erroneous housekeep readings. See Card Select-Read function on page 9.	
Miscellaneous Reg --- 00	10003	0	Low Power: No longer used!
		1	BJD: When bit is set to 1, Back junction diode voltage =80 Volt.
		2	Clock-swap.: Set to 1: sets CCD Serial transfer clock lines for bi-directional operation (4 separate video outputs); Set to 0: sets CCD Serial transfer clock lines for unidirectional transfer.(2 separate video outputs.)
		3	GSENOT: When bit 3 = 1, the GSE output is driven by selected board.
		4	STENNOT: When bit 4 = 1, Status output bus is driven by selected board.
		7	HKCAL: No longer used! (No a/d converters on Video Boards)
		notes No more than one Video Card at a time should be allowed to drive GSE or STATUS outputs. E.g.: Bit 3 and/or bit 4 set to "1" on one card only.	

TABLE 3. Video Card Control Register Definitions

Video Card DAC Channels are shown below.

All DAC outputs are 0 to 2.5 Volt, 8 Bits Resolution.

Selected Channel Address (Octal) + 200100	DAC Output Voltage Name	Description of it's USE	CV is programmed output voltage of DAC in Selected channel, unless full name is used. (CV = 0 to 2.5 Volt., 50mV Res.)
00	DAC PIA+	Parallel Image Array Shift clock High Level ($VPIA^+$).	$VPIA^+$ = 5.11 **CV** = 0 to 12. 775 Volt. (Resolution.:50mV)
01	DAC PIA-+	Parallel Image Array Shift Clock, Low Level ($VPIA^-$), can be set a combination of two DAC channels.	$VPIA^-$ = 5.11 (DAC PIA^{-+} - DAC PIA^-) = -12.775 to + 12.775 Volt. (Res.:50mV)
02	DAC PIA-		
03	DAC PFS^+	Parallel Frame Store Shift clock High Level	$VPFS^+$= 5.11 = -12.775 to + 12.775 Volt.
04	DAC PFS^{-+}	Parallel Frame Store Shift Clock, Low Level ($VPIA^-$), can be set by a combination of these DAC channels.	$VPFS^-$ = 5.11(DAC PFS^{-+} - DAC PFS^-) = -12.775 to + 12.775 Volt.
05	DAC PFS^-		
06	DAC S^+	Serial Shift clocks High Level.	VS^+ = 5.11 **CV**
07	DAC S^-	Serial Shift clocks Low Level.	VS^- = - 5.11**CV**
10	DAC R^+	Reset Gate Pulse. High Level	VR^+ = 5.11 **CV**
11	DAC R^{-+}	Reset Gate Pulse. Low Level (VR^-) , can be set by a combination of these DAC channels.	VR^- = 5.11(DAC R^{-+}-DAC R^-) = -12.775 to + 12.775 Volt.
12	DAC R^-		
13	DAC SCP	Scupper Bias Voltage.	SCP = 5.11 **CV**
14	DAC OG^+	Output Gate, Positive Levels	OG = 5.11 (DAC OG^++ DAC OG^-)
15	DAC OG^-	Output Gate, Negative Levels	
16	DAC RD	Set Reset Diode Bias Voltage (RD) and set **DREF,** used in circuit to generate $\mathbf{CV_{16}}$ for next 4 Channels.	RD = 5.11 **CV** DREF = -1.24 CV $\mathbf{CV_{16}}$ = **CV**
17	DAC DR0	Drain Bias Voltage, Output node A.	DR-A = 5.11 ($\mathbf{CV_{16}}$ +CV)
20	DAC DR1	Drain Bias Voltage, Output node B.	DR-B = 5.11 ($\mathbf{CV_{16}}$ + CV)
21	DAC DR2	Drain Bias Voltage, Output node C.	DR-C = 5.11 ($\mathbf{CV_{16}}$ +CV)
22	DAC DR3	Drain Bias Voltage, Output node D.	DR-D = 5.11 ($\mathbf{CV_{16}}$ +CV)
23	AOFF	Set D.C. Offset at input of Video A/D Converter A.	V_{offset} = +2.5 - 2 **CV** = - 2.5 to + 2.5 Volt. (0.02 V/Bit)
24	BOFF	Set D.C. Offset at input of Video A/D Converter B.	
25	COFF	Set D.C. Offset at input of Video A/D Converter C.	
26	DOFF	Set D.C. Offset at input of Video A/D Converter D.	
27	(SPARE)		

TABLE 4. Video Card Channel Assignment For setting of Voltage Levels

ADC Channel (octal) +200200	SIGNAL Name	Description	ADC RANGE (Volt)	mV /Bit
00	V PIA$^+$	Parallel Image Array Shift clock High Level.	-12.8 to 12.8	6.25
01	V PIA$^-$	Parallel Image Array Shift clock Low Level.	SAME	SAME
02	V PFS$^+$	Parallel Frame Store Shift clock High Level	SAME	SAME
03	VPFS$^-$	Parallel Frame Store Shift clock Low Level	SAME	SAME
04	V S$^+$	Serial Shift clocks High Level.	SAME	SAME
05	V S$^-$	Serial Shift clocks Low Level.	SAME	SAME
06	V R$^+$	Reset Gate High Level.	SAME	SAME
07	V R$^-$	Reset Gate Low Level.	-12.8 to 12.8	6.25
10	OG	Output Gate Bias Level	-12.8 to 12.8	6.25
11	SCP	Scupper Bias Voltage.	-12.8 to 12.8	6.25
12	RD	Reset Diode Bias Level.	-12.8 to 12.8	6.25
13	DR-A	Drain Bias Voltage, Output node A.	-38.4 to +38.4	18.75
14	DR-B	Drain Bias Voltage, Output node B.	-38.4 to +38.4	18.75
15	DR-C	Drain Bias Voltage, Output node C.	-38.4 to +38.4	18.75
16	DR-D	Drain Bias Voltage, Output node D.	-38.4 to +38.4	18.75
17	(SPARE)			
20	RT4	DEA Video board Thermistor 4:. board temperature.	SEE THERMISTOR CALIBRATION	
21	RT3	DEA Video board Thermistor 3: Memory (U37)temperature.		
22	RT2	DEA Video board Thermistor 2: A to D Converter		
23	RT1	DEA Video board Thermistor 1: ACTEL.		
24	(SPARE)			
25	(SPARE)			
26	(SPARE)			

TABLE 5.

2.4 DEA Interface Command Formats/Tasks.

While the DEA Video boards in general require two Command Words to execute a task, the DEA Interface uses a single,24 Bit word.
The Interface receives all Commands from the DPA and distributes these unmodified to the Video boards. The Video boards only act on commands when the codes in Bits 20 through 23 are recognized. See paragraph 2.2.

The interface acts on Command words with binary 0011 in Bits 23 -20.
An exception to this is the doublet Video board Command: "Write address 10080 through 10097 (hex)", followed by "read data". According to table 2, this would read a housekeep channel number 00 to 17 (hex) on the selected Video board.
Both the Interface and the Video board act on this Command.
The video Board places a representing analog level on the Housekeep bus in the back-plane. The interface than does an A/D Conversion on this voltage and sends the result of this as a status to the DPA.

Assignment of bits in the Interface Command word are:

Bits 23,22,21 and 20: When 0011, Command is directed to the DEA Interface.

Bit 19: A one for bit 19 specifies a read command, a zero is used for every non read.

Bit 16: Is used in some of the non-read tasks. It functions as a switch. "one" means turn on, and "zero" means turn off. What has to be turned on or off is specified by Bits 12 through 15 (the task number) and further detailed by the Task-Target-Selection bit field. For instance: When task 5 is executed with bit 0 at 0, the L.E.D. will not be switched, but with bit 0 at 1, it turns on when bit 16 is 1, and off when bit 16 is 0.

Bits 12 through 15: Contain task numbers. See Listing in Table 6.

Bits 0 through 11: Data field or bit map. See Listing in Table 7.

TABLE 6. Command structure for the DEA Interface

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1	1		X	X																	
THIS CODE SELECTS INTERFACE				READ			SWITCH	TASK NUMBER				DATA FIELD, OR REGISTER SELECT OR TASK-TARGET-SELECTION BIT FIELD											

TABLE 7. Listing of DEA Interface Command Tasks.

Task Name	Task #	Bit 19	Bit16 Used?	Description and bit assignment
Housekeep	10	1	No	Housekeep Channel. 00-27Hex.See table 8.
Focal Plane T.	11	1	No	No longer used! Focal plane temp. can be read by House-keep query. See Table 8.
Relays Posi-tion	12	1	No	Read position of 5 sets of relays. Each bit 0-4 is assigned to one set. See Note 1.

TABLE 7. Listing of DEA Interface Command Tasks.

Task Name	Task #	Bit 19	Bit16 Used?	Description and bit assignment
Set Focal Plane Temp. Fine	0	0	No	Both Course and Fine Setting have to be placed in the 8 Bit D/A converters.set.8 Bits resolution.Find initial values from graphs, If it is required to know the temperature more accurately, calibrate codes using housekeep channels 16 and/or 17.
Set Focal Plane Temp. Course	1	0	No	
Switch Power to Video Boards	4	0	Yes	Each Bit 0 - 9 is associated with one Board 1 - 10. Bit 0: Board 1, etc.
Switch miscellaneous 1.	5	0	Yes	Bit 0: L.E.D. Bit 2: Bake-out. Bit 9: Hold HK-address.
Calibrate and Reset.	6	0	No	Bit 0: Start Calibration cycle, internal in A/D. Bit 4: Software Reset of Video Boards. Task(s) executed every time the command is received.
Change Signal path See Note 3.	7	0	No	Bit 0: If "1", Reverse Direction of Command Signals Bit 4: If "1", No Comm. Word output to Video boards. Bit 5: I f"1", No Comm. Clock output to Video boards. Bit 6: If "1", No Sync. (100Kc.) output to Video boards. Bit 7: If "1", No Video Clock ou.put to Video boards.
Switch Relays See Note 1.	8	0	No	Bits 4 - 0: If 00001 (bin.): Switch Relay set # 1. If 00010 (bin.): Switch Relay set # 2. If 00100 (bin.): Switch Relay set # 3. If 01000 (bin.): Switch Relay set # 4. If 10000 (bin.): Switch Relay set # 5. Relay assignments: See note 1.

Note 1: There are 10 DEA Video Boards.(10 CCDs.). The boards are divided into 5 sets of 2 boards. The "A" or the "B" power supply can be used as the raw power source for any of these sets.
5 Sets of 3 Latching Relays are used to select "A" or "B"Power Supply.

When DEA Interface board 11 is in command, executing Task 8 can only switch selected relay sets to connect power supply "A"!
Task 12,executed when board 11 is in command, returns a "1" for those relay sets which are switched to power supply "A".

In a similar fashion:
When DEA Interface board 12 is in command, executing Task 8 can only switch selected relay sets to connect power supply "A"!

Task 12,executed when board 11 is in command, returns a "1" for those relay sets which are switched to power supply "A".

TABLE 8. DEA Board Assignments.

Relay Set Number	1	2	3	4	5
DEA Board Number	XA1	XA3	XA5	XA7	XA9
CCD Number	I0	I1	I2	I3	S4
DEA Board Number	XA2	XA4	XA6	XA8	XA10
CCD Number	S0	S1	S3	S2	S5

2.5 DEA Interface Housekeep Registers.

ADC Channel (Octal)	SIGNAL Name (on int. bd.)	Description	D/A RANGE (Volt)	mV /Bin
00	DPATHERM1	DPA-BEP-PC board therm.	SEE THERMISTOR CALIBRATION EQUATION. (PARAGRAPH 2.6)	
01	DPATHERM2	DPA-BEP-OSC therm.		
02	DPATHERM3	DPA-FEP0-Mongoose case therm.		
03	DPATHERM4	DPA-FEP0-PC board therm.		
04	DPATHERM5	DPA-FEP0-Actel therm.		
05	DPATHERM6	DPA-FEP0-SRAM therm.		
06	DPATHERM7	DPA-FEP0-FB therm.		
07	DPATHERM8	DPA-FEP1-Mongoose case therm.		
10	DPATHERM9	DPA-FEP1-PCB therm.		
11	DPATHERM10	DPA-FEP1-Actel therm.		
12	DPATHERM11	DPA-FEP1-SRAM therm.		
13	DPATHERM12	DPA-FEP1-FB therm.		
14	SUBAHK	DC Voltage level from selected DEA Video Board and channel.	SEE TABLE 5.	
15	SPARE	Not used- --Spare.		
16	SPARE	Focal Plane Temp.(RTC); Board 12	RTD Resistance (Rt) is: :Rt = 0.084N - 1.292 (Ohm) (N = A/D Conv. Output Code)	
17	SPARE	Focal Plane Temp.(RTD); Board 11		
20	DPAGNDREF1	DPA Ground reference.	- 2.5 to + 2.5	1.22
21	DPA5VHKA	+5 Volt Supply (A) on DPA.	-20.83 to +20.83	10.17 (Scale 2)
22	DPAGNDREF2	DPA Ground reference.	- 2.5 to + 2.5	1.22
23	DPA5VHKB	+5 Volt Supply (B) on DPA.	-20.83 to +20.83	10.17 (Scale 2)

TABLE 9. DEA Interface Housekeep Channels Assignments

ADC Channel (Octal)	SIGNAL Name (on int. bd.)	Description	D/A RANGE (Volt)	mV /Bin
24	TEMP-DH-A	Primary Detector Housing Temp. (RTD).	Spare Channels - Not used	
25	TEMP-FP-B	Secondary Focal Plane Temp. (RTD).		
26	TEMP-FP-A	Primary Focal Plane Temp. (RTD).		
27	TEMP-DH-B	Secondary Detector Housing Temp. (RTD)		
30	DEA+28VDCA	Primary raw +28Volt DEA Supply.	-41.9 to + 41.9	20.44
31	DEA+24VDCA	Primary raw +24Volt DEA Supply.	-41.9 to + 41.9	20.44
32	DEA -15.5VDCA	Primary raw -15.5Volt DEA Supply.	-20.83 to +20.83	10.17
33	DEA +15.5VDCA	Primary raw +15.5Volt DEA Supply.	-20.83 to +20.83	10.17
34	DEA-6VDCA	Primary raw -6Volt DEA Supply.	-20.83 to +20.83	10.17
35	DEA+6VDCA	Primary raw +6Volt DEA Supply.	-20.83 to +20.83	10.17
36	RAD-PCB-A	Relative Dose Radiation Monitor	- 2.5 to +2.5 mAmp	0.61 uAmp.
37	GND	Ground reference of Interface.	- 2.5 to + 2.5	1.22
40	DEA+28VDCB	Back-up, raw, +28Volt DEA Supply.	-41.9 to + 41.9	20.44
41	DEA+24VDCB	Back-up, raw, +24Volt DEA Supply.	-41.9 to + 41.9	20.44
42	DEA -15.5VDCB	Back-up, raw, -15.5Volt DEA Supply.	-20.83 to +20.83	10.17
43	DEA +15.5VDCB	Back-up, raw, +15.5Volt DEA Supply.	-20.83 to +20.83	10.17
44	DEA-6VDCB	Back-up, raw, -6Volt DEA Supply.	-20.83 to +20.83	10.17
45	DEA+6VDCB	Back-up, raw, -6Volt DEA Supply.	-20.83 to +20.83	10.17
46	RAD-PCB-B	Radiation Dose Monitor -- Reference.	- 2.5 to +2.5 mAmp	0.61 uAmp.
47	GND		- 2.5 to + 2.5	1.22

TABLE 9. DEA Interface Housekeep Channels Assignments

2.6 Thermistor Calibration Equation

A, 2.252 K (@ 25 ^{o} C) YSI, thermistor in series or in parallel with a 5.23 K fixed resistor will have a minimum of 1 LSB / ^{o} C resolution over the -40 to +60 ^{o} C temperature range. In our case, the series configuration is used. A bias voltage is connected to the 5.23 K and the thermistor is grounded on one side.
When the same source is used for both this bias voltage and the reference for the A/D Converter, the A/D Output code, N, will be independent on it.The measured temperature T in ^{o} C than is:

$$T = (1.074 \times 10^{-7} Q^3 + 2.372 \times 10^{-4} Q + 1.4733 \times 10^{-3})^{-1} - 273.16$$

$$Q = \ln (5.23 \times 10^3 \times N / (2^{12} - N)).$$

Where ($5.23 \times 10^3 \times N / (2^{12} - N)$) is the Thermistor Impedance.

3.0 CCD Data Interface

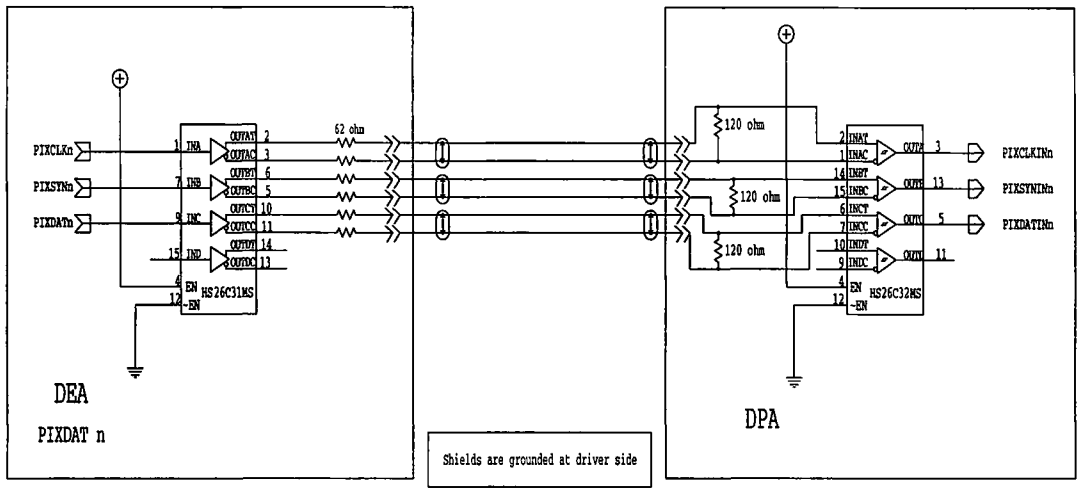
The CCD data interface operates in a similar fashion to a video interface. Data is shifted out serial, pixel-by-pixel. Each bit is synched to a dedicated clock line; and each pixel word (16-bits) is synched to a dedicated pixel synch line. Three lines are differentially driven independently by each Video Card:

Signal Name	Description
PIXCLK	6.4 MHz Pixel Clock
PIXDAT	Pixel Data, synch to PIXCLK, 16 bits/pixel, MSB first
PIXSYNCH	**Pixel Synch - 0.156 µsec pulse every pixel, proceeding the MSB by** one bit (one synch pulse every 2.5 µsec). NOTE: it is coincident with the LSB of the previous word for continuous data transfer (see Figure 6,"Video Signal Protocol," on page 17.

TABLE 10. Video (Pixel Data) Interface Signals

Each pixel output by the DEA contains two fields: a 4-bit pixel code field followed by a

The Video Drivers/Receivers are shown in Figure 5. Expected wire length is on the order of 5 feet.



DEA-DPA Pixel Data Interface (one DEA Subsystem)

FIGURE 5. Pixel Data Interface.

3.1 Video (Pixel) Signal Protocol/Timing

Due to the relatively high frequency of video data transmission, each DEA subsystems supplies the corresponding 6.4 MHz shift clock along with its data stream.

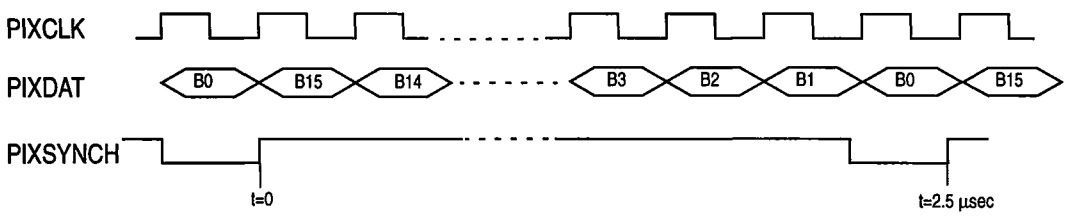


FIGURE 6. Video Signal Protocol

As shown in Figure 6, the pixel data is clocked out of the DEA on the rising edge of the 6.4 MHz (PIXCLK) clock. The DPA clocks the data in on the falling edge of CSCLK. (It is assumed that clock to data propagation delay on the DEA < 40 ns.) Skew between the video signals shall be limited to < 10 ns. (In order to accomplish this, the drivers and receivers for the three should be tapped from the same package.)DEA subsystem house-keeping channel assignments are shown below

3.2 Pixel Data Format

The pixel word has the following format:

15...Pixel Code....12	11.....Pixel Data.....0

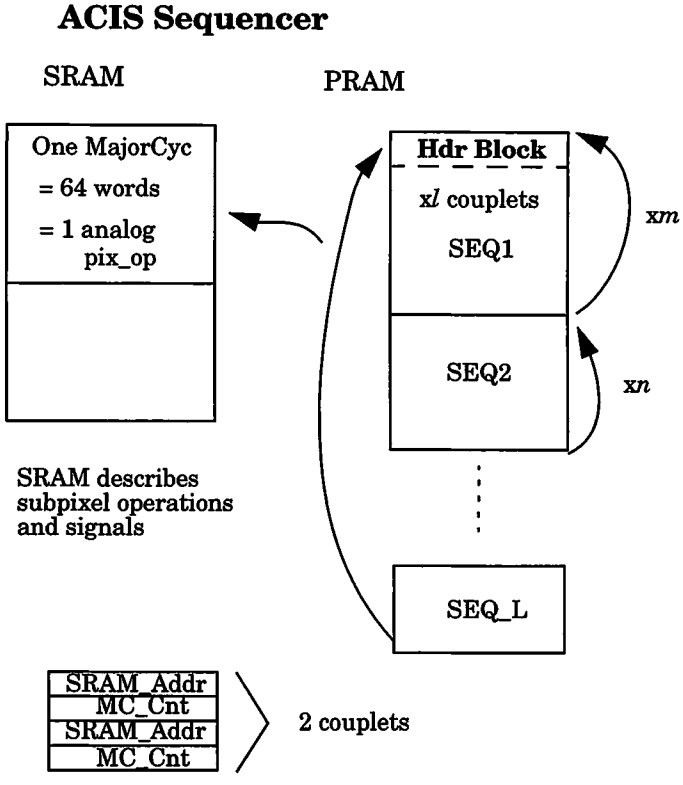
Pixel Data is a digitized 12-bit unsigned value representing the pixel energy. Pixel Code is a 4-bit DEA sequencer to DPA FEP "handshaking" signal. The pixel codes are programmed into the PRAM, and sent out synchronously with the associated pixel data (see the Appendix A: DEA Sequencer User's Guide, attached to this document).

The Pixel Code meanings are shown below.

Pixel Code (binary)	Description
0000	NO-OP - no operation, has no effect.
0011	VALID PIXEL
0100	Horizontal Synch - Beginning of row.
1000	Vertical Synch - Beginning of frame.
1100	Overclock Value.
1111	Sequence Error.

TABLE 11. Pixel Codes

Appendix A: Sequencer Users Guide



The PRAM Header Block is shown below:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fld Def	1	1	OP 1	OP 0	PRAM Sequence Count[0-11]											
Fld Def	1	0	PA 1	PA 0	Couplet Count[0-11]											

The OP bit field defines the sequencer jump options as follows:

OP1	OP0	Next Sequence Option
0	0	Restart
0	1	Continue
1	0	Halt
1	1	Page Jump to PRAM Page described by PA1:PA0 = PRAMADDR14:13

The couplets following the PRAM header block are defined as:

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Fld Def	0	1	SRAM PageAddr[6-14]									U	PixCode[0-3]			
Fld Def	0	0	U	U	Major Cycle Count[0-11]											

The SRAM Page Address points to a section of SRAM which represents the clock sequence desired for generating the current pixel timing.

The Major Cycle count indicates how many times to "playback" the sequence. (U is a spare bit, undefined.)

All counts (Sequence Count, Couplet Count and Major Cycle count) include zero, so programming a one will result in two iterations.

The Pixel Code (PixCode) is a four bit field which is shifted out in the digitized pixel stream to the DPA. It allows the DEA sequencer hardware to synchronously link to the DPA front-tend HW. Pixel information such as beginning of frame, beginning of row, advance address generator, overclock region, etc. can be included. The detailed definition of these codes will be included in the DPA HW Specification following the FEP detailed design.

When the sequencer is not active, its output bus is held in a predetermined state (TBD) by the hardware. During inactive periods, PixCode is held at 0.

If the sequencer determines a synch error has occurred, (bits 15 and 14 are not as expected), it will assert a signal called SeqError and halt the sequencer. SeqError will cause a unique PixCode to be generated (all ones - hex F). Seq Error is reset by the restarting of the Sequencer via the command status interface. (TBD: should we also provide for SeqError to be reset via an explicit command?)

A 6- bit offset-delay register, programmable via the Command/Status Interface is provided in order to properly align the actual readout of SRAM with the ADC 100 KHz SOC clock. Between 0 and 63 offset delay clocks can be programmed to take place between the time the sequencer hardware receives the STARTSEQ pulse and when it actually begins to cycle SRAM.

NOTE: SRAM address is held to zero when the sequencer is halted. Therefore, Major_Cycle "zero" should be reserved for the default values of the analog sequencer bus signals.

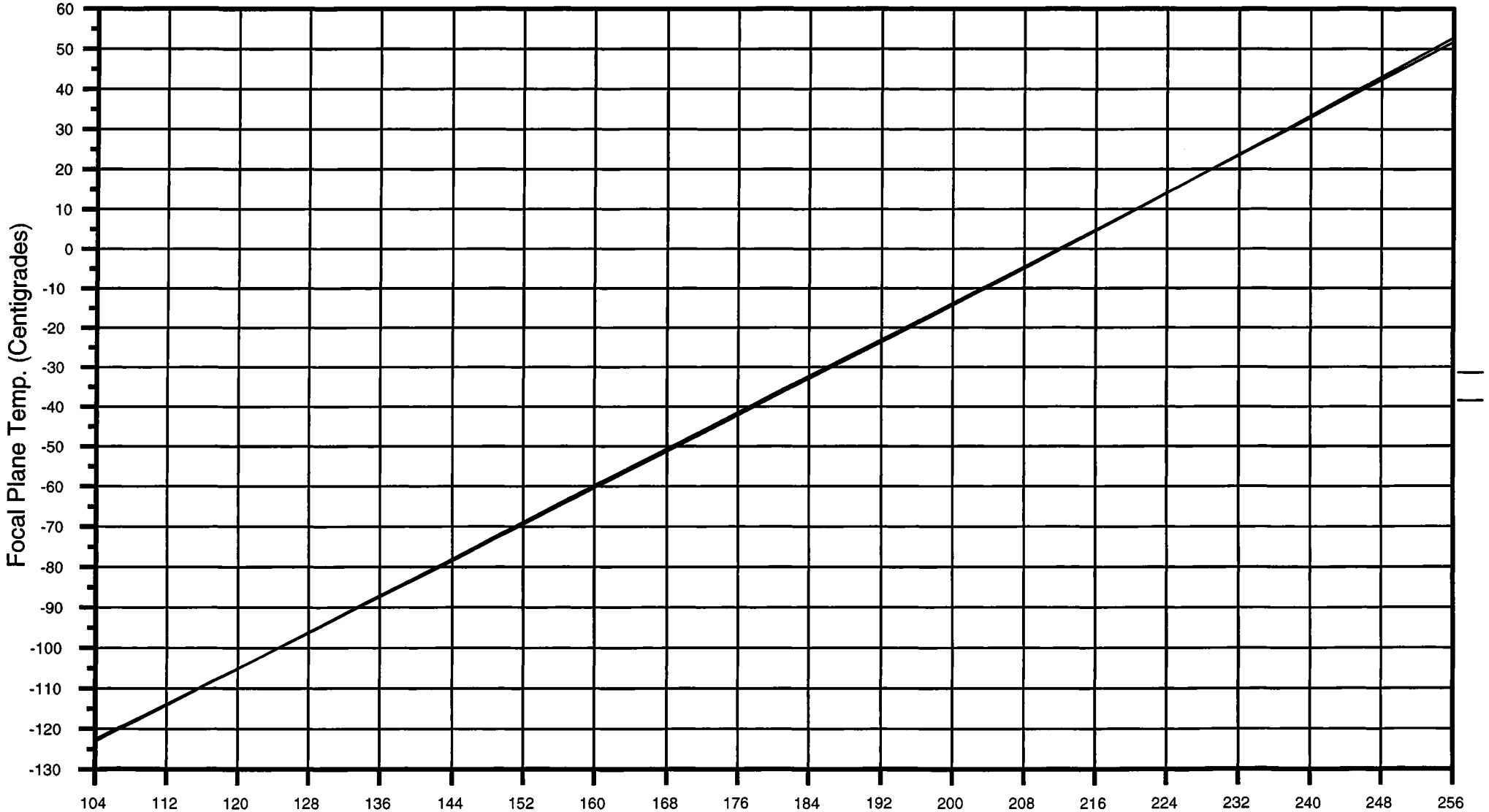
APPENDIX B

Table for assembly of Video Board Commands.

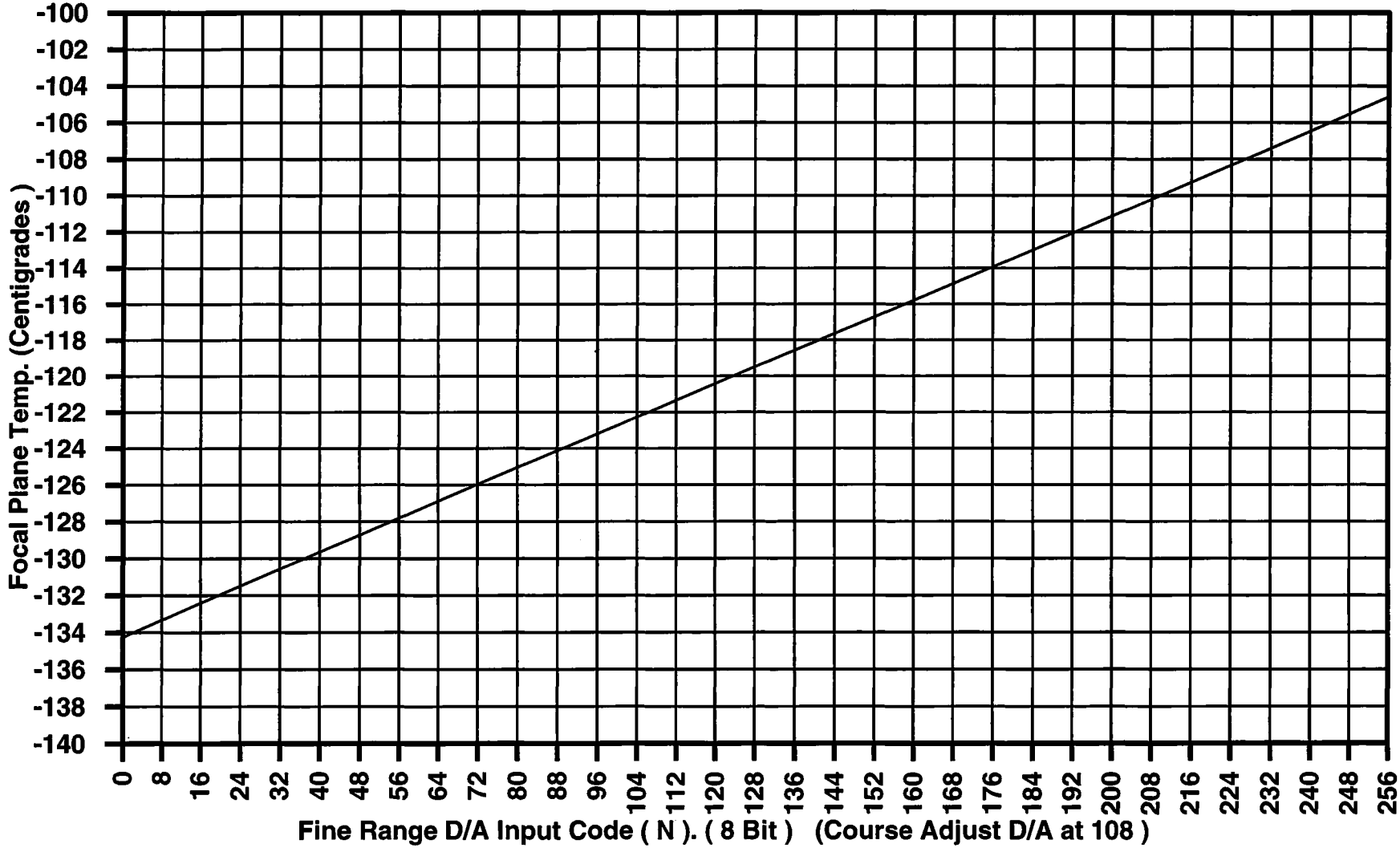
COMMAND	MODIFIER	HEX (add all selected numbers.)	DEC.	NOTES
Write - Address		200000	2097152	
	S.R.A.M Address	000000 - 007FFF	0 - 32767	
	P.R.A.M. Address	008000 - 00FFFF	32768 - 65535	
	Register Number	010000 - 01003F	65536 - 65599	Only first 4 used. (Table 3)
	D/A Conv.	010040 - 01005F	65600 - 65631	0-23 dec. (Table 4)
	A/D Conv.	010080 - 0100FF	65664 - 65791	(Table 5)
Write - Data		000000	0	
	Mem. Data	xxxx		
	D/A Conv	xxx		
Read - Address		600000	6291456	
Read - Data		400000	4194304	

COMMAND	MODIFIER	HEX
Card-select - Write		800000
	Select Any or All Cards to Write to	$\sum 2^{(W-1))}$ $1 \leq W \leq 10$ W = card no.
	Select one Card to Read from (Code= R)	00R000 R = 1 through 10
Cards-select - Read		C00000
		(Card with code= R, returns R in Bits 7-10 and 12-15 and sets check-bit 11 to 1)

Approx. Focal Plane Temperature Selection (T=1.1421N-241.67)



Focal Plane Temp Set Fine. (At Course Set N = 108)



Deviation From Lin. Fit. Due to RTD Prescision and Tolerances of other Components