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Detector Electronics Assembly(DEA) Hardware Specification and System Description
Rev 1.0

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1. OVERVIEW

1.1 INTRODUCTION

The Detector Electronics Assembly(DEA) provides all necessary electronic circuitry to operate the ACIS focal plane CCD detectors. Its main functions are to provide all static and dynamic stimulus; and to acquire and digitize X-ray induced image data from the detectors. This digitized image data stream is sent to the Detector Processing Assembly(DPA) for further processing.

The DEA is part of the ACIS experiment being designed for the AXAF-I satellite. Its main mission is to observe the X-ray universe, acquiring and sending image and spectral information back down to Earth.

This document defines the performance , design, and architecture of the DEA system. It also describes the interface requirements to the CCD detectors, the DPA, and the Power Supply Mechanism Control(PSMC) unit.

1.2 REFERENCES

ACIS-DD-012	"Technical Proposal to NASA for the AXAF CCD Imaging Spectrometer", 9/88
MIT Internal Doc	"HETE Lasagna Box User's Guide", T. Brady, J. Doty,
MIT Internal Doc.	" ACIS Onboard Data Management Requirements Analysis.", Rev 0.3 Draft
MIT-CSR 36-01101-04	"CEI Specification for AXAF ACIS", P. Gray, G. Garmire, 3/22/94
MIT-CSR 36-03001.02 Rev A	Block Diagram, DEA I/O & Control
MIT-CSR 36-03001.03 RevC	ACIS DEA Backplane Schematic
MIT-CSR 36-03001.04 Rev 3	DEA Interface Worksheet
MIT-CSR 36-03001.01 Rev E	ACIS DEA Subsystem Schematic
MIT-CSR 36-02205 RevC	"DPA/DEA Interface Control Document" Dorothy Gordon 5/4/94
MIT-CSR 36-03001.05 Rev I	DEA Thermal Control/Interface Board Schematic
MIT-CSR 36-02104 Rev C	"DPA Hardware Specification & System Description", Dorothy Gordon 5/4/94

1.3 LIST OF ACRONYMS AND ABBREVIATIONS

ACIS	AXAF CCD Imaging Spectrometer
ADC	Analog to Digital Converter
ADU	Analog to Digital Unit
AXAF	Advanced X-Ray Astrophysics Facility
BEP	Backend Processor
CCD	Charge Coupled Device
DAC	Digital to Analog Converter

DCS	Double Correlated Sampler
DEA	Detector Electronic Assemble
DN	Digital Number
e	Electron
FEP	Frontend Processor
FPGA	Field Programmable Gate Array
GSE	Ground Support Equipment
IDOP	Command Operation Identification
KPIX	Kilo Pixel (1000 Pixels)
LED	Light Emitting Diode
LSB	Least Significant Bit
N/A	Not Applicable
PSMC	Power Supply and Mechanism Control Unit
SRAM	Sequencer Random Access Memory
PRAM	Program Random Access Memory
TBD	To Be Determined
TBS	To Be Specified

2. DEA DESCRIPTION

2.1 SYSTEM

The DEA consists of 10 independent and identical subsystems which are also known as video cards. Each video card is uniquely tied to 1 of 10 CCDs on the ACIS focal plane and provides all necessary control and acquisition electronics to interpret the x-ray images that are formed on the sensors.. A complete video board consists of 5 sections; 1 driver section, 1 video section, 1 Digital Command Decoder/Sequencer section, 1 power regulation/isolation section, and 1 analog houskeeping section.

The driver section provides all clocking and bias signal requirements sent to the sensor. The video section provides all acquisition and digitization requirements for the signals received from the sensor. The digital command decoder/sequencer section provides all the intersectional timing, synchronization, and command decoding requirements to interrogate each sensor. The analog houskeeping section multiplexes a compliment of on card analog signals for diagnostic readout and to verify on board conditions.

The Video cards are commandable individually and collectively by the DPA. In addition to the 10 video cards which define the core of the system, 2 Thermal Control/Interface cards dedicated to the management of the CCD focal plane heaters and LEDs are included to form the full complement of the DEA. The entire system resides on a passive backplane.

2.2 REFERENCE CLOCKS

The DPA sources 3 reference clocks to the DEA. The 1.6 MHz command clock is used to synchronize command words sent. The DEA video cards listen to these commands and decoding and execution are performed only upon proper address identification. Details of the command structure is explained under section 3, "Command Structure" of this document.

The 6.4 MHz video clock is used by the DEA to synchronize the CCD digitized data stream, which ultimately is transmitted to the DPA for processing. All DEA video cards receive this reference clock and distributes it to their respective video sections.

The DPA also sources a 100 KHz clock which is utilized by the DEA to synchronized its sequencing operations. In addition, the PSMC also receives the 100 Khz reference clock to synchronize its switching regulators. In this manner, the power supply induced switching noise becomes in sync with the CCD signal acquisition process and thus,can be eliminated.

2.3 INTERFACES

2.3.1 INTRODUCTION

There are basically two interface requirements for the DEA.. One interface is to the ccd focal plane, and the other interface is to the DPA. The DPA interfaces are:

1) 10 independent digital video data streams with their associated sync and clock signals. These signals are sent in differential format from the DEA to the DPA and constitutes the high speed data interface. This interface is directly sourced by the video cards via the passive backplane in differential format.

2) 2 independent command and status data channels and associated reference clocks. These signals are in differential format and interfaces directly to the Thermal Control/Interface cards before distribution via the backplane. Detail interface

specifications can be found in the DPA/DEA Interface Control Document" 36-02205 Rev C.

2.3.2 DPA INTERFACE

There are 2 redundant DPA processors which commands and monitors the status of the DEA. They are the Backend Processors A and B(BEP-A, BEP-B). Commanding is either sourced by BEP-A or BEP-B, but not both. The command structure is such that The DPA can talk to the DEA video cards individually or collectively(broadcast mode). During normal operation, a maximum of 6 video cards can be under broadcast mode. The physical interface to the BEP's are through the Thermal Control/Interface cards on the DEA backplane. Detail specifications and clock timing protocols are shown in document 36-02205 Rev-C

There are 6 Front End Processors(FEP) on the DPA which receives and interprets digitized video images from the DEA video cards. Each FEP has 10 sets of receivers and thus, can interrogate any of the 10 ccds. However, only six ccds can be observed at any given time. Data, Sync, and Video Clock signals are driven directly from each video card and received at the FEP's. Detail timing protocols and signal names are specified in the DPA/DEA Interface Control Document.

On the DPA, there exist a group of discrete analog housekeeping channels such as power and temperature monitors It is the sole responsibility of the DEA Interface cards for analog houskeeping digitization, and therefore, this group of signal interfaces directly to the DEA Interface cards.

2.3.3 CCD INTERFACE

Each DEA video card also interface directly to 1 of 10 ccds on the focal plane. Their respective assignments are listed in the DPA/DEA Interface control document. The signal names, formats, programmable range and resolution are shown in the table below:

SIGNAL NAME	DEFINITION	SIGNAL TYPE	PROG. RANGE	PROG. RES.
P3-IA	Phase 3 Image Array	Dynamic Clock	-12.8V to +12.8V	50 mV/bit
P2-IA	Phase 2 Image Array	Dynamic Clock	-12.8V to +12.8V	50 mV/bit
P1-IA	Phase 1 Image Array	Dynamic Clock	-12.8V to +12.8V	50 mV/bit
P3-FS	phase 3 Frame Store	Dynamic Clock	-12.8V to +12.8V	50 mV/bit
P2-FS	Phase 2 Frame Store	Dynamic Clock	-12.8V to +12.8V	50 mV/bit
P1-FS	Phase 1 Frame Store	Dynamic Clock	-12.8V to +12.8V	50 mV/bit
DR-D	Drain-D	Static DC Bias	0V to +23V	50 mv/bit
DR-C	Drain-C	Static DC Bias	0V to +23V	50 mv/bit
DR-B	Drain-B	Static DC Bias	0V to +23V	50 mv/bit
DR-A	Drain A	Static DC Bias	0V to +23V	50 mv/bit
P1-OR-BD	Phase 1 Output Reg. BD	Dynamic Clock	-12.8V to +12.8V	50 mv/bit
P1-OR-AC	Phase 1 Output Reg. AC	Dynamic Clock	-12.8V to +12.8V	50 mv/bit

P2-OR-AC	Phase 2 Output Reg. AC	Dynamic Clock	-12.8V to +12.8V	50 mv/bit
P2-OR-BD	Phase 2 Output Reg. BD	Dynamic Clock	-12.8V to +12.8V	50 mv/bit
P3-OR	Phase 3 Output Reg.	Dynamic Clock	-12.8V to +12.8V	50 mv/bit
RAG	Reset Gate	Dynamic Clock	-12.8V to +12.8V	50 mv/bit
RD	Reset Diode	Static DC Bias	0V to +12.8V	50 mv/bit
SCP	Scupper	Static DC Bias	0V to +12.8V	50 mv/bit
OG	Output Gate	Static DC Bias	-12.8V to +12.8V	50 mv/bit
BJD	Back Junction Diode	Static DC Bias	+12V or +70V	assert/deassert bit
OUT-A	Video Output A	Analog Video A	Delta V=300 mV	charge dependent
RET-A	Video Output A Return	Video A Return	Video Gnd Ref.	n/a
OUT-B	Video Output B	Analog Video B	Delta V=300 mV	charge dependent
RET-B	Video Output B Return	Video B Return	Video Gnd Ref.	n/a
OUT-C	Video Output C	Analog Video C	Delta V=300 mV	charge dependent
RET-C	Video Output C Return	Video C Return	Video Gnd Ref.	n/a
OUT-D	Video Output D	Analog Video D	Delta V=300 mV	charge dependent
RET-D	Video Output D Return	Video D Return	Video Gnd Ref.	n/a
SUB1	Substrate 1	Substrate Gnd 1	CCD Chip Gnd	n/a
SUB2	Substrate 2	Substrate Gnd 2	CCD Chip Gnd	n/a
SUB3	Substrate 3	Substrate Gnd 3	CCD Chip Gnd	n/a

2.3.4 GSE INTERFACE

Under normal ground operation, there exists a video high speed tap whereby a single digital video data stream with its associated clocks, can be observed. This digital video data stream constitutes 1 of the 10 video cards on the DEA. The selectability of this data stream is commandable via software and is used only for ground support diagnostics. The physical access to this high speed tap is a connector on the DEA housing structure.

2.3.5 HANDSHAKING FORMAT

2.3.5.1 Commands

Command and status received by each card on the DEA have handshaking and timing formats as specified in the DPA/DEA Interface Control Document 36-02205 rev C. The presence of a command word is signified by the command word's logic level going low(start Bit). No separate sync pulse is required, although the serial command word is synchronized to the 1.6 MHz command clock.

2.3.5.2 Video

The video handshaking and timing specification for each video card is shown in DPA/DEA Interface Control Document 36-02205 rev C. A video sync pulse and a video clock is sent along with the video data.. The video word length is 64 bits wide and represents a group of 4 pixels worth of data. One pixel worth of data consists of 12 bits of magnitude and 4 bits of tag information. The video clock frequency is 6.4 MHz.

2.3.5.3 Status

See the DPA/DEA Interface Control Document 36-02205 Rev C for detail handshaking timing specification s

3. COMMAND STRUCTURE

3.1 INTRODUCTION

All cards resident on the DEA passive backplane listens to incoming commands from the DPA. Commands are decoded only if the command word contains the proper address field. In addition, broadcasting to multi-card decoding can occur simultaneously if the card select bit and Mask bits of a command word are asserted. The command word length is 24 bits wide.

3.2 COMMAND WORD STRUCTURE

The command word field specifications are shown in detail in the DPA/DEA Interface Control Document 36-02205 Rev C.

4. DEA VIDEO CARD FUNCTIONS

4.1 INTRODUCTION

A complete video card consists of 5 sections; 1 driver section, 1 video section, 1 Digital Command Decoder/Sequencer section, 1 power regulation section, and 1 analog houskeeping section.

The driver section provides all clocking and bias interface requirements sent to the ccd sensor. This includes all dynamic clocks with programmable voltage amplitudes.

The video section provides all acquisition and digitization interface requirements for the signals received from the ccd sensor. As the poly-phase clocks are sent to the ccd to initiate charge transference, the video section samples and digitizes, at the appropriate time, the charge equivalent voltage signal in 4 separate channels simultaneously. Thus, the readout rate of a ccd would be 4 times faster than if the ccd had only 1 output node.

The digital command decoder/sequencer section provides 3 important functions:

1) It provides command decoding and execution.

2) It provides video data time division multiplexing.

3) It provides all intersectional timing and synchronization requirements to readout each ccd sensor. One central Actel Field Programmable Gate Array is dedicated for this task.

The power regulator/control section provides on board power regulation and isolation of each video card. Its presence is crucial in low noise operations of the video cards and helps to eliminate inter-card crosstalk. It has the ability to turn on or off by the assertion/deassertion of a power control bit sent by the interface card. Flight software command dictates which video card is turned on.

The Analog Houskeeping section of a video board provides diagnostic signals which the flight software can access. Thus, the state of health and programmed verifications of the video card can be performed. All analog houskeeping channels are multiplexed and sent to the Interface card for digitization. It is the responsibility of the interface card for HK digitization and the subsequent status communication with the DPA.

4.2 DRIVER SECTION

4.2.1 OPERATIONAL DESCRIPTION

All bias and clock amplitude values required by the CCD sensors are programmable. These programmable values are held in DAC Banks resident on the driver section of the video card. The outputs of the DAC Banks are then electronically conditioned and amplified before final drive to the CCD. In addition to holding driver voltage values, the DAC banks must also hold voltage offset values for video data processing as required by the video section of the card. All dynamic clock switching is done by analog switches resident on the driver section. Timing and control of all ccd clocking signals are controlled by assign bits on the analog sequence bus. This bus is generated by the resident ACTEL chip with associated PRAM and SRAM memory devices and constitutes the SEQUENCER portion of the system. For detail information, please look under the ICD documentation and the ACIS DEA subsystem Schematic. The onboard DAC Bank registers and designations are listed below.

4.2.2 DAC FUNCTION

Driver DAC Control Channels

DAC Channel	*Signal Name*	*Resolution*	*range*
0 (DACPIA+)	Parallel Image Clock High (VPIA+)	8 bit	0.0v to 2.5v
1 (DACPIA- +)	Parallel Image Clock Low (VPIA-)	8 bit	0.0v to 2.5v
2 (DACPIA- -)	bi-polar capability		
3 (DACPFS+)	Parallel Frame Store Clock High(VPFS+)	8 bit	0.0v to 2.5v
4 (DACPFS- +)	Parallel Frame Store Clock Low(VPFS-)	8 bit	0.0v to 2.5v
5 (DACPFS- -)	bipolar capability		
6 (DACS+)	Serial Clock High(VS+)	8 bit	0.0v to 2.5v
7 (DACS-)	Serial Clock Low(VS-)	8 bit	0.0v to 2.5v
8 (DACR+)	Reset Clock High(VR+)	8 bit	0.0v to 2.5v
9 (DACR- +)	Reset Clock Low(VR-)	8 bit	0.0v to 2.5v
10 (DACR- -)	bipolar capability		
11 (DACSCP)	Scupper Bias(SCP)	8 bit	0.0v to 2.5v
12 (DACOG+)	Output Gate Bias high(OG+)	8 bit	0.0v to 2.5v
13(DACOG-)	Output Gate Bias Low(OG-)	8 bit	0.0v to 2.5v
14 (DACRD)	Reset Diode Bias(RD)	8 bit	0.0v to 2.5v
15 (DACDR0)	Drain A Bias(DR-A)	8 bit	0.0v to 2.5v
16 (DACDR1)	Drain B Bias(DR-B)	8 bit	0.0v to 2.5v
17 (DACDR2)	Drain C Bias(DR-C)	8 bit	0.0v to 2.5v
18 (DACDR3)	Drain D Bias(DR-D)	8 bit	0.0v to 2.5v
19 (AOFF)	Offset Voltage to video Chain A	8 bit	0.0v to 2.5v
20 (BOFF)	Offset Voltage to Video Chain B	8 bit	0.0v to 2.5v
21 (COFF)	Offset Voltage to Video Chain C	8 bit	0.0v to 2.5v
22 (DOFF)	Offset Voltage Video Chain D	8 bit	0.0v to 2.5v
23 Uncommitted	Uncommitted	8 bit	0.0v to 2.5v

4.3 VIDEO SECTION

4.3.1 OPERATIONAL DESCRIPTION

The video section processes 4 parallel analog video data streams from the ccd simultaneously. There are 4 identical video processing chains, each consists of a differential video clamping front-end amplifier, a dual slope integrator, an offset injection summing amplifier, and a 12 bit low noise ADC converter. All 4 digitized serial video data streams are then timed multiplexed at the actel controller chip before differentially driven to the FEPs. This data stream is synchronized to the 6.4 MHz video clock. 4 leading bits tagged along with the video stream is used to spatially stamp the video data and to identify the beginning of a CCD frame(Beginning Of Frame (BOF) Pixel) Total video pixel word length is thus, 16 bits wide., and the total multiplexed video word length is 64. The timing and control of the video section are determined by assigned bits on the analog sequence bus. This bus is generated by the sequencer portion of the actel with

associated ic memory components that are resident on the video card. Video ADC conversion is synchronized to the 100 Khz sync pulse and can be programmable delayed from the leading edge of this clock by up to 64 counts.(see ICD) For detail design information, please see the ACIS DEA Subsystem Schematics.

4.3.2 VIDEO GAIN

For the ACIS application, the nominal gain requirement is 1 ADU/e-. Utilizing a 12 bit ADC, the nominal dynamic range is approximately 4000 e-. The responsivity of the CCD at the x-ray energy of interest is approximately 25uV/e-. For a 4000e- system, the maximum voltage swing is approximately 100 mV, referenced at the video chain inputs. All gain components of the video chain s are designed such that the total dynamic input swing is translated to the 2.5 Volt reference value used by the ADC. For detail design information, please see the ACIS DEA subsystem Schematics.

4.3.3 VIDEO THROUGHPUT

A single pixel processing period is determined by the reference sync clock sent by the DPA. This clock is 100Khz, and thus a video pixel processing period is 10 us. The theoretical full frame process time for the ACIS 1 megapixal ccds is thus 2.62 seconds, when all video chains are processing simultaneously. This is known as bi-directional readout, when all 4 output nodes of the ccd are enabled. The ACIS ccds also have a unidirectional readout in which only 2 output nodes are active. Unidirectional readout is possible by providing reversal to its clock phases via software command. For bi-directional readout, the actual full frame process time is slightly higher than 2.62 seconds to account for integration and image to frame store transference time requirements. See the detail throughput calculations attached to this document for further detail.

4.4 DIGITAL COMMAND DECODER / SEQUENCER SECTION

4.4.1 OPERATIONAL DESCRIPTION

Each video card is controlled by an ACTEL FPGA. There are 2 major tasks under its jurisdiction. The first is command decoding and execration. The second is sequencer control. and execration.

4.4.2 COMMAND DECODING AND EXECRATION

There are 5 decoding and execration functions required by the ACTEL. They are as listed:

1) SEQUENCER

The resident ACTEL has the ability to write and to read from the Programmable RAM (PRAM) and Sequencer RAM(SRAM) devices. The contents of the SRAM is the Analog Sequence Bus, and cycling through SRAM will generate all interactive clocking and video processing waveforms required by the CCD. The analog sequence bus is 16 bits wide. The contents of PRAM dictate the readout configuration of the CCDs. See the ICD for sequencer related command specifications.

2) DAC BANKS

The DAC banks resident on the Video Cards are writeable devices only. The controlling ACTEL provides all addressing, clocks, and serial word streams to load the banks. All ADCs are loaded with a serial format, having a 8 bit magnitude. Addressing and command field specification can be access through the DPA/DEA Interface Control Document.

3) ADC

The resident ACTEL Controller provides all clocks and Start Conversion pulses to the DAC converters. Additionally, the controlling ACTEL also multiplexes all 4 ADC data streams along with tag bits for final data transmission. The ADC Start Conversion pulses are synchronized to the 100 Khz clock. and can be program delayed up to 64 counts. Detail addressing and command word format to the ADC can be seen in the DPA/DEA Interface Control Document.

4) HOUSEKEEPING ANALOG MUX

For operational diagnostic purposes, there are 19 analog channels that can be observed. The digitization and transmission of these signals are the responsibility of the Interface Cards. The controlling ACTEL provides all addressing and enable signals to switch the proper channel to the interface card for digitization. Detail command format for HK muxing is shown in the DPA/DEA interface Control Document.

5) CONTROL REGISTER FUNCTIONS

The assertion/deassertion of bits on discrete registers in the controlling ACTEL enables certain functions on the video card. Examples of these functions are, to start the sequencer, to enable the back junction diode voltage multiplier, and to enable clock phase swapping for bi-directional/unidirectional ccd readout.

Detail command addressing of these functions are listed in the DPA/DEA Interface control Document.

4.4.3. SEQUENCER CONTROL

Upon loading timing and control parameters into PRAM and SRAM, the controlling actel decodes and executes the Sequencer Start command sent by the DPA. The execration of the sequencer start command is synchronized to the 100Khz clock and can be programmable delayed by up to 64 counts. During normal operation, X-ray images will continue to transmit to the DPA FEP's until the video boards sees a Sequencer Stop Command. Thus, all video boards on the DEA are autonomous once the sequencer start command is executed. All commands directed at the sequencer are listed in the DPA/DEA Interface Control Document.

4.5 POWER REGULATION SECTION

4.5.1 OPERATIONAL DESCRIPTION

There exist 6 conditioned voltages on each video card. 5 of the 6 power conditioners incorporate Current Foldback Linear Regulation schemes. This design scheme safeguards against radiation induced latchup conditions that may occur during the operational life cycle of the ACIS instrument. In addition to independent short circuit shutdown, all conditioners are shutdown/turnon programmable. Video card power control commands are decoded at the Interface card, and their execration signals are distributed to their destination via the passive backplane. The list of the video card conditioners are listed below.

Conditioned Rail V	Name	Short Circuit Protection	Current Foldback Reg.
+24 Volts	+24CL	YES	NO
+15 Volts	+15CL	YES	YES

-15 Volts	-15CL	YES	YES
+5 Volts Analog	PFIVEACL	YES	YES
+5 Volts Digital	PFIVEDCL	YES	YES
-5 Volts	-5CL	YES	YES

4.6 VIDEO ANALOG HOUSEKEEPING

4.6.1 OPERATIONAL DESCRIPTION

All Video Card Analog Houskeeping channels are multiplexed onto the Analog HK Bus on the passive backplane. This bus routes the desire channel of the desired video card to the Interface Card. The Interface card then performs the Analog Housekeeping Digitization.

Also, there exists a digital status bus on the passive backplane which routes digital status signals from the Video Cards to the Interface Card. All digitized analog HK data and Digital status data are multiplex together at the Interface Card ACTEL controller before final differential transmission to the DPA.

Following is a list of the Video Card Houskeeping Channels. Detail channel address assignments are shown in the DPA/DEA Control Document.

CHANNEL ADDRESS	NAME	DEFINITION	DYNAMIC RANGE
65664	VPIA+	parallel image array high	-12.8V to +12.8V
65665	VPIA-	parallel image array low	-12.8V to +12.8V
65666	VPFS+	parallel frame store high	-12.8V to +12.8V
65667	VPFS-	parallel frame store low	-12.8V to +12.8V
65668	VS+	serial clock high	-12.8V to +12.8V
65669	VS-	serial clock low	-12.8V to +12.8V
65670	VR+	reset gate high	-12.8V to +12.8V
65671	VR-	reset gate low	-12.8V to +12.8V
65672	OG	output gate bias	-12.8V to +12.8V
65673	SCP	scupper bias	-12.8V to +12.8V
65674	RD	reset diode	-12.8V to +12.8V
65675	DR-A	drain bias node A	-38.4V to +38.4V
65676	DR-B	drain bias node B	-38.4V to +38.4V
65677	DR-C	drain bias node C	-38.4V to +38.4V
65678	DR-D	drain bias node D	-38.4V to +38.4V
65679	(NOT USED)	(NOT USED)	(NOT USED)

65680	RT4	Thermistor 4, v-bd temp.	-40C to +60C
65681	RT3	Thermistor 3,mem. temp	-40C to +60C
65682	RT2	Thermistor 2, v bd ADC	-40C to +60C
65683	RT1	Thermistor 1, v bd fpga	-40C to +60C

5.1 INTRODUCTION

Within the Detector Electronics assemble there are two redundant but not identical Interface Cards. These cards are referred to as the DEA 11 th and 12 th cards. The primary Interface Card is the 11 th Card and is fully populated However, the 12 th card is partially populated with redundant function components only. Under normal ACIS operation, command directives from BEP A go to the primary interface card first, setting initial conditions such as turning power on, before commands can be sent to the video cards.

5.2 INTERFACE CARD FUNCTIONS

The tasks that are performed by the interface cards are as listed. below:

1) RAIL POWER SWITCHING

The Primary Interface Card provides redundant power supply switching for the DEA by utilizing 5 sets of dual latching relays. The relays route either PSMC A side rails, or its redundant B side rails onto the DEA backplane. The format for power switching is 1 by 2, that is, each relay set delivers rail power to 2 video cards. Rail power to the video cards are switchable, where as rail power to the Interface cards are not switchable.

The primary Interface Card(card 11) receives its rail power from the A side power supply of the PSMC, whereas the secondary Interface Card(card 12) receives its power from the B side power supply. The Interface cards are active and listens to, and executes commands as long as the PSMC is on. In the event that both side A and B of the PSMC are on, the Primary Interface Card asserts command dominance and disables the 12 th card from any further command interaction.

Command directives for rail power switching are listed in the DPA/DEA Interface Control Document. Required rail powers for the DEA are listed below.

VIDEO	+6 Volt	-6 Volt	+15.5 Volt	-15.5 Volt	+24 Volt	----------
INTERFACE	+6 Volts	-6 Volts	+15.5 Volts	-15.5 Volts	+24 Volts	+28 Volts

2)POWER REGULATION

All regulated power on the Interface cards are current foldback, short circuit protected to safeguard against mission latchup scenarios. So long as the PSMC is on, these regulators are active. There are 2 regulated sources which powers critical components on the Interface cards. They are the +5 Volt and the -5 Volt regulated outputs.

3) COMMAND DECODING

The DEA Interface Cards receives commands, clocks, and status from either the DPA BEP A processor or the BEP B processor. The selection of either A or B is a 1 bit hard wired signal from the DPA. In the event this signal(Select) is broken, the Interface card defaults to A side commanding.

All command words, clocks, and status signals have differential drive/ receive format across the DPA/DEA interface. Distribution of clocks and commands from the Interface Cards to the Video Cards are designated into either A or B group of signals. The

distribution of these signals have single ended format and is done via the passive backplane. The resident command decoder on the interface cards are ACTEL FPGA's. Its detail design is under separate ACIS database documentation.

4) HK ADC CONVERSION

The digitization of all Analog Houskeeping signals is performed on the Interface Cards. Signal scaling, filtering, and selecting are also done on the Interface cards. The digitized information is sent back to the DPA on the Status transmission line. The HK ADC converters have 12 bits of resolution and is configured for bipolar operation. For detail HK channel command addressing , please refer to the DPA/DEA Interface Control Document.

5) THERMAL CONTROL

The control of the ACIS focal Plane temperature is the responsibility of the DEA Interface Cards. This is done by utilizing a close loop linear control system. The primary thermal control loop resides on the 11 th card, whereas the redundant thermal control loop resides on the 12 th card. The focal plane temperature is settable by 2, 8 bit DACs. One of which is for fine control, and the other, course control. Under bakeout condition, the issuance of the bakeout software command enables an additional heater on the focal plane for this purpose.

The thermal control transfer functions and command list are shown in the DPA/DEA Interface Control Document. Detail schematic diagram of the thermal control loop can be seen in the DEA Interface + Temperature Control Schematic Document 36-03001.05

6) LED CONTROL

The on/off control of the primary LED on the ACIS focal plane is the responsibility of the primary(11 th) interface cared. The on/off control of the secondary LED on the focal plane is controlled by the secondary(12 th) Interface card. The command word which activates the LED control bit is listed in the ICD.

7) VIDEO CARD POWER CONTROL

Under normal ACIS observation modes, 6 Video cards are sequentially powered on prior to parametric loading of operational software into the video cards. The assertion/deassertion of the video card power on bits is the responsibility of the Interface Cards. The command word and bit mapping of this command is listed in the ICD.

6. POWER REQUIREMENTS

Nominal operating voltage and current requirements for the Detector Electronics Assemble are are listed below. The conditions are for 6 of 10 video cards active and acquiring images. plus the 11 th Interface card active. Staggered parallel clock transference is assumed. Total maximum DEA power requirements are also shown. Detailed power specifications for the PSMC is under separate ACIS documentation(see ACIS database).

	+6 V	**-6 V**	**+15.5 V**	**-15.5 V**	**+24 V**	**+28 V**
Current (Amps)	1.768	0.748	0.441	0.273	0.099	0.147
Power(Watts)	10.608	4.488	6.835	4.232	2.376	4.116
Total DEA Electronics Power	28.539W					
Total Focal Plane Heater Power	4.116W					
Total DEA Power	32.655W					

7. DEA BACKPLANE

The DEA Backplane contains 12 on-board connectors and 6 off-board connectors. The on-board connectors are used for the full compliment of the DEA resident circuit card assembles; namely, 10 video cards and 2 Interface cards. The off-board connectors are utilized to route signals to and from the BEP. FEP, and the High Speed Data tap. Rail power from the PSMC A and B power supplies interfaces directly onto connectors on the primary Interface Card. The DEA Backplane contains no active components and is completely passive. For further detail, see the backplane schematics in the ACIS DEA database.

8. PHYSICAL SPECIFICATIONS

The physical specifications are under separate ACIS documentation.

APPENDIX A: THROUGHPUT CALCULATION

The frame rate of a CCD is govern by the throughput of the Analog to Digital Converters(ADC).

The ADC is the CS5012A or equivalent which has a nominal throughput of 100 KHz.

The DEA is utilizing a 16 bit system, 12 bit ADC plus 4 tag bits.

The CCD imaging area is processed in quadrants. All 4 quadrants are processed simultaneously.

There are 256 * 1026 =262656 pixels per quadrant. To process a pixel requires 1/(100 KHz)= 10 usec(governed by ADC throughput).

To process a quadrant of pixels require 262656 * 10 usec.= 2.626 seconds.

Since all 4 quadrants are processed in parallel, the frame rate is also 2.626 seconds. Actual throughput is slightly higher because of parallel pixel transference and image integration time.

To Time Division Multiplex(TDM) all 4 quadrants into 1 data stream, each quadrant must occupies 1/4 * (throughput time)= 1/4 * (10 usec)= 2.5 usec..

Since the ACIS DEA is a 16 bit system, the throughput bit rate is 16 bits/2.5 usec = 6.4 Mbits/sec..

APPENDIX B: TOP LEVEL SCHEMATICS

The ACIS DEA top level schematics are under separate ACIS documentation. See the ACIS database.