REVISIONS

Letter	ECO No.	Description	Checked	Approved	Date
A	36-133	INITIAL RELEASE	FJK	RFG	3/15/95
B	36-366	INCORPORATE MSFC NEGOTIATED REQUIREMENTS	RFG	WFM	10/11/95
C	36-410	ADD CONFORMAL COATING AND CHANGE SOLDER MASK	RFG	WFM	11/6/95
D	36-425	ADD GLASS TRANSITION AND NHB ALTERNATES	FJK	WFM	12/6/95
E	36491	ADD SOLDER MASK ALTERNATIVES	FJK	WFM	2/15/96
F	36-572	Correct IPC Spec. Number and add 3 ounce /ft^2 copper specification	BK	[illegible]	4/16/96

NAME	DATE
Drawn: Brian Klatt	3/13/95
Checked: F. Kasparian	3/13/95
Approved: R. F. Goeke	3/15/95
Released: D. Gage	3/15/95

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CENTER FOR SPACE RESEARCH

PRINTED WIRING BOARDS

Size	Code Identification No.	Drawing No.	Rev.
T	80230	36-02105	F

Scale: NONE

1.0 SCOPE

This drawing defines the design, fabrication, test, and inspection requirements of double sided and multilayer printed wiring boards (PWB's), for use in the Advanced Xray Astrophysics Facility (AXAF). These PWB's will be used in an experiment in an Earth orbiting satellite at an altitude of 10,000 km. by 140,000 km.

2.0 APPLICABLE DOCUMENTS

2.1 The following documents form a part of this specification to the extent specified herein. Unless otherwise specified, the latest released version on the date of invitation to bid, is applicable.

STANDARDS

IPC-CF-150F	Metal Foil for Printed Wiring Applications (Institute for Printed Circuits Standard)
IPC-D-275 (MIL-STD-275)	Printed wiring for electronic equipment

SPECIFICATIONS

MIL-P-55110	General Specification for Printed Wiring Boards
MIL-P-13949	Plastic Sheet, Laminated, Metal Clad (For Printed Wiring Boards), General Specification For
MIL-C-14550	Copper Plating (Electrodeposited)
MIL-P-81728	Plating, Tin Lead (Electrodeposited)

HANDBOOKS

NHB5300.4 (3I)	Requirements for Printed Wiring Boards
NHB5300.4 (3K)	Design Requirements for Rigid Printed Wiring Boards and Assemblies

MIT

36-02106	PC Design - Component Library

2.2 ORDER OF PRECEDENCE In the event of conflict between the text of this document and the references cited herein, the text of this document takes precedence.

3.0 REQUIREMENTS

3.1 PWB DESIGN: The goal for printed wiring board (PWB) design is per NHB5300.4 (3K). The requirement for the design of printed wiring boards is IPC-D-275, as modified by this specification.

3.1.1 Minimum external annular ring for plated-through holes is .005 inch, and .015 inch for non-plated-through-holes.

3.1.2 Minimum annular ring on internal layers of multilayer boards is .002 inch.

3.1.3 Conductor thickness and width for external layers should be per figure 6-1 of NHB5300.4(3K), assuming a 20°C rise.

3.1.4 Conductor thickness and width for internal layers should be per figure 6-2 of NHB5300.4(3K), assuming a 20°C rise.

3.1.5 Minimum conductor spacing should be per table 6-1 of NHB5300.4(3K). If this requirement cannot be met, the conductor spacing may be reduced, but not less than the conductor spacing requirements of IPC-D-275.

3.1.6 Board Thickness: The thickness of finished multilayer boards as measured over the outside plating shall be per the PWB drawing. The thickness of double sided boards is determined by the material specification.

3.2 PWB LAYOUT AND OUTLINE

3.2.1 Layout: PWB layout shall be in accordance with the applicable MIT schematic and associated parts list.

3.2.2 Outline: PWB outline and layer assignments shall be in accordance with the applicable MIT outline drawing.

3.2.3 Surface Mount Land Patterns: Land patterns shall be in accordance with 36-02106.

3.2.4 Reference designators: Reference designations are identified on the schematic drawing. The reference designators shall be marked adjacent to or within the envelope of the component, where possible, on the PWB.

3.3 MATERIAL

3.3.1 Double Sided and Multilayer Boards: The copper clad laminated sheet and bonding material shall be in accordance with MIL-P-13949. Copper foil shall be in accordance with IPC-CF-150F, type HTE, class 3, for 1 and 2 ounce/ft.^{2} copper. Copper foil shall be in accordance with IPC-CF-150F, type C, class 1, for 3 ounce/ft.^{2} copper.

MATERIAL USAGE

MIT PCB P/N	TYPE	CLAD	BOND	CIC	SOLDER MASK
36-30201.01	ML	/10(GI)	/13(GI)	YES	YES
36-30202.01	ML	/10(GI)	/13(GI)	YES	YES
36-30203.01	ML	/4(GF)	/12GF	NO	YES
36-30301.01	ML	/10(GI)	/13(GI)	YES	YES
36-30302.01	ML	/10(GI)	/13(GI)	YES	YES
36-30304.01	ML	/4(GF)	/12(GF)	NO	YES
36-30317.01	ML	/4(GF)	/12(GF)	NO	YES
36-10102.0201	DS	/22(AB)	-	-	NO

3.3.2 Solder Mask: Solder Mask shall be SR-1000, Vacrel 8140, Ciba-Geigy Probimer 52, or Conformask 2000. Solder mask must be applied over bare copper.

3.3.3 Copper Invar Copper (CIC): The CIC foil shall be in accordance with MIL-P-13949. The CIC shall be nominally .006 inches thick with copper to invar in the ratio of 12.5% - 75% - 12.5%.

3.4 PLATING

3.4.1 Copper: Plated through holes and outside layer conductor shall be copper plated per MIL-C-14550 to a minimum thickness of 0.001 inch.

3.4.2 Tin-lead: Tin-lead plating shall be in accordance with MIL-P-81728, followed by reflow. Tin content is to be maintained at or above 58%. Tin lead fusing via hot oil reflow process is preferred, however, infrared leveling may be used.

3.5 FABRICATION PWB's shall be fabricated in accordance with MIL-P-55110 and this specification.

3.6 WARP AND TWIST Printed Wiring Boards shall not have warp or twist resulting in a total deviation from a flat plate exceeding 0.010 in/in.

3.7 IDENTIFICATION AND MARKING Marking shall be on the part mounting side and shall include, as a minimum:

Marking	Obtained from
Manufacturer's Name	PWB Manufacturer
Manufacturer's P/N	PWB Manufacturer
PWB P/N and Rev. level	MIT Outline Drawing
PWB Name	MIT Outline Drawing

3.7.1 Serial Number: Each PWB shall be uniquely serialized with a three (3) digit number, starting with 201 for Engineering boards and starting with 301 for flight boards, as stated in the purchase order.

3.8 WORKMANSHIP Workmanship shall be of a quality which will assure a product free of foreign materials, burrs, corrosion, scratches, chips, sharp edges, particles, or other defects which could affect serviceability or appearance.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 RESPONSIBILITY FOR INSPECTION Unless otherwise specified in this document, the PWB manufacturer is responsible for all inspections, examinations, and tests, as specified herein.

4.2 QUALITY CONFORMANCE INSPECTION (QCI) TEST COUPONS

4.2.1 Quality conformance inspection shall be in accordance with MIL-P-55110. A total of three (3) coupons are required per panel. Coupons shall be clearly marked to identify panel and boards represented by the coupon.

4.2.2 Disposition of coupons: The PWB manufacturer shall inspect one (1) coupon per this specification, deliver one coupon per panel to MIT and archive one coupon.

4.2.3 Configuration: The configuration of the test coupons will conform to IPC-D-275

4.2.4 Coupon Microsections

4.2.4.1 Coupons for multi-layer PWB's require a pad at each layer of the microsection.

4.2.4.2 There shall be no delamination of the individual layers or plies when viewed in the microsection.

4.2.4.3 Plating voids are not permitted when viewed in the microsection.

4.3 ACCEPTANCE TESTS The circuitry of each board (100%,) shall be tested for continuity and shorts in accordance with paragraph 3I516, subparagraph 10, of NHB5300.4 (3I). The minimum insulation resistance shall be greater than 100 Megohms at 60 V DC.

4.3.1 Visual Inspection: The PWB shall be inspected to insure that it meets the size and pattern requirements of the outline drawing, and the identification and marking requirements of 3.7 herein. Measling and crazing of the bare boards shall not exceed 2% of the board area, and shall not reduce the spacing by more than 25%.

4.4 INSPECTION AND TEST RECORDS Test data for all acceptance/screening tests and inspections shall be submitted to MIT with the delivery of the PWB. In addition, the PWB manufacturer shall maintain inspection and test records for 36 months after PWB delivery to MIT.

4.5 PRODUCT UNIFORMITY All PWB's of a given part number and revision, delivered to MIT, shall be made with the same design, materials, processes, and procedures, and shall be tested and inspected to the same criteria conforming to this specification.

5.0 PRESERVATION AND STORAGE

5.1 PACKING, PACKAGING, AND MARKING Preservation, packing, packaging, and marking shall be in accordance with MIL-P-55110, paragraph 5.0, for immediate domestic usage.

6.0 NOTES

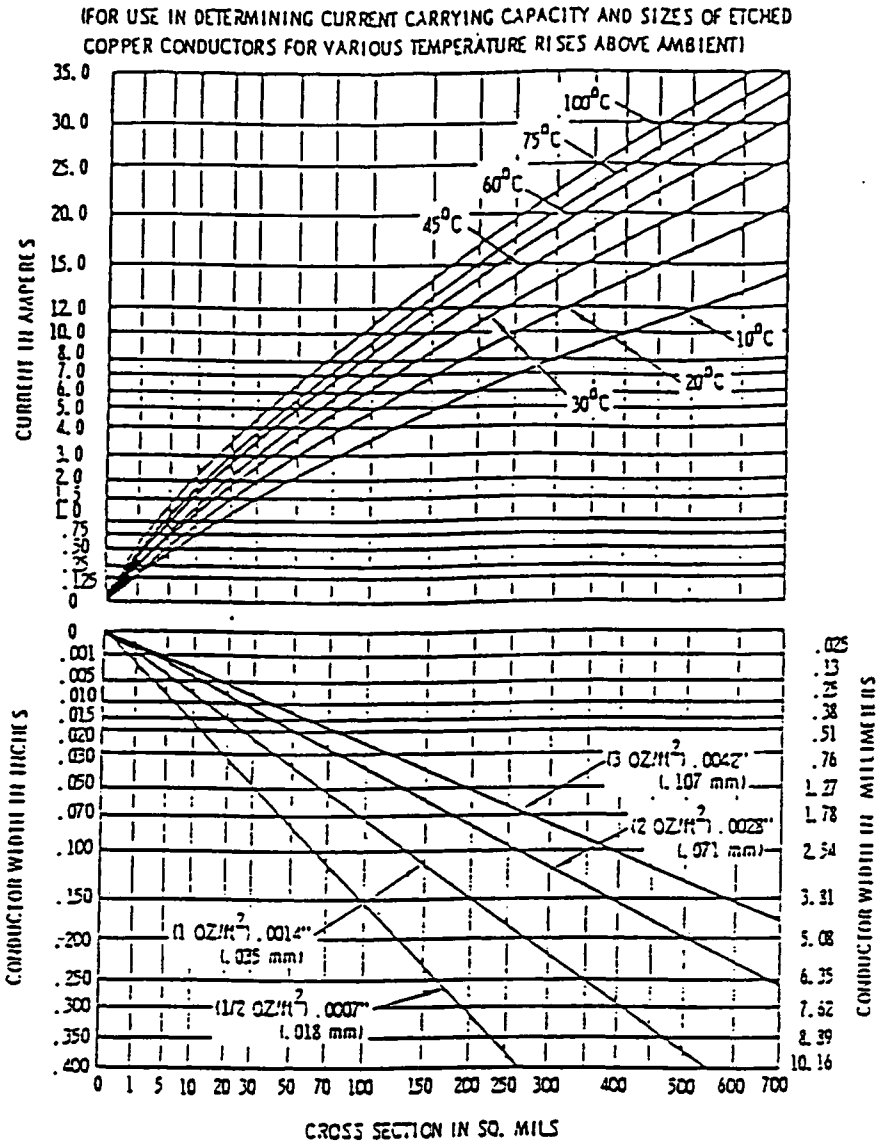
6.1 APPROVED SOURCES OF SUPPLY

LAYOUT

TBD

FABRICATION

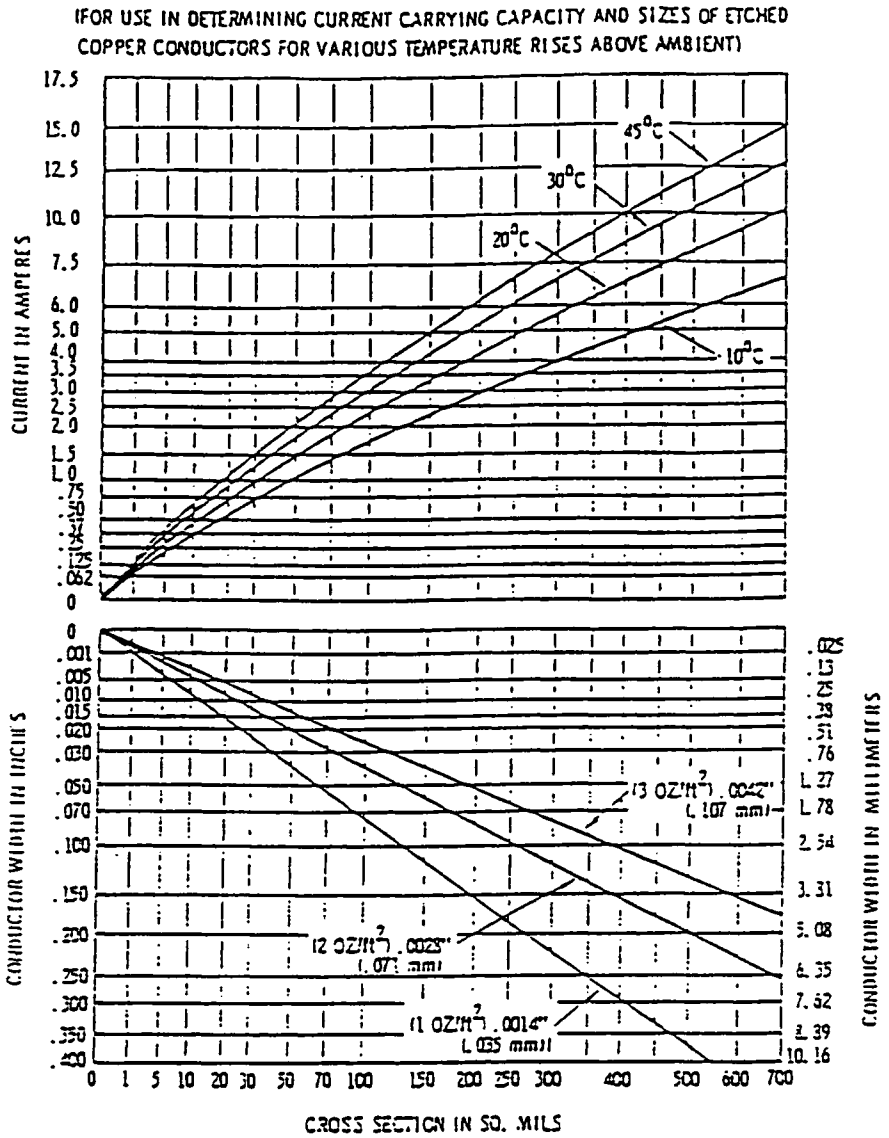
TBD



NOTES:

1. THE DESIGN CHART HAS BEEN PREPARED AS AN AID IN ESTIMATING TEMPERATURE RISES (ABOVE AMBIENT) VS CURRENT FOR VARIOUS CROSS-SECTIONAL AREAS OF ETCHED COPPER CONDUCTORS. IT IS ASSUMED THAT FOR NORMAL DESIGN CONDITIONS PREVAIL WHERE THE CONDUCTOR SURFACE AREA IS RELATIVELY SMALL COMPARED TO THE ADJACENT FREE PANEL AREA. THE CURVES AS PRESENTED INCLUDE A NOMINAL 10 PERCENT DERATING (ON A CURRENT BASIS) TO ALLOW FOR NORMAL VARIATIONS IN ETCHING TECHNIQUES, COPPER THICKNESS, CONDUCTOR WIDTH ESTIMATES, AND CROSS-SECTIONAL AREA.
2. ADDITIONAL DERATING OF 15 PERCENT (CURRENT-WISE) IS SUGGESTED UNDER THE FOLLOWING CONDITIONS:
   (a) FOR PANEL THICKNESS OF 1/32 INCH OR LESS.
   (b) FOR CONDUCTOR THICKNESS OF 0.0042 INCH (3 OZ/FT²) OR THICKER.
3. FOR GENERAL USE THE PERMISSIBLE TEMPERATURE RISE IS DEFINED AS THE DIFFERENCE BETWEEN THE MAXIMUM SAFE OPERATING TEMPERATURE OF THE LAMINATE AND THE MAXIMUM AMBIENT TEMPERATURE IN THE LOCATION WHERE THE PANEL WILL BE USED.
4. FOR SINGLE CONDUCTOR APPLICATIONS THE CHART MAY BE USED DIRECTLY FOR DETERMINING CONDUCTOR WIDTHS, CONDUCTOR THICKNESS, CROSS-SECTIONAL AREAS, AND CURRENT CARRYING CAPACITY FOR VARIOUS TEMPERATURE RISES.
5. FOR GROUPS OF SIMILAR PARALLEL CONDUCTORS, IF CLOSELY SPACED, THE TEMPERATURE RISE MAY BE FOUND BY USING AN EQUIVALENT CROSS-SECTION AND AN EQUIVALENT CURRENT. THE EQUIVALENT CROSS-SECTION IS EQUAL TO THE SUM OF THE CROSS-SECTIONS OF THE PARALLEL CONDUCTORS, AND THE EQUIVALENT CURRENT IS THE SUM OF THE CURRENTS IN THE CONDUCTORS.
6. THE EFFECT OF HEATING DUE TO ATTACHMENT OF POWER DISSIPATING PARTS IS NOT INCLUDED.
7. THE CONDUCTOR THICKNESSES IN THE DESIGN CHART DO NOT INCLUDE CONDUCTOR OVERPLATING WITH METALS OTHER THAN COPPER.

FIGURE 6-1
CONDUCTOR THICKNESS AND WIDTH FOR TYPE 1, TYPE 2, AND EXTERNAL LAYERS OF TYPE 3 PRINTED WIRING BOARDS



NOTES:

1. THE DESIGN CHART HAS BEEN PREPARED AS AN AID IN ESTIMATING TEMPERATURE RISES (ABOVE AMBIENT) VS CURRENT FOR VARIOUS CROSS-SECTIONAL AREAS OF ETCHED COPPER CONDUCTORS. IT IS ASSUMED THAT FOR NORMAL DESIGN CONDITIONS PREVAIL WHERE THE CONDUCTOR SURFACE AREA IS RELATIVELY SMALL COMPARED TO THE ADJACENT FREE PANEL AREA. THE CURVES AS PRESENTED INCLUDE A NOMINAL 10 PERCENT DERATING (ON A CURRENT BASIS) TO ALLOW FOR NORMAL VARIATIONS IN ETCHING TECHNIQUES, COPPER THICKNESS, CONDUCTOR WIDTH ESTIMATES, AND CROSS-SECTIONAL AREA.
2. ADDITIONAL DERATING OF 15 PERCENT (CURRENT-WISE) IS SUGGESTED UNDER THE FOLLOWING CONDITIONS:
   (a) FOR PANEL THICKNESS OF 1/32 INCH OR LESS.
   (b) FOR CONDUCTOR THICKNESS OF .0042 INCH (3 OZ/FT²) OR THICKER.
3. FOR GENERAL USE THE PERMISSIBLE TEMPERATURE RISE IS DEFINED AS THE DIFFERENCE BETWEEN THE MAXIMUM SAFE OPERATING TEMPERATURE OF THE LAMINATE AND THE MAXIMUM AMBIENT TEMPERATURE IN THE LOCATION WHERE THE PANEL WILL BE USED.
4. FOR SINGLE CONDUCTOR APPLICATIONS THE CHART MAY BE USED DIRECTLY FOR DETERMINING CONDUCTOR WIDTHS, CONDUCTOR THICKNESS, CROSS-SECTIONAL AREAS, AND CURRENT CARRYING CAPACITY FOR VARIOUS TEMPERATURE RISES.
5. FOR GROUPS OF SIMILAR PARALLEL CONDUCTORS, IF CLOSELY SPACED, THE TEMPERATURE RISE MAY BE FOUND BY USING AN EQUIVALENT CROSS-SECTION AND AN EQUIVALENT CURRENT. THE EQUIVALENT CROSS-SECTION IS EQUAL TO THE SUM OF THE CROSS-SECTIONS OF THE PARALLEL CONDUCTORS, AND THE EQUIVALENT CURRENT IS THE SUM OF THE CURRENTS IN THE CONDUCTORS.
6. THE EFFECT OF HEATING DUE TO ATTACHMENT OF POWER DISSIPATING PARTS IS NOT INCLUDED.
7. THE CONDUCTOR THICKNESSES IN THE DESIGN CHART DO NOT INCLUDE CONDUCTOR OVERPLATING WITH METALS OTHER THAN COPPER.
8. THE CURRENT MAY BE UP-RATED 100 PERCENT FOR EXTERNAL CIRCUITRY.

FIGURE 6-2
CONDUCTOR THICKNESS AND WIDTH FOR INTERNAL LAYERS OF TYPE 3 BOARDS

TABLE 6-1
CONDUCTOR SPACING FOR COATED BOARDS

Voltage Between Conductors DC or AC Peak	Minimum Spacing (Inch)	(mm)
0 to 15	0.005	(0.13)
16 to 30	0.010	(0.25)
31 to 50	0.015	(0.38)
51 to 100	0.020	(0.51)
101 to 300	0.030	(0.76)
301 to 500	0.060	(1.52)
Greater than 500	0.00012 1/	(0.003)1/

1/ Inch (mm) per volt.