RFG

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CCD Description (CCID-10)

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LINCOLN LABORATORY CCID10 DEVICE

1.0. INTRODUCTION

The Lincoln Laboratory CCID-10 CCD imager is a 1024x1024-pixel frame-transfer device (Fig. 1). The pixel's three phase polysilicon on nitride clock structure provides high yield, high charge transfer efficiency and is relatively insensitive to bias levels. Small charge packets (~4e$^-$) have been transferred through nearly 1300 pixels with no noticeable image quality degradation. The device layout allows 3 side abbutting so that close spacing of devices can be achieved in both the imaging and spectrometer array in ACIS. The CCID-10 output transistor has been designed to have high output responsivity and low noise at a 1 MHz or lower pixel rate. Most devices tested at Lincoln Laboratory have been measured to have less than 6 electrons rms equivalent noise when run at 4 Mpixel/second (1 Mpixel/second at 4 outputs).

2.0 GENERAL USAGE RECOMMENDATIONS

A. CCDs are susceptible to static charge damage. Do not handle them unless the handler is well grounded and the mating sockets are grounded.

B. Do not insert/remove a CCD from its socket unless power is off and the ground returns are the same as the handler's ground.

C. Never short the video output to any voltage, including ground.

D. Current limit all biases. Most biases require less than 10mA. Clock currents can be high; be careful with clocks.

E. Keep lead lengths as short as practical. Lincoln has been using RG-170 coax for video and clock signals with video cable lengths up to 10" and clock cable lengths up to 18" to permit locating electronics outside the vacuum test chamber. All biases are usually capacitor decoupled at the socket pins with 0.01pF ceramic capacitors. An exception is the RD bias, which drains off all the photo charge, and may be measured with a picoammeter. The RD bias then should be filtered with a very low leakage capacitor, such as one with a Teflon dielectric.

F. It is not necessary to keep the CCD darkened. Damage levels of light are substantially greater than normal room lighting, even when powered.

G. If necessary, the CCD can be cleaned by rinsing with highly purity acetone with power off. This should only be attempted at by Lincoln Laboratory personnel.

H. Before cooling the CCD, it must be in a water free environment, either dry nitrogen or high vacuum. It is recommended that the environment be a vacuum of $1x10^{-5}$ Torr or less before attempting to cool the CCD. Water condensing on an operating CCD is likely to destroy the CCD.

3.0 CCD DESCRIPTION

3.1. Specification, Front Illuminated CCID10

Array size	1024x1026 pixels, imaging area
1024x1026 pixels, storage area	
Imaging area	24.576x24.624 mm, 605.1 mm^2
Pixel size	24 m square, imaging area
21x13.5 m, storage area	
Clock rate	Up to 1.0 MHz serial clocks on each of 4 ports
Output Amplifier Gain	11V/electron, nominal
Operating Temperature	-135°C to +40°C
Output Amplifier Noise	< 6 electrons rms @ -50°C and 1.0 MHz
Full Well Capacity	> $1x10^5$ electrons
Read Time	266 ms, nominal @ 1.0 MHz

3.2 Description

3.2.1 Chip Architecture

Figure 1 depicts the basic layout of the chip. The imaging array is 1024 columns by 1026 rows with 24-m pixels. The bottom two rows (#1025 and 1026) were added to accommodate misalignment of the framestore shield. Row 1026 actually lies at the top of the tapered section because of a design constraint and therefore has smaller, non-square pixels. Therefore, these two rows will generally not have the same responsivity as the remaining pixels and would not normally be used. The imaging array is not partitioned, that is, the entire array must be clocked as a whole. Both right and left ends of the poly fingers are driven from metal clock busses in order to provide maximum clocking speed. The maximum parallel rate should be approximately 400 kHz.

The frame store is partitioned into two independent halves, labelled "AB" and "CD" to correspond to the output circuit labelling shown later. Each section has 512 columns and 1026 rows and can be independently clocked. Pixel size in the non-tapered section is 21 X 13.5 m. There is no transfer gate separating the frame store from the output register.

The serial or output register allows charge to be directed to either of two output ports at the ends of the register. Moreover, the clock busses are partitioned in a manner that allows the left and right halves of the register to be clocked in opposite directions. Figure 2 illustrates in detail the design of the register and two

of the options for clocking. Each register has five clock connections, with independent phases 1 and 2 for the left and right halves and a phase 3 which is common to both halves. In Figure 2a the two P1 and P2 busses are connected off-chip, and the result is that the left half of the register is clocked to the left port ("A" in this case) and the right half to the right port ("B"). In Figure 2b the P1 and P2 connections are interchanged, and the entire register is clocked to the A port. A change in the clocking sequence will, of course, allow the direction of charge transfer to be reversed toward the B port.

Figure 3 shows details of the gate arrangement as an aid in deriving a timing sequence for the device and illustrates the output sensing circuit. As in earlier devices, there are four extra stages between the first column and the output. The left and right halves of the serial register and the corresponding output circuits are precise mirror images of each other. This means that the output signals should have nearly identical characteristics, including the more subtle features such as clock feedthrough from the serial register.

The output circuits of the CCID-10 use the same design as a previous 420 X 420 frame-transfer device, which was used in the ASCA instrument, and therefore should have the same responsivity, noise and bandwidth. The output circuits of the CCID-10L device are modified to have reduced sense-node capacitance and therefore increased responsivity and reduced noise. A single-stage source follower with an off-chip load resistor is used and feeds the gate of a U309 which also is to be used in the follower mode. Both the first-stage load resistor and U309 are placed inside the package next to the CCD, but the U309 load resistor must be supplied outside the package by the user. The responsivity of the CCID-10 output is approximately 8-10 V/e^-, and the output bandwidth constrains the maximum serial data rate to about 1.7 MHz. Measurements here and at MIT/Center for Space Research have demonstrated noise levels down to 4 e^-.

3.2 Packaging

The packaging of the device is detailed in Figure 4 and the drawings of the focal plane assembly. Table 1 and Figure 5 detail the pin out and flexprint circuitry. Because the chip design has mirror symmetry about a line running down the center, both front- and back-illuminated versions of the chip will have identical pinouts. The lead labelled "back junction" is used only if the front-illuminated version of the device is used.

Provisions have been made for two types of temperature sensors, which will be mounted at several placed on the focal plane paddle. The first option is a Pt RTD which is manufactured in a thin-film version by Omega. Four leads are brought out for this two-terminal device so that a four-terminal measurement of the sensor resistance is possible. Also mounted on the focal plane paddle will be several heater cartridges. These will be used to assist with temperature regulation and to evaporate contaminates that condense on the chip.

3.3 Testing

In general, the set of biases and clock levels as suggested below is used, but for optimum noise performance it is often advantageous to explore slightly different levels. The levels most likely to affect noise performance are the DR and RG levels.

CLOCKS:	Low	High	
IA and FS clocks:	-6	+4	Inversion mode
	0	+10	Non-inversion mode
OR:	0	+10	
RG:	+4	+11	

DC BIASES:	
DR:	+18
RD:	+12
OG:	+2
SCP:	+10

4.0 TIMING DESCRIPTION

All registers in the CCD are three phase clocked. The attached timing flow charts (Figures 6 through 10) show the general strategy taken timing control. Prior to being read, the CCD is in an idle sequence where the serial and reset clock are constantly running to bleed off dark current in the serial register. When a READ command is received, the serial clocks are stopped with phase 2 high (the end of a serial sequence, step F) and 1026 parallel transfers are run, with both image and storage area clocks run simultaneously. The parallel transfer is run at a rate of 4 s/line.

Once the charge has been transferred into the storage area, a new integration time starts and the previous signal can be read. (Each of the 4 serial registers are usually read-out separately in the "bi-directonal" mode.) First, a parallel line sequence puts the first line (trashy data) into the serial register (serial clock phase 2 high) and the serial register is clocked for 266 serial clock sequences, one per pixel. The first 4 pixels are the extended register pixels and contain data which can be used as a black reference. The next 256 pixels contain the real imaging data for the line being read. The last 6 pixels are equivalent to an overscan and contain no signal, except for dark current acquired during the serial readout, usually a very small charge. Lincoln prefers to use one of the overscan pixels for black reference, as they have no residual parallel clock artifacts. It is optional to read out more than 260 pixels. The pixel order on two of the four read ports must be reversed to reconstruct the image.

During a serial sequence, the video waveform contains several pieces of information. At step 0, the reset clock injects a pulse into the video, typically less than 0.15 volts positive amplitude. Immediately after the reset pulse, there are no serial clocks, which gives the output time to settle for the first sample of the correlated double sample and hold. This settled level has a noise caused by the KTC noise of the reset sense capacitor. At the mid point of the serial sequence, the remaining clock activity occurs, followed by a quiet time for settling. This second plateau has the actual video in it. The change shifts the voltage level negative from the reset plateau reference level.

The line read sequence is repeated 1025 times to clear out all the charge transferred into the storage area. More lines could be clocked, if desired, but they will not contain any useful information. At the end of a read, the CCD continues integrating with the serial clock constantly running in their idle sequence.

5.0 REFERENCES

1. B. E. Burke et al, "420X420 charge-coupled-device imager and four-chip hybrid focal plane", Optical Engineering, sep 1987, Vol.26, No.9, p.890.

2. D. C. Harrison, Barry E. Burke, "Large area focal plane comprising charge-coupled devices and fiber optics", Optical Engineering, Sep 1987, Vol.26, No.9, P.897.

Figure 1

Chip Layout

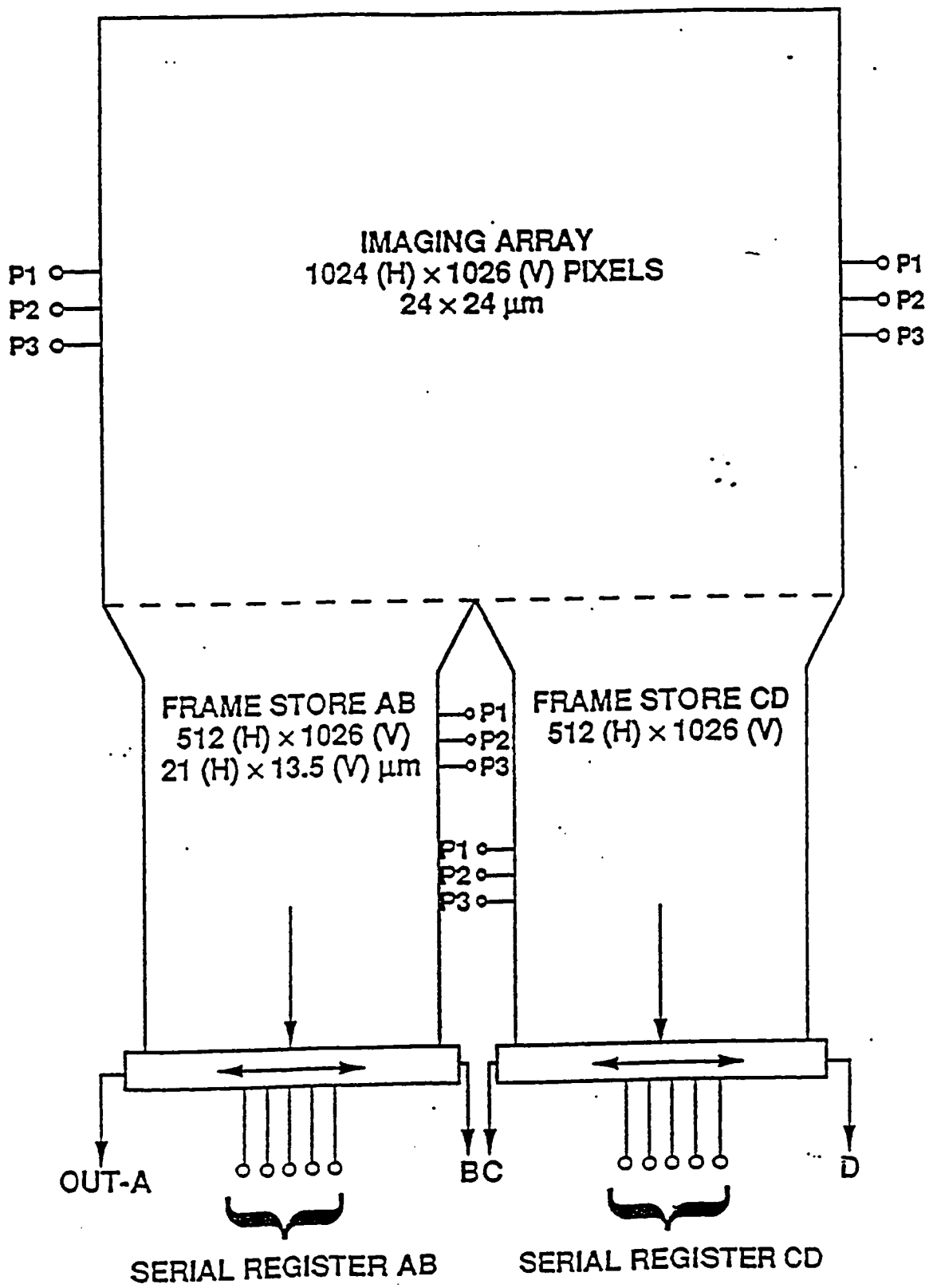
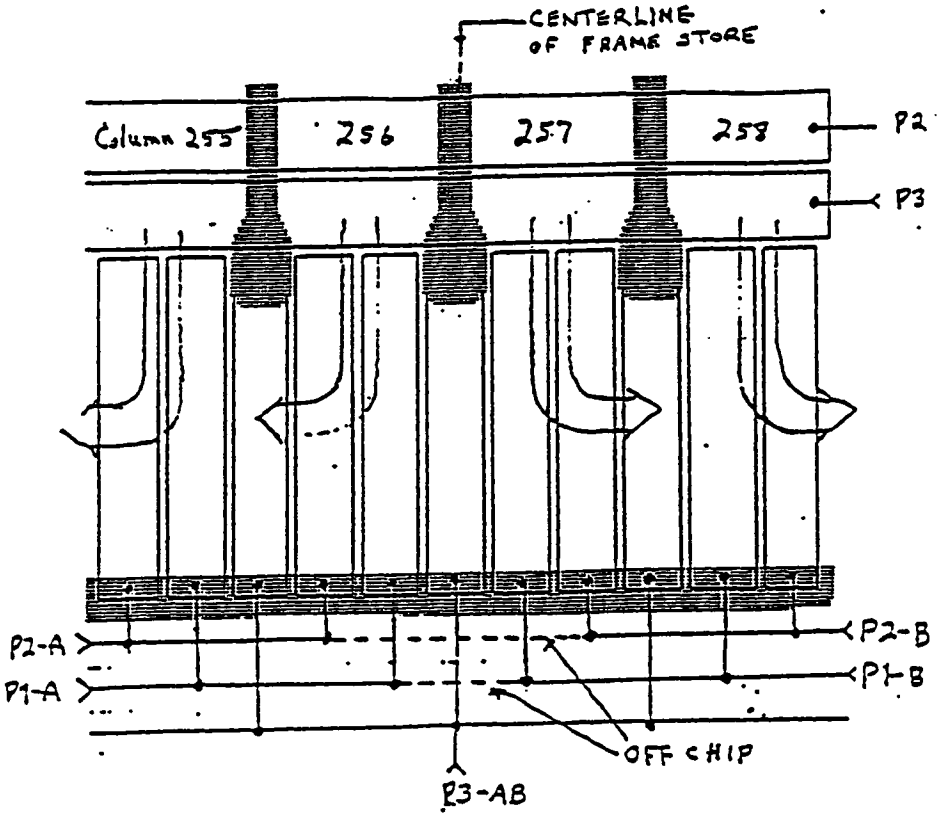
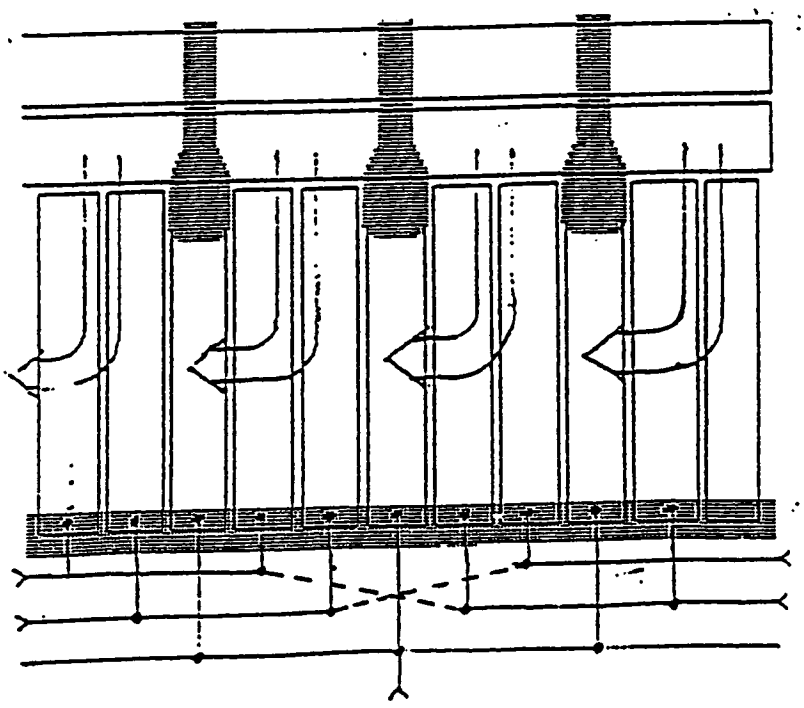


Figure 2

Register Design



a. BI-DIRECTIONAL (2-PORT)



b. UNI-DIRECTIONAL (1-PORT)

Figure 3

Gate Arrangement

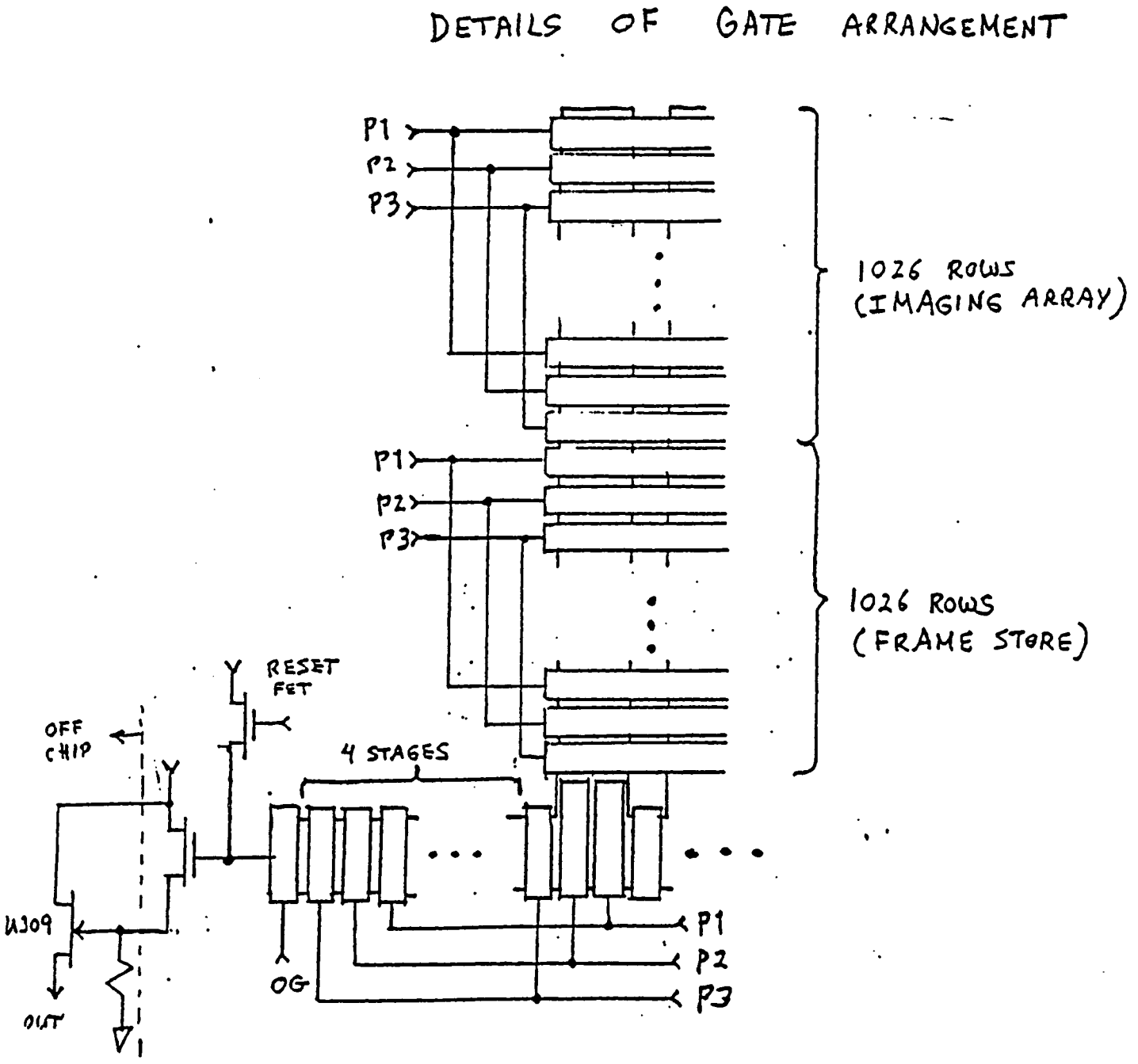


Figure 4

Packaging

TBR

Table 1

Pin Out Arrangement

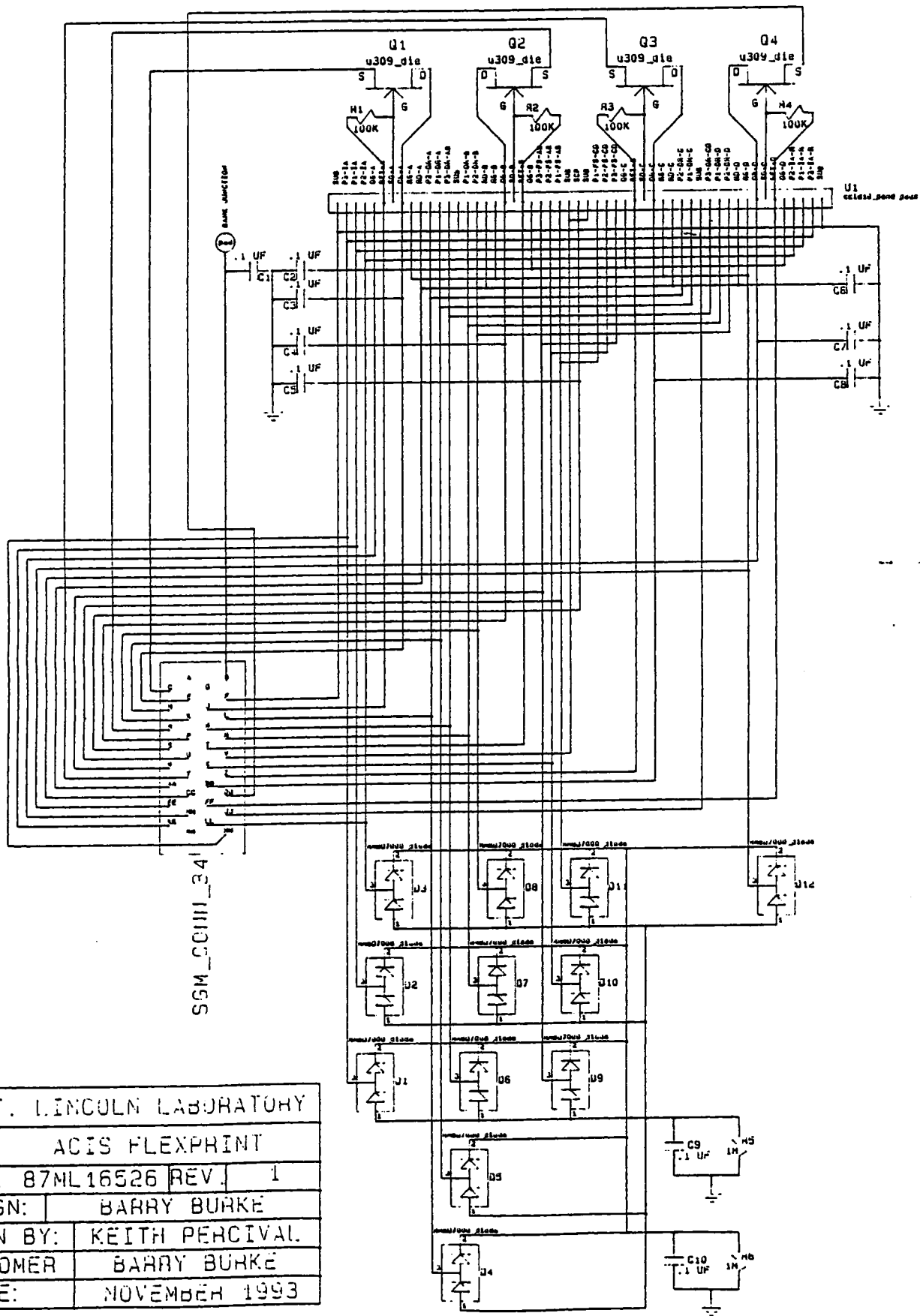
ACIS FLEXPRINT CONNECTIONS FOR CCID-10/10L

5/19/94

Device Pads: Mnemonic	**Function**	**34-Pin Positronics Connector:** Mnemonic	Pin Letter
P1/IA-L, -R	Phase-1 imaging array	P1/IA	KK
P2/IA-L, -R	Phase-2 imaging array	P2/IA	LL
P3/IA-L, -R	Phase-3 imaging array	P3/IA	NN
P1/FS-AB, -CD	Phase-1 frame store	P1/FS	U
P2/FS-AB, -CD	Phase-2 frame store	P2/FS	X
P3/FS-AB, -CD	Phase-3 frame store	P3/FS	W
P1/OR-A, -C	Phase-1 output registers A & C	P1/OR-AC	H
P1/OR-B, -D	Phase-1 output registers B & D	P1/OR-BD	R
P2/OR-A, -C	Phase-2 output registers A & C	P2/OR-AC	L
P2/OR-B, -D	Phase-2 output registers B & D	P2/OR-BD	K
P3/OR-AB, -CD	Phase-3 output registers A-D	P3/OR-ABCD	N
OG-A, -B, -C, -D	Output gates A, B, C, D	OG-ABCD	HH
RG-A, -B, -C, -D	Reset gates A, B, C, D	RG-ABCD	CC
RD-A, -B, -C, -D	Reset diodes A, B, C, D	RD-ABCD	AA
SCP	Scupper (charge collection diode)	SCP	S
DR-A	Drain-A	DR-A	E
DR-B	Drain-B	DR-B	P
DR-C	Drain-C	DR-C	BB
DR-D	Drain-D	DR-D	EE
SO-A	Source-A		
SO-B	Source-B		
SO-C	Source-C		
SO-D	Source-D		
	Video output-A	OUT-A	C
	Video output-B	OUT-B	M
	Video output-C	OUT-C	Y
	Video output-D	OUT-D	DD
RET-A	Video return-A	RET-A	J
RET-B	Video return-B	RET-B	T
RET-C	Video return-C	RET-C	Z
RET-D	Video return-D	RET-D	FF
SUB (6)	Chip substrates	SUB	V, F, JJ
BJ	Back junction	BJ	B

Figure 5

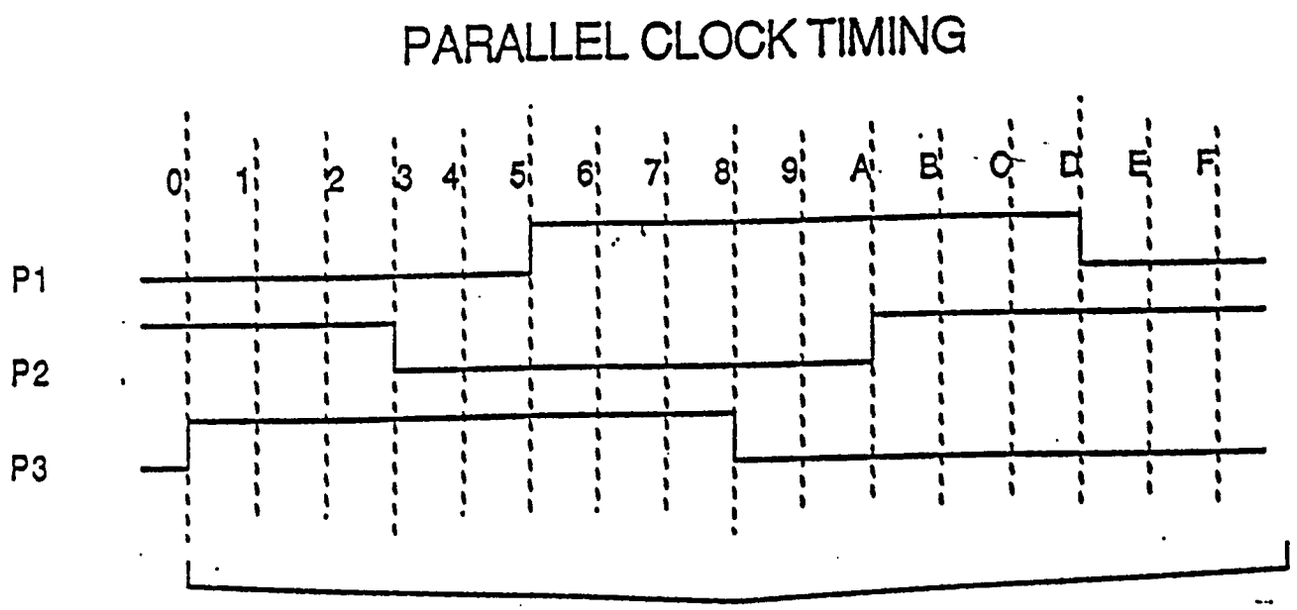
Flexprint Schematic



M.I.T. LINCOLN LABORATORY			
TITLE	ACIS FLEXPRINT		
NO.	87ML16526	REV.	1
DESIGN:	BARRY BURKE		
DRAWN BY:	KEITH PERCIVAL		
CUSTOMER	BARRY BURKE		
DATE:	NOVEMBER 1993		

Figure 6

Timing 1



DURING FRAME TRANSFER, TRANSFER PERIOD IS 4 MICROSECONDS, 0.25 MICROSECONDS PER INCREMENT AND P1=IP1 AND SP1, P2=IP2 AND SP2, P3=IP3 AND SP3.

DURING READ, TRANSFER PERIOD IS 8 MICROSECONDS, 0.5 MICROSECONDS PER INCREMENT. P1=SP1, P2=SP2, P3=SP3. IP1 AND 1P3 ARE LOW, IP2 IS HIGH.

CLOCK VOLTAGES -6V TO +5.0V

Figure 7

Timing 2

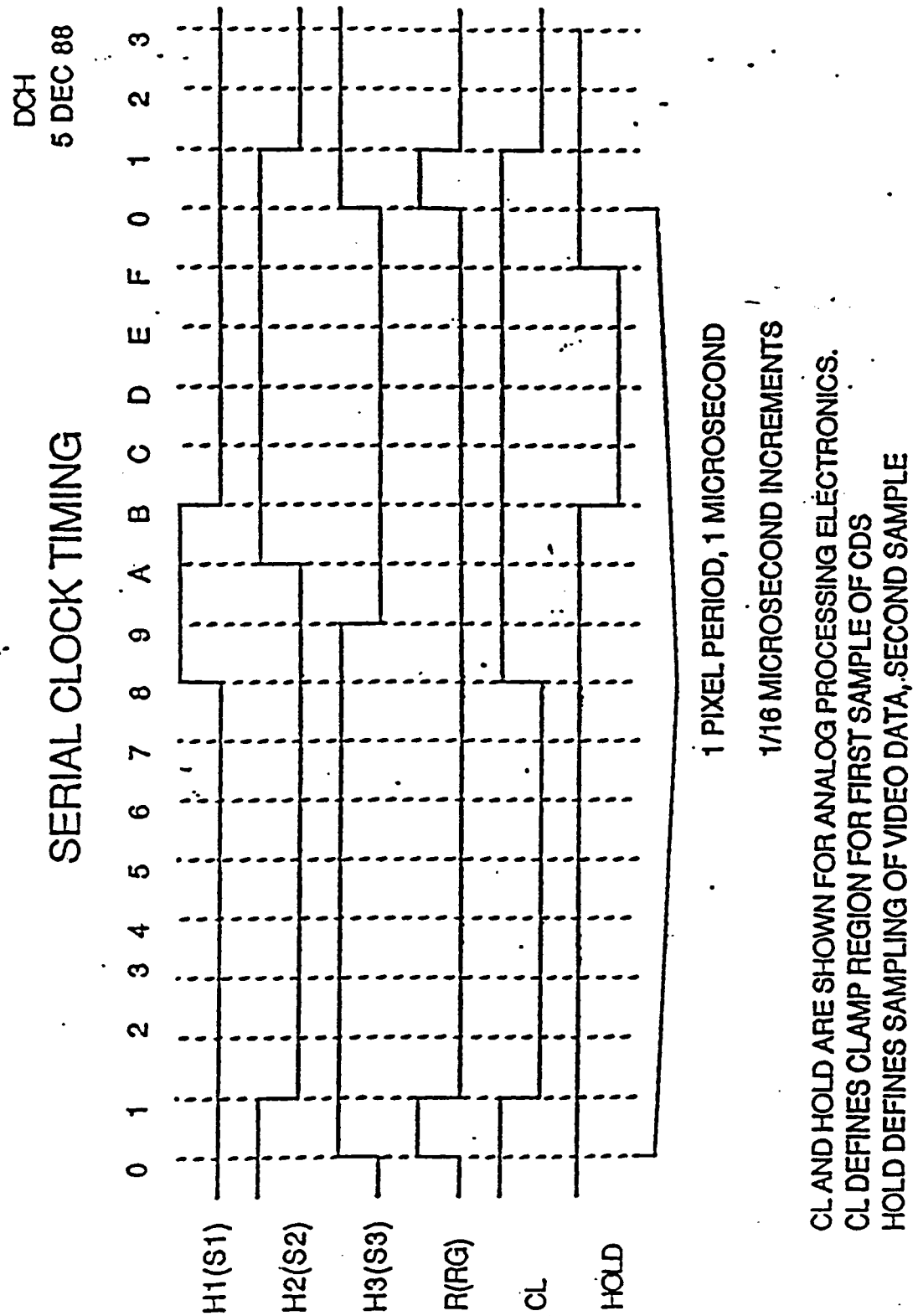


Figure 8

Timing 3

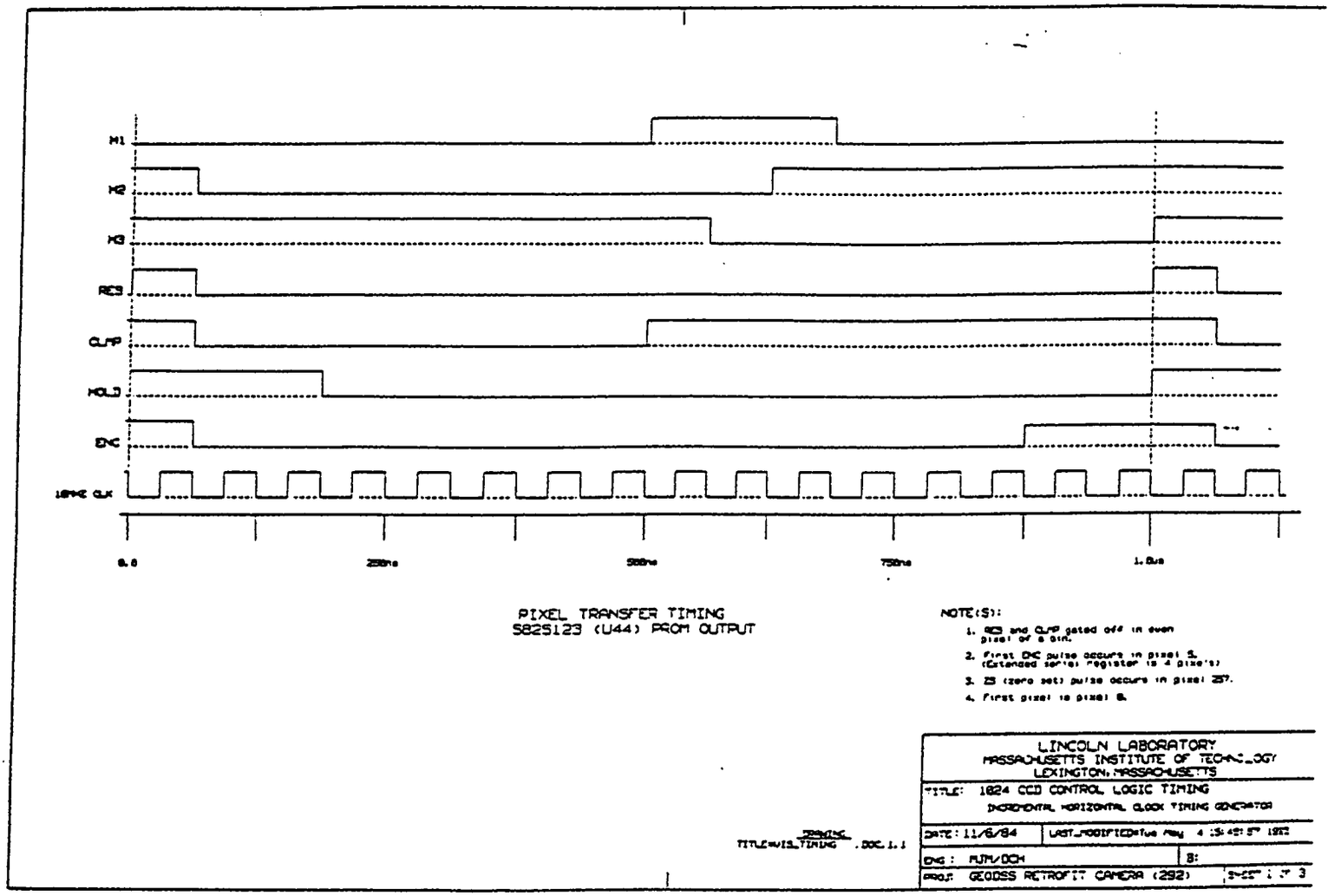


Figure 9

Timing 4

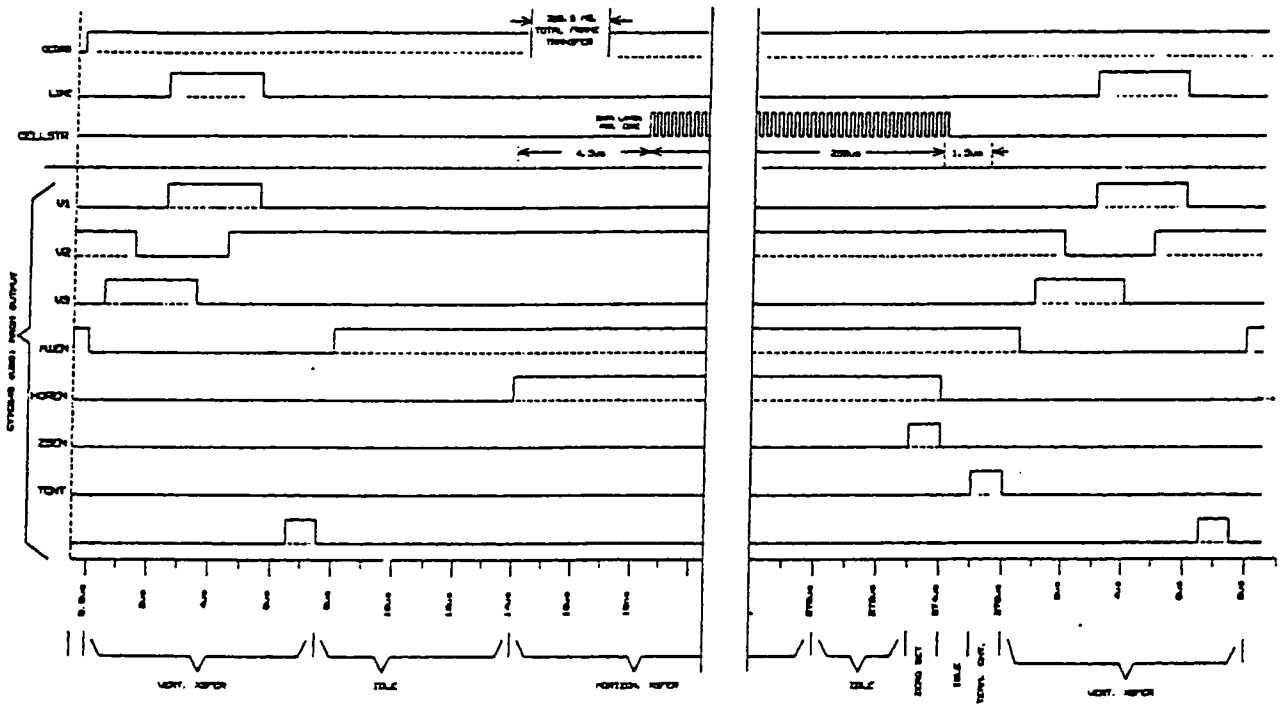


Figure 10

Timing 5