36-01510.031

ACIS Verification Summary Report

Specification:	ACIS Contract End Item Specification
Requirement Number/Title:	3.1.3.2a Event Modes (VRSD 3.1.3.2a-20)

Requirement Statement: Event timing information shall be relatible to the AXAF-I clock with an accuracy of 15 μs of the AXAF-I central clock as defined in paragraph 3.6.3 of the Observatory to Science Instrument ICD. Paragraph 3.6.3 of the Observatory to Science Instrument ICD states that the clock resolution is 1us.

Verification Method:	Measurement and Analysis
Procedure Number:	N/A

Configuration:

Eng Unit DEA and DPA

Cycle Time:

Verification Discussion/Results:

See attached memo.

Dorothy Gordon 17 JUNE '97

ACIS Cognizant Engineer Date

ACIS Timestamping/Counters

The purpose of the ACIS timestamp hardware is to provide knowledge, relative to the AXAF-I timebase, of when an actual CCD exposure has occurred. A 32-bit free-running counter resident on the Digital Processing Assembly (DPA) backend processor (BEP) is cleared only upon power-on reset of the BEP. This counter (BEP Free-Running counter in Figure 1) is clocked by the 100 KHz (TSClk in Figure 1) subdivision of the 38.4 MHz DPA master clock. Its rollover time is ~43Kseconds, approximately 12 hours.

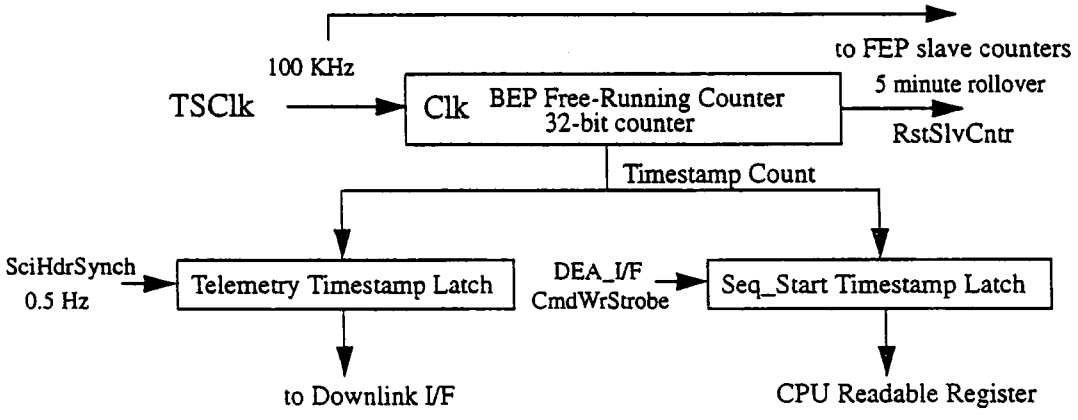

FIGURE 1. BEP Counters/Latches

The Telemetry Timestamp Latch and the Seq_Start Timestamp Latch are both 32 bit registers which are written to by the hardware. The Telemetry Timestamp Latch relates the AXAF-I timebase to the ACIS Free Running Counter via the telemetry stream. The leading edge of the Science Header Synch (received differentially from the S/C IU) generates a latch pulse which transfers the BEP Free Running Count to the Telemetry Timestamp Latch. This 32-bit quantity is then shifted out by the BEP as the first four bytes in the science telemetry following the reception of a Science Header Synch.

The Seq_Start Timestamp Latch is written to every time the BEP sends a command to the DEA I/F. When the BEP CPU initiates a command, the BEP hardware waits for the rising edge of the 100 KHz TSClk (identical to the ADC clock which is sent to the DEA) before shifting out the command. Thus, the DEA sequencing starts deterministically within the 10 μsec period. At the instant (following the rising edge of TSClk) that the DEA command is sent to the interface, the timestamp count is loaded into the Seq_Start Timestamp Latch. The BEP processor then reads the Seq_Start timestamp latch and uses it to compute the time (to within approximately 10 μsec) of the first CCD integration.

The BEP Free Running Counter broadcasts a reset pulse to all the Slave Timestamp Counters resident on the FEPs.The FEP slave counters (20 bits each), loaded into FEP resident latches upon receipt of a beginning of frame synch (BOF) from the DEA, are used to further verify frame onsets and deltas.

The accuracy of the relation of the AXAF-I clock depends on:

1. The predictable arrival of the Science Header Synch at the DPA interface, and consistent synchronization: The edge rates of the differential pulses are specified as less than or equal to 100 nanoseconds (Observatory to Science Instrument ICD, 5/2/1997). The cable delay and skew are not specified, but probably do not significantly affect timing on the order of microseconds. (Delay is a constant we should know; skew is probably trivial.) Synchronization jitter in the BEP also adds another 100 nanoseconds of imprecision.
2. The consistent alignment of the Science Header pulse with respect to the AXAF-I clock: The pulse is specified as 62.5 μseconds with an error of 10 μseconds. If the leading edge is aligned, and the error only accumulates at the trailing edge, ACIS maintains its accurate alignment to AXAF-I clock. However, if the arrival of the Science Header synch varies by 10 μseconds, ACIS can fall out of alignment with the AXAF-I clock by approximately 20 μseconds,
3. The accuracy of the ACIS free-running clock: The frequency stability over a military temperature range of the ACIS oscillator is specified as 65 ppm initially and 100 ppm at the end of life. Since ACIS transmits the timestamp every 2 seconds, relating its count to the more accurate AXAF-I oscillator, the accumulated drift is not significant.
4. The consistency of the DEA sequencer activation following a Start Sequencer command as issued by the BEP: This quantity was measured in the lab, using a DEA and DPA running the flight software. The time between the onset of a start sequencer command and the actual startup of the sequencer was repeatedly (~25 instances) measured and found to be 21.5 μseconds without significant variation. Thus the Seq_Start Timestamp Latch directly and accurately relates to DEA sequencer timing. (See Figure 2, the logic analyzer measurement of Sequencer Startup Time.)

Adding up internal ACIS errors, total accrued inaccuracy in the ACIS instrument is approximately 10.2 μseconds. Adding the error due to placement and transmission of the Science Header pulse may bring the total inaccuracy slightly above 20 μseconds. More information is needed on the edge alignment of the Science Header pulse in order to determine whether the ACIS clock is relatable to AXAF-I clock below 20 μseconds, and to the stated 15 μsecond goal.

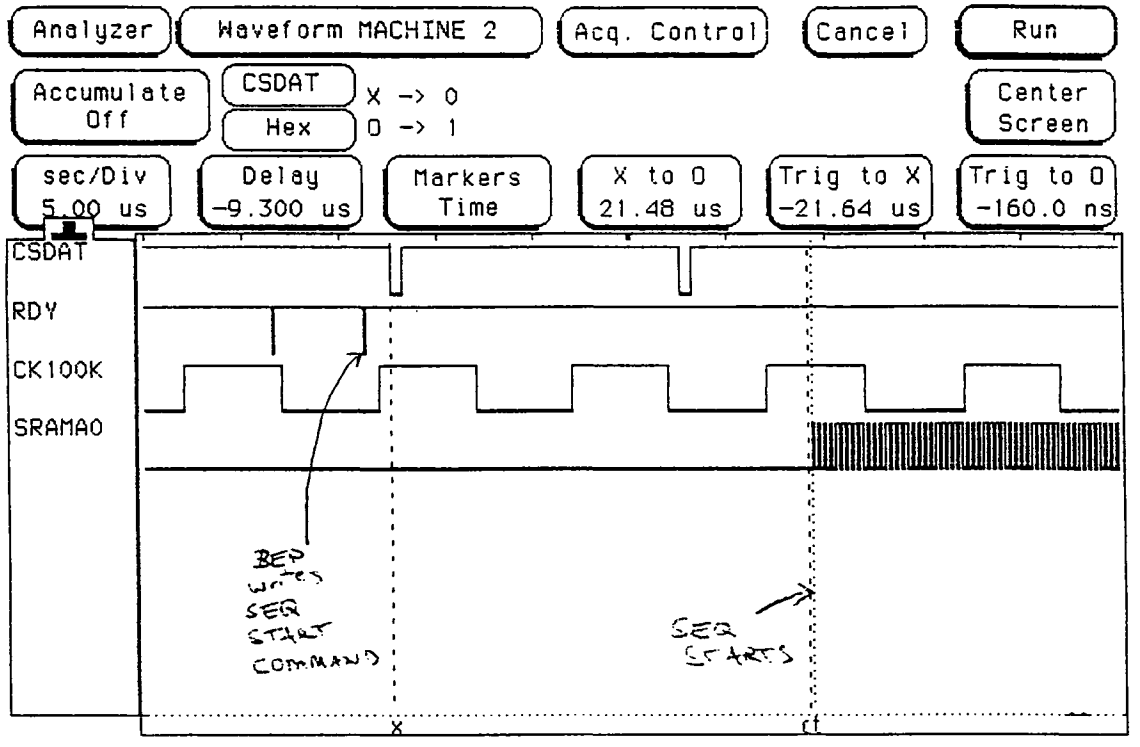

Figure 2: Sequencer Start-up
Timing Measurement

Lavoie, Tony
From: Lavoie, Tony
Sent: Thursday, July 24, 1997 2:54 PM
To: 'ACIS - Goeke, Bob'; 'ACIS - Mayer, Bill'
Cc: Lavoie, Tony; Reed, Ken
Subject: FW: Accuracy of Science Header Pulse to AXAF-I clock

Looks like you meet spec after all.....Bill, please pass to Dorothy Gordon. I assume that this reduces the uncertainty to 10.2 microsec plus, say, 1 microsec for error between sync leading edge and AXAF-I clock, which gets us under the spec.
You can confirm with E-Mail and if it is OK, I'll xerox the E-Mail and put it in our file and close it.

Tony

From: Robbie James[SMTP:rjames@gordata.com]
Sent: Thursday, July 24, 1997 2:40 PM
To: Lavoie, Tony; Thomas, Leann; mike.roderick@trw.com
Subject: Accuracy of Science Header Pulse to AXAF-I clock

======== Original Message ========
Mike or Robbie or Mike or Leann (you can tell that I don't know really who to ask),

I'm reviewing the ACIS verification that requires them to relate their timer to the AXAF-I clock to some accuracy (15 microsec). To do this, they operate off of the Science Header sync pulse, defined in the SI ICD on page 103, Table 3.6.5-7. My question is, does the signal duration variability (+10, -0 microsec) defined for that sync pulse in the table imply that the leading edge of the pulse may have up to 10 microsec of inaccuracy in relation to the AXAF-I clock or does it mean that that the trailing edge may be up to 10 microsec later than nominal, but that the leading edge is always known with respect to the AXAF-I clock to better than a microsec?

The answer makes a big difference as to whether or not ACIS meets its requirement.

Thanks,

Tony
======== Fwd by: Robbie James ========
The leading edge of the SHSP from the IU is known to the AXAF-I clock to better than 1 microsecond. The trailing edge can vary due to a transistor turn-off time in the circuit path from the CTU to the IU.

OPTIONAL FORM 99 (7-90)

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To Bill Mayer	From Tony Lavoie
Dept./Agency	Phone #
Fax #	Fax #

NSN 7540-01-317-7368 5099-101 GENERAL SERVICES ADMINISTRATION

Date: Thu, 24 Jul 97 16:59:41
From: wfm (William Mayer)
To: Anthony.R.Lavoie@msfc.nasa.gov
X-UIDL: 869778436.004

Tony,

Your reading of the verification report is correct. We (ACIS) identified about 10.2 microsec of uncertainty on our side of the interface, but we didn't know how much to add for TRW. According to Dorothy, if they have less than a microsec of uncertainty, then the overall answer is less than 11.2 microsec and we meet the specification of 15 microsec.

Thanks for your help.

Bill