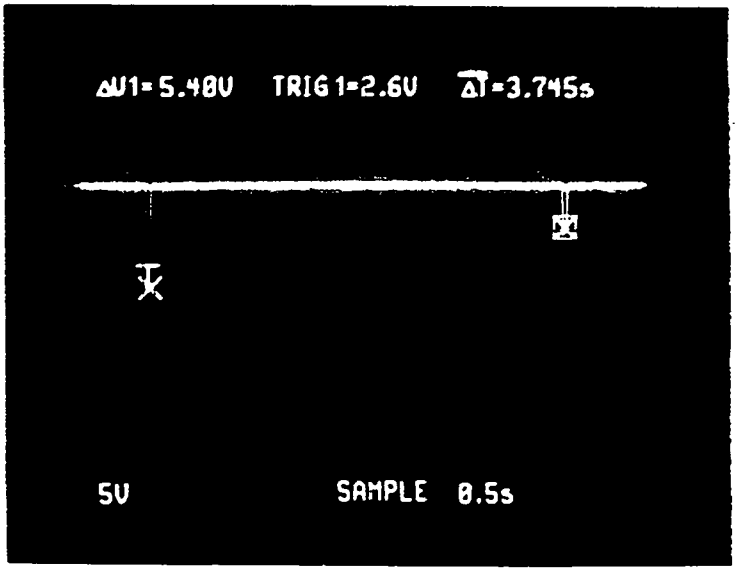
36-01510.005

ACIS Verification Summary Report

Specification:	ACIS Contract End Item Specification
Requirement Number/Title:	3.1.3.1a Timed Exposure Mode (VRSD 3.1.3.1a-3)
Requirement Statement: ACIS shall be capable of reading out the framestore in less than 6.5 sec.	
Verification Method:	Timing analysis by observing parallel clock waveform osc. trace.
Procedure Number:	
Configuration:	Single event trigger on osc.. probe is tied to video card; parallel clock outputs, time scale to 0.5 seconds. Cursors mark the time difference of the parallel clock bursts. Period between clock bursts is indicated on the upper right hand corner of photo shown below.
Cycle Time:	

Verification Discussion/Results:

Clearly, the period between bursts is ~ 3.7 seconds. The PRAM timing parameters used is programmed for ~3.7 second frames.



Gordon C. Garmire — May 20-97

ACIS Cognizant Engineer — Date