36-01510.004

ACIS Verification Summary Report

Specification:	ACIS Contract End Item Specification
Requirement Number/Title:	3.1.3.1a Timed Exposure Mode (VRSD 3.1.3.1a-2)

Requirement Statement: The imaging-to-framestore operation shall be executed in no more than 60 msec.

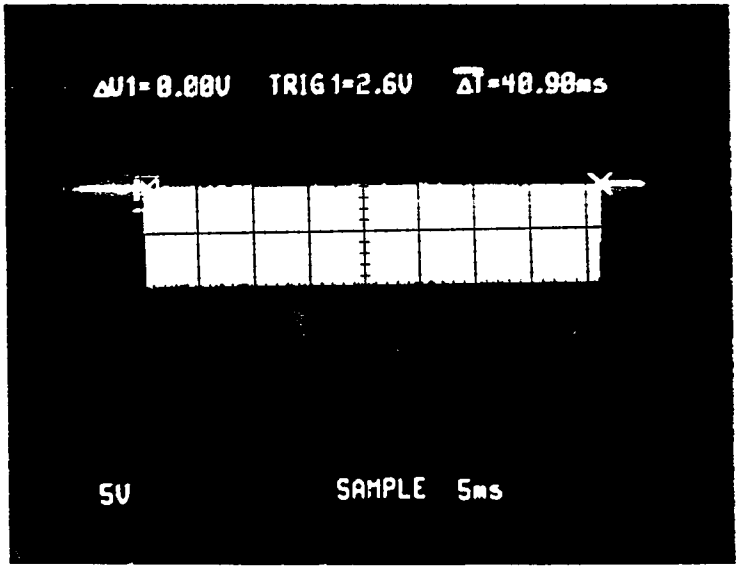
Verification Method:	Timing analysis by observing parallel clock waveform osc. trace.
Procedure Number:	

Configuration: Single event trigger on osc., probe is tied to video card, parallel clock output. Cursors mark the beginning and the ending of a clock burst. Time between bursts is indicated on the upper right-hand corner of the photo shown below.

Cycle Time:

Verification Discussion/Results:

Clearly, the burst time indicated is ~40 ms. The SRAM/PRAM timing parameters were programmed for 40 ms and is flight configuration.



ACIS Cognizant Engineer — Date: May 20-97