Triana Faraday Cup
Interface Control Document

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Rev. 12

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Contents

Preface

Revision 01 tries to enumerate the interfaces between MIT and the GSFC Science Group on Triana. It does not include a door.

Revision 02 modifies the instrument command interface to use an implicit run command upon loading of HV steps. The software interface(s) are also initially defined.

Revision 03 changed the serial interface to a standard RS232 protocol (with 422 hardware).

Revision 04 changed the serial interface to a synchronous, single-ended design. It also specified some boundary behavior of the controlling software.

Revision 05 introduced many comments from the science community and fixed the command and telemetry diagrams to show (properly) the 600KHz shift clock.

Revision 06 added the High Voltage Modulator interface as well as specifying pinouts for connections from the digital board to both DPU and Modulator. It also added the ServiceTime variable to extend the length of an measurement interval.

Revision 07 put the Status bit onto the DPU interface connector and refined the state of the instrument at the end of an observation as well as in the presence of a general reset.

Revision 08 changed the pinouts on the DPU interface connector(s) and specified the analog housekeeping thermistors.

Revision 09 reflects several changes made by GSFC: wiring to interface connectors and the use of an 'HCS32 instead of an 'HCS125. We also added a software command to change the time delay between the reference and the delayed 200Hz clock used by the demodulator. It also includes new pin outs for the power connector.

Revision 10 fixed a logic inconsistency in 4.3.4 . It also includes new pin outs for the modulator connector.

Revision 11 clarifies use of the Calibration Directive.

Revision 12 changed the master clock frequency at Goddard's request. More importantly it adds some limitations upon the timing of the first and second pair of modulator voltage commands sent while starting an observation sequence.

1 Introduction

1.1 Program Overview

MIT is designing and fabricating a Faraday Cup (FC) for use in measuring components of the solar wind; this cup is intended to be similar, but not identical, to that flown on the WIND mission. MIT is also providing engineering support for the associated electronics: three analog measurement chains -- intended to be identical to those flown on WIND -- and a digital board which will require some modification from the original WIND design. A High Voltage Modulator supply -- which is supplied by GSFC -- provides a time-varying voltage to the Faraday Cup.

On WIND a second digital board sat between the Faraday Cup digital board and the Digital Processing Unit (DPU), referred to as a DPUii (DPU Instrument Interface). This board communicated with the DPU *via* an RS422 interface for both commands and telemetry, received and distributed clock signals from the DPU and formatted commands for use by the high voltage modulator. These functions will be incorporated into the primary/sole digital board.

1.2 Experiment Overview

The FC operates by applying a sequence of 200 Hz, biased square wave voltages to a grid within the cup in order to determine the energy/charge of the entering particles. The upper and lower voltage pair which forms the square wave is called a "voltage window".

The resulting 200-Hz-modulated fluxes produce currents into three, 120-degree sectors of the circular collector plate at the rear of the cup. The currents are AC coupled to three independent analog measurement chains, one for each collector sector. The currents are amplified, synchronously detected, and integrated. At the end of the "integration period", the voltage on an integrating capacitor is logarithmically converted to a digital signal.

The integration period is a multiple of the 5 millisecond period of the modulator signal. Additional 5 ms periods are allotted for the A/D conversion and for switching the modulator voltages to a new set of upper and lower voltage levels. The resulting total time is called a "Measurement Interval".

The voltage windows necessary to cover the energy/charge range of the incoming particles are set by a fixed table or by tracking the peak signal current observed.

A "Measurement Cycle" consists of a sequence of Measurement Intervals using a set of increasing Voltage Windows including those additional measurement intervals which allow the modulator to settle at its initial window.

We define an "Observation" to be a continuous set of Measurement Cycles which normally are only interrupted to change voltage windows, do a calibration exercise, *etc*.

2 Reference Documents

(none)

3 Electrical Interfaces

3.1 Supply Voltages

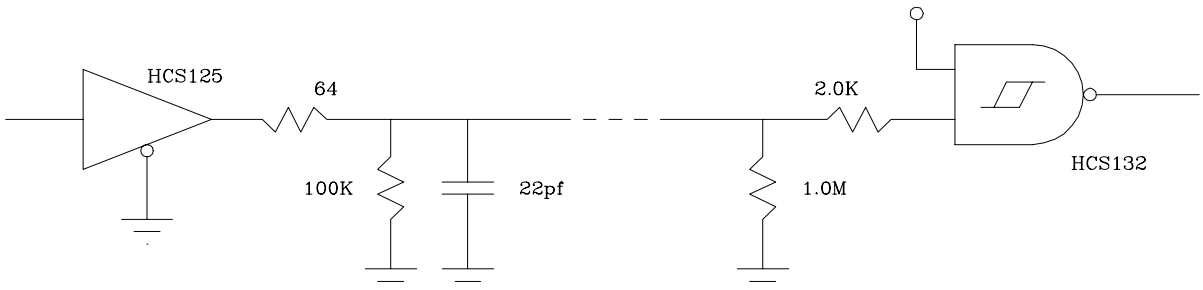
The voltages received from the DPU for operation of the complete instrument are

Voltage	Tolerance	Typical Current	Maximum Current
+5VDC	± 5%	30 ma	50 ma
+12.8VDC		90 ma	120 ma
-12.8VDC		90 ma	120 ma
28VDC	± 4VDC	36 - 135 ma	160 ma

Note that the 28VDC is simply passed through to the High Voltage Modulator.

3.2 Drivers and Receivers

All signal interfaces are implemented as single-ended HCS125 drivers and HCS132 Schmitt receivers, both between DPU and the digital board and between the Modulator and the digital board.



3.3 DPU to FC Signal Interfaces

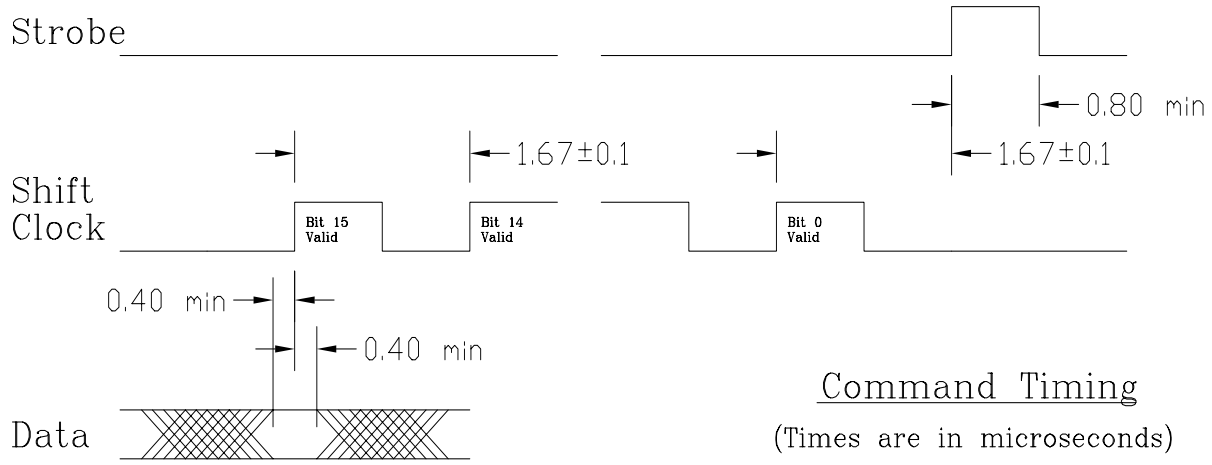
3.3.1 Clock from DPU

614.4KHz, tolerance unknown

Note that all of the timing shown in this document assumes the original 600KHz clock. Since all of the internal timing is derived from this clock, everything is now running a bit faster; e.g. the 200Hz modulation clock is now really 204.8Hz.

3.3.2 Commands from DPU

All 16-bit command words are delivered MSB first. Sending one or more NULL words in a row will result in resetting the entire FC Instrument.

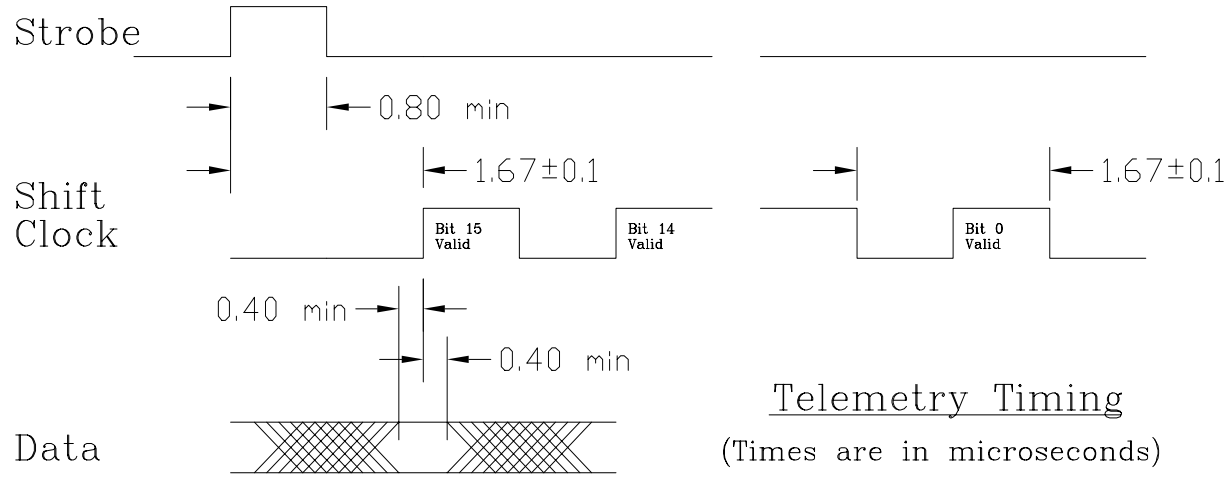


On each rising edge of the shift clock, the FC Instrument reads a data value into a shift register; on the trailing edge of the shift clock the DPU updates the data. After 16 clock pulses a strobe pulse validates completion of the command and is used to latch the full command word into the instrument. A value of +5volts is defined to be a Logical One.Status from FC

A single bit is delivered as the __STATUS__ signal by the FC Instrument to the DPU. A value of +5volts is defined as READY; a value of 0volts is defined as NOTREADY.

3.3.3 Telemetry from FC

All 16-bit data words are delivered MSB first on a serial interface..



The read strobe tells the FC Instrument to latch the 16-bit telemetry word into a shift register. On the rising edge of each clock pulse the DPU reads the next bit, and on each trailing edge the FC advances the next bit in the register to the output node. A value of +5volts is defined to be a Logical One.

3.3.4 Serial Command and Data Timing

The command and telemetry serial interfaces run at 600KHz.

The __STATUS__ bit will indicate NOTREADY upon receipt of a _ModulatorHigh_ command and indicates that the FC is busy. The bit indicates READY when telemetry data are available from the previous integration interval, within 1 millisecond of the start of the following interval. As a result the DPU has

(IntegrationTime * 5 - 1) milliseconds

to read the 3 telemetry words and send (typically 2) command words; the DPU may handle the command and telemetry functions in any time order or in parallel.

3.3.5 Analog Housekeeping

Each of the following are available to the DPU for sampling on an infrequent basis.

Quantity	Type
FC Outer Cup Temp	Thermistor 2.25K@25C || 4.7K
FC Enclosure Temp.	
Modulator Voltage A	Voltage monitor
Modulator Voltage B	
Suppressor Grid Voltage	

3.3.6 Physical Connections

The actual pinouts used for signals and power are given in Appendix A.

3.4 Digital Board to Modulator Signal Interfaces

3.4.1 Parallel Command Word

A six bit command word is presented in parallel on the interface by the digital board, positive logic, so that 0x3F requests a maximum voltage output, 0x00 a minimum voltage.

A single line is used to load the command word into the HV Modulator. Although often incorrectly referred to as a 200Hz clock, the interface does not require any particular duty cycle as only the rising and falling edges of this signal are used to load the parallel command word into the Modulator. During any one measurement interval two parallel command words will be presented on the interface. The higher value will be available for loading on the rising edge of the 200Hz Load Signal, and the lower value will be available for loading on the falling edge of the 200Hz Load Signal.

The timing relationships of this interface may be seen in the overall system timing diagram given in Appendix E; the 200Hz Load Signal is labeled as "U200" in that diagram.

3.4.2 Modulator On

This single bit enables the Modulator's high voltage supply; the suppressor voltage is present, however, whenever the 28VDC main power is available.

4 Software Interfaces

4.1 Command Definition

4.1.1 Interface Command Word Format

Each command from the DPU to the FC Instrument consists of an 8 bit directive in the most significant byte and an 8 bit argument in the least significant byte. The following table defines, for each directive, the legal range of values which the argument can take.

Directive	Name	Unit Conversion	Valid Arguments
0x00	_GeneralReset_	NULL	0x00
0x01	_ModulatorHigh_	volts = 150 * $e^{N*0.0631}$	0 - 63
0x02	_ModulatorLow_		
0x10	_ModulatorOn_	1 =: On	0 - 1
0x04	_IntegrationTime_	Time (ms) = N * 5	1 - 63
0x08	_ServiceTime_	Time (ms) = N * 5	1 - 15
0x40	_ClockDelay_	Time (μs) = N * 6.7	0 - 63
0x80	_Calibration_	(see table below)	0 - 255

(Real numbers for the modulator voltages are given in Appendix D .)

4.1.2 Uplink Command Structure

The command structure which is sent to the DPU for control of the FC Instrument is defined as follows:

Name	Legal Values	Description
ModulatorVoltage[]	0 - 63.	A monotonically increasing set of values through which the HV modulator will step. The array may have any number of valid entries between 2 and 64. If fewer than 64, the end of valid entries is indicated by a value of 0xFF.
ModulatorOn	0 - 1	Enables the HV Modulator to turn on (the suppressor grid voltage is always on).
RetraceIntervals	0 - 7	The number of measurement intervals which will be allowed for the HV Modulator to return to its starting, low value.
IntegrationTime	1 - 63	The number of 5ms intervals during which the FC signal will be integrated.
ServiceTime	1 - 15	The number of 5ms intervals which the instrument will insert between integrations.
ClockDelay	0 - 63	The number of 6.7μs intervals by which the demodulator clock is delayed from the 200Hz clock sent to the HV Modulator.
Calibration	0 - 255	Defines the magnitude and application of calibration currents in the FC analog electronics.
PeakOffsetHigh	1 - 31	Defines how many voltage steps above the calculated peak the scan should terminate.
PeakOffsetLow	1 - 31	Defines how many voltage steps below the calculated peak the scan should start.
PeakRepeatCount	0 - 4095	Defines how many times the peak scan should be repeated before a new full scan should be made.
PeakCurrentMin	0 - 4094	Defines a value which a peak current must exceed to be valid; a value of 4095 inhibits incremental tracking.
RunHalt	0 - 1	When set to "1" start the Observation. When set to "0" complete the current measurement cycle and terminate (executed upon receipt).

4.1.3 Word Format for Calibration Directive

Calibration directives are subdivided into fields; we define bit 7 to be the MSB of the argument. The measurement chains into which current is injected is selected by Bits 7 and 6. Bit 5 controls the modulation of the injected current; the magnitude of the current injected is that selected by Bit 3 times the power of 10 selected by Bits 2 - 0 (in amperes).

Bit Field	Function	Coding
7 - 6	Chain Select	0 =: apply to all 1 =: only chain A 2 =: only chain B 3 =: only chain C
5	Modulation	1 =: On, 0 =: Off
4	(not used)	
3	Multiplier	1 =: 10x, 0 =: 3x
2 - 0	Exponent	0 =: Current Off 1 =: -14 2 =: -13 3 =: -12 4 =: -11 5 =: -10 6 =: -9

Internally the lowest 4 bits are distributed in parallel to all three chains when written to Chain A (or "all"), but the Modulation command is distributed separately. To command only Chain B to be active, therefore, one might send a command "apply to all"&"Modulation off"&"magnitude bits" first, and then send a command "only Chain B"&"Modulation on"&"magnitude bits".

4.2 Telemetry Definition

Each telemetry word starts with 2 bits of identification; ID 0 echoes the instrument state and is generated by the DPU as it sets up the measurement cycle.

ID Bits 15-14	Bits 13-6	Bits 5-0
0	_Calibration_	_ModulatorLow_

ID 1-3 returns the measured data as received from the FC. Four telemetry words are thus generated for each Integration Time interval.

Bit Field	Function	Coding
15 - 14	Collector	1 =: Chain A 2 =: Chain B 3 =: Chain C
13	HV Modulation	1 =: On
12	(unused)	
11 - 10	MUX Range	0 =: Minimum Signal
9 - 0	A/D Value	0 =: Minimum Signal

4.3 Setup and Logical Data Flow

4.3.1 Initialization

At the start of an observing run, the DPU receives from its uplink a set of commands described above: `ModulatorVoltage[]`, `ModulatorOn`, `RetraceIntervals`, `IntegrationTime`, `ServiceTime`, `ClockDelay`, `Calibration`, `PeakOffsetHigh`, `PeakOffsetLow`, and `PeakRepeatCount`. It is a function of the DPU software as to whether it will insist upon receiving values for each of these commands, or will use a default value of 0x00 for any uninitialized values.

It would probably be good practice for the DPU to send the FC Instrument a `_GeneralReset_` command to clear all internal registers before starting a new observation. The DPU also needs to deal intelligently with the receipt of a new set of commands while a current observation is underway. It is required that observation parameters not change while the FC Instrument is taking data, but the protocol for accomplishing this is completely within the control of the DPU software engineer.

4.3.2 Measurement Intervals

The FC Instrument operates by doing a synchronous demodulation of the solar wind signal for a period of time equal to the value of `IntegrationTime` * 5ms followed by an additional service interval of `ServiceTime` * 5ms during which the HV Modulator is primed for the next measurement and the A/D converters do their work. For (typical) values of `IntegrationTime = 6` and `ServiceTime = 2`, therefore, a single instrument measurement cycle is 40ms. The values the DPU sends to the instrument for `_IntegrationTime_` and `_ServiceTime_` are identical to those received from the uplink as `IntegrationTime` and `ServiceTime`, respectively.

4.3.3 Modulator Voltage Settings

The DPU must send, for each measurement interval, a value for _ModulatorLow_ and _ModulatorHigh_. The first two values sent are `ModulatorVoltage[0]` for _ModulatorLow_ and `ModulatorVoltage[1]` for _ModulatorHigh_. If `RetraceInterval` has a value `r`, then for the next `r` cycles the DPU sends the identical values again. The DPU then steps up the array and sends `ModulatorVoltage[1]` and `ModulatorVoltage[2]`. This continues until the end of the array -- indicated by a content of 0xFF or an array index >63. What happens then depends upon the science mode (described below).

4.3.4 Command Flow

Initially the DPU sends _Calibration_ , _IntegrationTime_ , _ServiceTime_, and _ModulatorOn_ to set up the FC instrument. The commands _ModulatorLow_ and _ModulatorHigh_ must be sent last, however, and in that order. As soon as the instrument receives _ModulatorHigh_ the instrument starts an initialization cycle which, depending upon the phase of internal clocks, will last between 5 and 10ms. The actual measurement interval then starts and lasts the commanded duration. The Status bit was initially NOTREADY -- indicating it is has no data available, and will stay that way until the end of the service intervals. Note especially that the _ModulatorOn_ command does not take effect until the beginning of the first measurement interval; this prevents the Modulator from being turned on with an unspecified voltage command.

When a sequence is started, the second pair of _ModulatorLow_ and _ModulatorHigh_ commands, which will be used for the second measurement interval, must be sent after the the completion of the initialization cycle (guaranteed to be less than 10ms after receipt of the first _ModulatorHigh_ command) and before the end of the commanded integration interval. Following the first measurement cycle the Status bit will go READY. At this point the next _ModulatorLow_ and _ModulatorHigh_ may be sent, with no delay if desired, but at least before the end of the current integration interval. The high voltage values are forwarded to the modulator at the beginning of the service interval so that stability may be reached prior to the start of the next integration interval.

If the DPU fails to update the voltage settings during a measurement interval, the FC instrument will halt at the end of the service interval and the HV Modulator will be set to its minimum voltage (but not disabled). The _Calibration_ , _IntegrationTime_ and _ModulatorOn_ directives will be retained until explicitly commanded to change.

4.3.5 Normal Operating Mode

Normal operation of the FC Instrument involves sweeping the HV Modulator through a series of increasing levels and taking measurements at each level.

At the end of the sweep and retrace interval, the sequence is repeated *ad nauseam*, starting again at the lowest voltage level.

4.3.5.1 Parameter Setup

The normal mode is defined by an array of increasing voltage levels in `ModulatorVoltage[]` -- the number of valid array elements may be between 2 and 64; a command to turn the modulator on -- `ModulatorOn = 1`; an integration count of between 1 and 63, though the normal usage will simply be `IntegrationTime = 6`, and a service time count of between 1 and 15, though the normal usage will simply be `ServiceTime = 2`. Although PeakOffsetHigh and PeakOffsetLow are undefined for this mode, it is necessary that `Calibration = 0x00` and `PeakRepeatCount = 0x00` (whether by command or default).

From a software point of view, the normal mode can be treated as simply a Peak Tracking mode with a Repeat Count of zero, but it was easier to describe this special case by itself first, and the user thinks of it as a separate mode.

4.3.5.2 Retrace Handling

When the HV Modulator is commanded to drop from its highest working voltage to its lowest, a certain amount of settling time is required. To that end `RetraceIntervals` defines the number of times the first pair of values in `ModulatorVoltage[]` should be repeated each time the sweep begins -- typical values are 1 or 2, allowing 35 or 70ms for the modulator to stabilize.

The results of the first measurement cycle in a series will be polluted also by the simultaneous turnon of the HV Modulator with the start of the measurement interval; a `RetraceInterval > 0` will solve this problem, too.

4.3.6 Calibration Mode

From a software point of view, calibration differs not a whit from the normal operating mode. The value for `Calibration` which was uplinked is simply passed along unaltered as _Calibration_ to the FC Instrument prior to initiation of a measurement sequence. It is the ground's responsibility to arrange a sensible combination of bits within this directive. Note from the discussion of 4.1.3 that sending than one _Calibration_ directive is legal, and in some cases required.

4.3.7 Peak Tracking Mode

An initial sweep through the values contained in `ModulatorVoltage[]` is performed in exactly the same manner as described under Normal Mode above; assume that there were K entries in the voltage array. At the end of the sweep, the data channel from the instrument has returned (K-1) triplets of amplitude data. These 3*(K-1) data words are scanned to pick out the algebraically largest value of bits 11 - 0 (MUX plus A/D data) The step in which the largest value is found -- the

index into ModulatorVoltage[] -- is defined to be the peak channel P with associated low and high voltages given by ModulatorVoltage[P] and ModulatorVoltage[P+1] . If PeakCurrentMin < 4095 we require that the largest value found exceed PeakCurrentMin; if not, the answer is considered invalid and the initial sweep is repeated, If PeakCurrentMin = 4095 this test is not performed.

Practical matters: the maximum values can be tracked as the data triplets are received by the DPU so that less work has to be done at the end. We insist, also, that the peak channel not be at the end of the range defined by ModulatorVoltage[] (we always scan at least one interval past the computed peak). Therefore, the peak search can stop one step before the end. This is convenient since the first set of voltage values for the peak scan need to be sent to the instrument before the last measurement interval of the full scan is complete.

Ambiguity resolution: assume that the algorithm starts at the first triplet received -- the minimum voltage level -- and each triplet is scanned for a maximum value before moving on to the next. If the maximum value occurs at more than one voltage level, the last match (the highest voltage level) will be the one used to define the peak channel P.

The DPU now commands PeakRepeatCount consecutive peak sweeps. Let the value of PeakOffsetLow = A and PeakOffsetHigh = B. Then these peak sweeps will run from

```
from    ModulatorVoltage[P-A], ModulatorVoltage[P-A+1]
to      ModulatorVoltage[P+B], ModulatorVoltage[P+B+1].
```

and the use of RetraceIntervals (as described above) applies on every transition from maximum high voltage to minimum high voltage. After each peak sweep, if PeakCurrentMin < 4095, the peak channel is recalculated (as was done initially). If the largest detected current does not exceed PeakCurrentMin , the peak sweeps are immediately terminated. If PeakCurrentMin = 4095 this test is not performed.. In any event, at the conclusion of PeakRepeatCount sweeps, the DPU repeats the entire process, returning to sweep through the entire ModulatorVoltage[] table and calculating a new peak value.

Range adjustment: if the calculated maximum modulator voltage step P+B lies outside the valid range of ModulatorVoltage[], then the maximum voltage step will be set to the last entry in ModulatorVoltage[] and the lower limit will be adjusted accordingly; viz:

```
from    ModulatorVoltage[K-2-(B+A)], ModulatorVoltage[K-1-(B+A)]
to      ModulatorVoltage[K-2], ModulatorVoltage[K-1]
```

The same adjustment ensues if the lower step is calculated to be less than zero; viz:

from `ModulatorVoltage[0], ModulatorVoltage[1]`
to `ModulatorVoltage[B+A], ModulatorVoltage[1+(B+A)]`

4.3.8 Ending an Observation

When the DPU receives a RunHalt = 0 command, it continues sending the _Modulator*_ voltage pairs until the current Measurement Cycle is complete and then stops responding to the __STATUS__ signal. As previously stated the FC electronics will reduce the modulator output voltage to a minimum as soon as a _ModulatorHigh_ command fails to arrive when expected.

A _GeneralReset_ will turn the diable the Modulator in addition to setting its voltage magnitude command to a minimum. _Calibration_ will be set to 0x00, and both _IntegrationTime_ and _ServiceTime_ will be set to a value of 1.

5 Mechanical Interfaces

5.1 Faraday Cup Definition

The Faraday Cup mechanical interfaces are defined by MIT Dwg. 27-40100.

5.2 Analog Board Outline

The analog board outline is defined by MIT Dwg. 27-50101.

5.3 Digital Board Outline

The digital board outline is defined by MIT Dwg. 27-50201.

6 Thermal Interfaces

6.1 Power Dissipation

6.2 Required Temperature Ranges

The following table defines survival and normal operating temperatures.

Assembly	Survival		Operating	
	Minimum	Maximum	Minimum	Maximum
Faraday Cup	-30C	+50C	-20C	+40C
Electronics	-30C	+50C	-10C	+30C

Appendix A
DPU-to-FC Digital Board Pinout

The signal wiring interface is a hole pattern on the digital board which is consistent with a male, high-density D-subminiature connector, GSFC part number 311P4/07-2P-B-12.

Contact	Function	Internal Ties
1	Serial Command Line	
2	Serial Command Strobe	
3	600KHz Clock	
4	Analog -- Electronics Temperature	
5	Analog -- Cup Temperature	
6	5VDC Return	14
7	+5VDC	15
8	+12.8VDC	16
9	-12.8VDC	25
10	Serial Shift Clock	
11	Shield - 5Rtn	18 - 23 - 26
12	FC Status Bit	
13	Analog -- Modulator A	
14	5VDC Return	6
15	+5VDC	7
16	+12.8VDC	8
17	12.8VDC Return	24
18	Shield - 5Rtn	11 - 23 - 26
19	Serial Data Line	
20	Serial Data Strobe	
21	Analog -- Modulator B	
22	Analog -- Modulator Suppressor	
23	Shield - 5Rtn	11 - 18 - 26
24	12.8VDC Return	17
25	-12.8VDC	9
26	Chassis Ground	11 - 18 - 23

For reference, the male connector pattern looks like this:

```
   1   2   3   4   5   6   7   8   9
 10  11  12  13  14  15  16  17  18
   19  20  21  22  23  24  25  26
```

The power wiring interface is a hole pattern on the digital board which is consistent with a standard 9-pin male D-subminiature connector. Unfortunately the interface connector actually supplied has 15 pins, GSFC G311P407-1P.

PC Pattern	Connector	Function	Internal Ties
1		nc	
2	1	+28VDC	3
3	2	+28VDC	2
4		nc	
5		nc	
6	11	28VDC Return	8
7		Chassis Ground	9
8	12	28VDC Return	6
9	13	Chassis Ground	7

For reference, the male connector pattern looks like this:

```
1   2   3   4   5
  6   7   8   9
```

Appendix B
Digital/Analog Interface Bus

The inter-board connections are made with a bussed flat ribbon cable. Pins 1-20 are common to all boards. Each analog board picks up its own signals by jumper selection on the analog board; e.g. board A picks up the signals on pings 29 through 32.

Pin	Function	Pin	Function	
1	K1 - Cal Gain Select	21	n/c	
2	K2	22	n/c	
3	K3	23	D200 - Delayed Clock	
4	K4	24	Hold	
5	K5	25	Dump	
6	K6	26	CHAP	
7	K7	27	n/c	
8	K8 - Cal on/off	28	n/c	
9	U200 - 200Hz Clock	29	RGE1	A
10	n/c	30	RGE2	A
11	n/c	31	CompOut	A
12	n/c	32	ExtCal Input	A
13	+12.8VDC	33	RGE1	B
14		34	RGE2	B
15	Analog Ground	35	CompOut	B
16		36	ExtCal Input	B
17	Digital Ground	37	RGE1	C
18		38	RGE2	C
19	-12.8VDC	39	CompOut	C
20		40	ExtCal Input	C

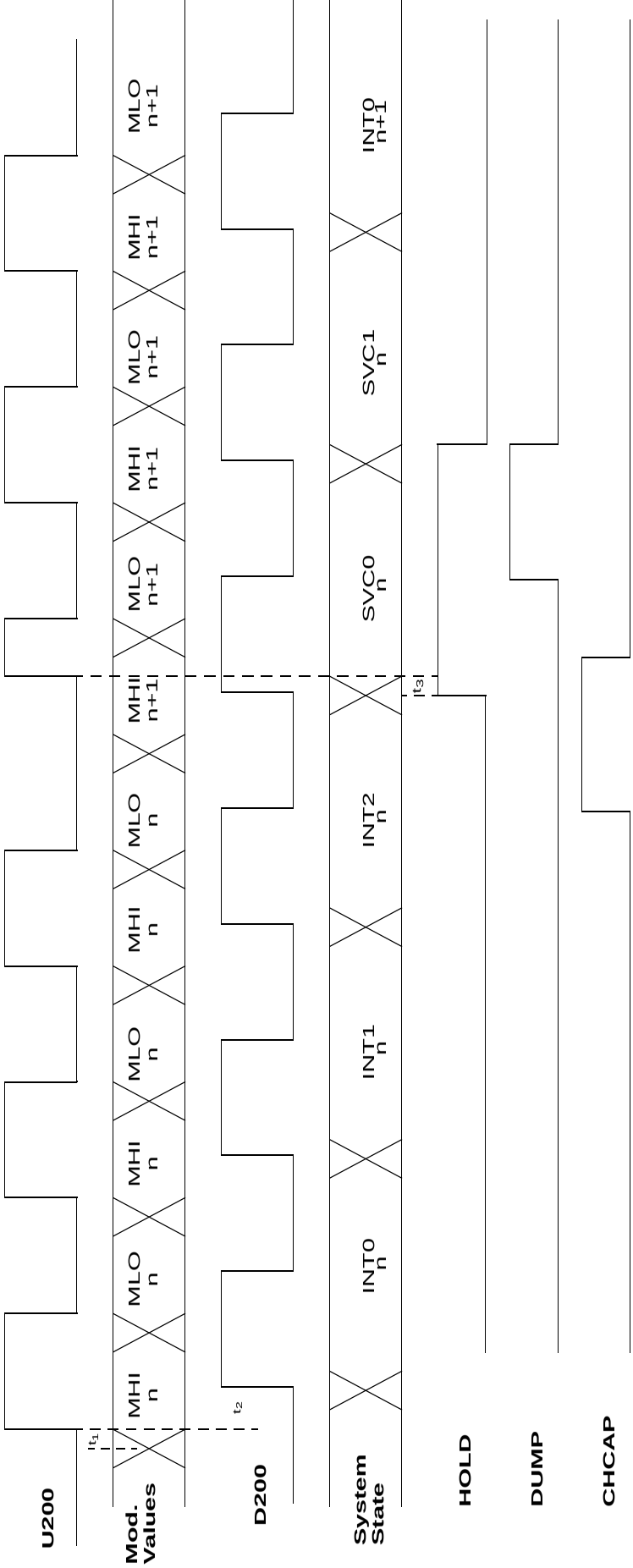
Appendix C
HV Modulator-to-FC Digital Board Pinout

The wiring interface is a hole pattern on the digital board which is consistent with a 25-pin MDM Socket Connector, M83513/0-D. (The board was layed out per Rev 08 of this document for a female, high-density D-subminiature connector.)

PC Pattern	Connector	Function	Internal Ties
1	1	+28VDC	2
2	2	+28VDC	1
3	3	Chassis Ground (Shields)	26
4	4	NC	
5	5	5VDC Return	12
6	6	+5VDC	
7	12	Command bit D1	
8	13	Command bit D0 (LSB)	
9	7	NC	
10	14	28VDC Return	11
11	15	28VDC Return	10
12	19	Analog -- Return	5
13	16	NC	
14	21	NC	
15	24	200Hz Command Strobe	
16	10	Command bit D3	
17	11	Command bit D2	
18		NC	
19	17	Analog -- Modulator B	
20	18	Analog -- Modulator A	
21	20	Analog -- Modulator Suppressor	
22	23	NC	
23	22	Modulator On Command	
24	8	Command bit D5 (MSB)	
25	9	Command bit D4	
26	25	Chassis Ground	3

Appendix D
Nominal HV Modulator Output Voltages

Command	Voltage (V)	Command	Voltage (V)
0	150	40	1872
1	160	41	1994
2	170	42	2124
3	181	43	2262
4	193	44	2409
5	206	45	2566
6	219	46	2733
7	233	47	2911
8	248	48	3101
9	265	49	3303
10	282	50	3518
11	300	51	3747
12	320	52	3991
13	341	53	4251
14	363	54	4528
15	387	55	4823
16	412	56	5137
17	438	57	5472
18	467	58	5828
19	497	59	6208
20	530	60	6612
21	564	61	7043
22	601	62	7501
23	640	63	7990
24	682		
25	726		
26	774		
27	824		
28	878		
29	935		
30	996		
31	1061		
32	1130		
33	1203		
34	1282		
35	1365		
36	1454		
37	1549		
38	1650		
39	1757		


U200
Mod. Values
D200
System State
HOLD
DUMP
CHCAP
t1
t2
t3
MHI n
MLO n
MHI n
MLO n
MHI n
MLO n
MHI n+1
MLO n+1
MHI n+1
MLO n+1
MHI n+1
MLO n+1
INT0 n
INT1 n
INT2 n
SVC0 n
SVC1 n
INT0 n+1

The delays pictured above are not to scale. The timing diagram shows the sequence of events in the course of one "measurement cycle" (n) and the beginning of the next measurement cycle (n+1). The system is programmed for an integration time of 15 ms and a service/recovery time of 10 ms.

Timing Parameters and Delays

Period of U200 and D200 = 5ms (200 Hz). They normally have a duty cycle of approximately 50%, except for U200 in the following circumstance: The U200 clock is conditioned such that preceeding the first service interval (when the A/D conversion is done) it stays low until after the "HOLD" signal is asserted. (HOLD is aligned with the D200 clock).

Parameter	Description	Time
t_1	Modulator value setup time before U200 rising or falling edge	6.7 us
t_2	U200 to D200 Delay (programmable via external jumpers).	Adjustable between about 5 us and 425 us in 6.7 us steps
t_3	HOLD rising edge to delayed onset of U200 clock during the SVC0	6.7 us

Definitions

Interval here refers to a 5 ms time segment, aligned with the D200 clock. Interval states are shown above in the time diagram (INT0, INT1..., SVC1). All intervals states, and decode signals described below, are algined with the D200 clock.

CHCAP: holds reference charge on capacitor at input to the comparator at the final stage of the analog electronics. This signal goes high at the second half of the last measurement interval, and goes low after autoranging is performed during the first service interval (less than 100 usec after HOLD is asserted).

HOLD: causes the integrated charge accumulated during the measurment cycle to be locked-in and held at the input to the final stage of the analog electronics. Asserted during SVC0 (first service interval).

DUMP: causes the charge on the reference capacitor, charged during the assertion of CHCAP, to be dumped following an A/D conversion. This signal is asserted during the second half of the SVC0 Interval, after A/D conversion has occurred.

REVISIONS

Letter	ECO No.	Description	Checked	Approved	Date
01		First Pass		RFG	2/28/99
02		Added Software Description		RFG	3/4/99
03		Changed to RS232 protocols		RFG	3/5/99
04		Reverted to custom serial protocol		RFG	3/31/99
05		Add Science comments		RFG	4/7/99
06		Add Modulator Interfaces		RFG	4/21/99
07		Add Status to I/F connector		RFG	4/27/99
08		Revise DPU connector pinouts		RFG	4/30/99
09		Add Digital/Analog board interface		RFG	5/3/99
10		Change Modulator pin outs		RFG	12/29/00
11		Clarify Calibration Directive		RFG	4/11/00
12		Add start-up timing requirements		RFG	6/21/00

	NAME	DATE
Drawn:		
Checked:		
Approved:		
Released:		

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CENTER FOR SPACE RESEARCH

Faraday Cup
Interface Control Document

Size	Code Identification No.	Drawing No.	Rev.
T	80230	27-03001	12

Scale: NONE