### TABLE 1

<table>
<thead>
<tr>
<th>Drawing Number</th>
<th>Voltage</th>
<th>Ref. Des</th>
</tr>
</thead>
<tbody>
<tr>
<td>50-40102</td>
<td>-5V</td>
<td>PAH</td>
</tr>
<tr>
<td>50-40103</td>
<td>-15V</td>
<td>PQ3</td>
</tr>
</tbody>
</table>

**NOTE:**
1. REFER TO KIT DRAWING 50-03202.0002 FOR SCHEMATIC.
2. FABRICATE IN ACCORDANCE WITH NASA-STD-8739-0.

- Mark voltage per Table Appendix where shown using F/N 23. Cover with F/N 24.
- Remove existing marking, R2 and C3 on silk screen and install R2 and C3 as shown. Remaining as shown is optional.

6. Bag and tag assemblies with part number, revision and serial number.
   - Bake all up solutions, both sides, prior to conferral coat.
   - Cure at 85C ambient pressure for 8 hours.
   - Remove masking and marking resist prior to bake.
8. Bake F/N 2 off F/N 1 by 75-80 prior to soldering F/N 1 to F/N 2.
9. EL R3, ES and GS are not used.