MWA Digital Receiver: Backplane circuit and PCB layout

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Abstract

This report gives the circuit schematic and PCB layout of the Backplane designed for the MWA Digital Receiver.

1 Backplane Description

The digital receiver consists of two ADFB (analog to digital converter filter bank) boards and an AgFo (Data aggregation and formatting) board. These three boards are plugged into a backplane (see Fig. 1), which provides the interconnection between the ADFB and AgFo boards.

The Backplane is an 8 layer PCB of size 263 mm x 285 mm. The data and the clock signals from the ADFB cards are in the form of LVDS. The high speed routing constraints such as (a) similar lengths for the LVDS (the LVDS 2.5 V is used for the design) PCB trace pairs, (b) separation and trace thickness adjusted for 100 ohms differential impedance and (c) smooth bending of the traces are considered during the design. The Backplane also distributes the 165 MHz FPGA clock and the synchronization signal SCTN, both in LVDS format. A jumper selection is provided to select the source of the FPGA clock and SCTN – they can either be connected from the AgFo card or from an external LVDS source through dual SMA connectors. For the interim software correlator for the 32T operations, the AgFo output data is provided at the Backplane, which can be connected to the VSIB data acquisition system. This feature is also useful for the initial testing of the digital receiver at the lab.

The circuit schematic of the Backplane is given in Appendix A. Appendix B gives the PCB layout files.

Acknowledgement

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Figure 1: (Left) Picture of the Digital Receiver under test at the Radio Astronomy Laboratory, RRI, Bangalore. The two ADFB boards and an AgFo board are marked on the picture. (Right) The three boards are plugged in to a Backplane. The Backplane provides the interconnection between the boards as well as the distribution of the clock and synchronization signal.

Reference

Briggs, F., 2007, February 25, MWA Knowledge Tree
Roshi, D. A., 2007, June 5, MWA Knowledge Tree
Appendix A : Backplane Circuit Schematic

Figure 2: Circuit schematic of the Digital Receiver Backplane (Page 1/2)
Figure 3: Circuit schematic of the Digital Receiver Backplane (Page 2/2)
Appendix B : PCB Layout and related plots

Figure 4: Mechanical and PCB parameters of Backplane
Figure 5: Component side PCB layout
Figure 6: PCB layout of layer 2: Ground layer
Figure 7: PCB layout of layer 3: Interconnection between ADFB and AgFo
Figure 8: PCB layout of layer 4: Ground layer
Figure 9: PCB layout of layer 5: power layer
Figure 10: PCB layout of layer 6: SCTN, clock and VSIB data connection
Figure 11: PCB layout of layer 7: power layer
Figure 12: Solder side PCB layout