The AgFo board receives CLOCK and Synchronization signal SCTN through the backplane connectors. A copy of this clock from the V5 FPGA (pins AB6, AB7 of BANK-18) is fed to SMA* J10(P) and J34(N). The signal SCTN is brought out to RJ45 J1 (pins 1 and 2). All the signals are in LVDS 2.5V level.

* Note: In the AGFO PCB, the legend (text) LVDS P and N are reversed. The J10 SMA connector is for the LVDS_P and J34 SMA is for the LVDS_N