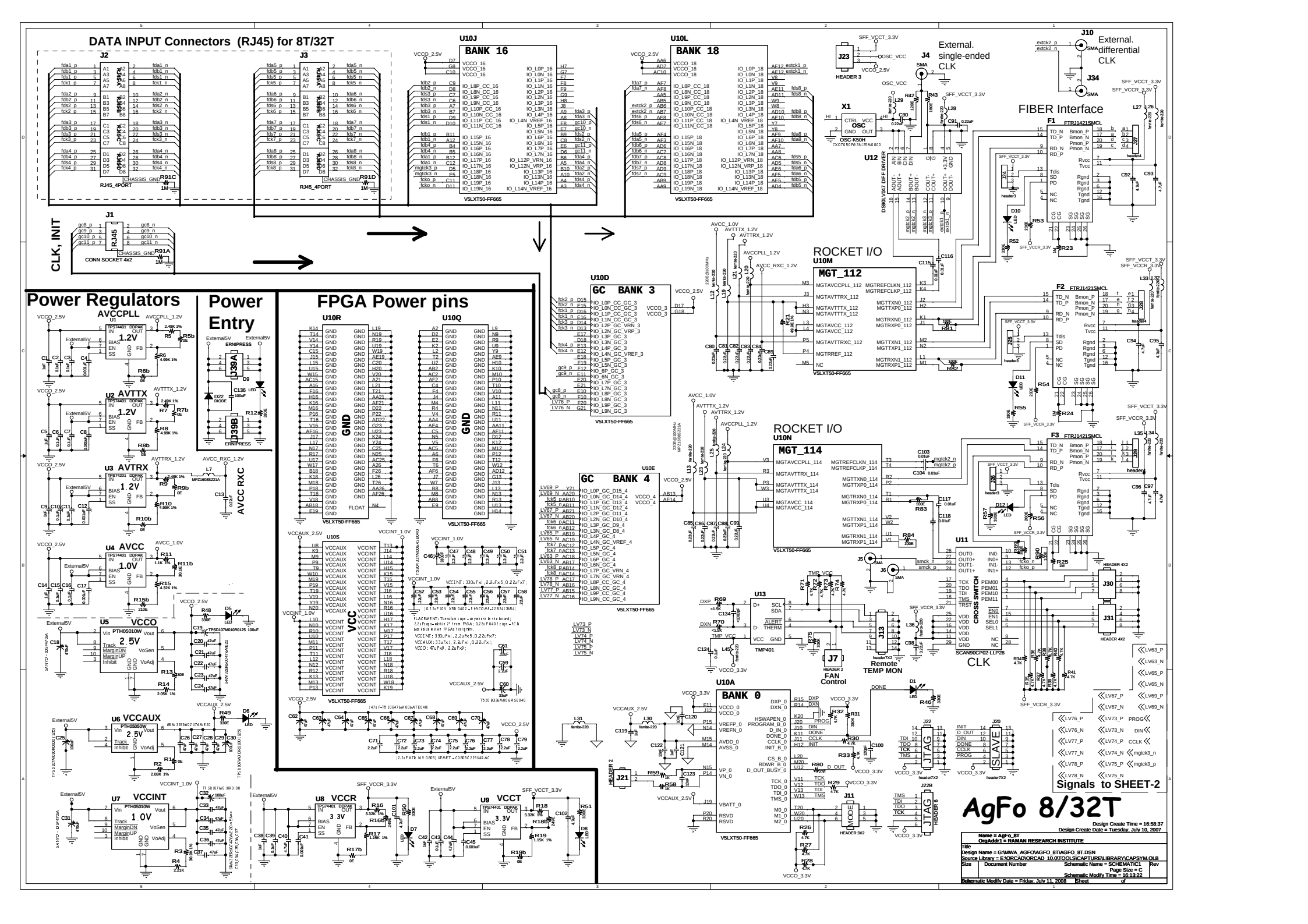
DATA INPUT Connectors (RJ45) for 8T/32T
J2
J3
RJ45_4PORT
CHASSIS_GND
CLK, INIT
J1
CONN SOCKET 4x2
U10J
BANK 16
U10L
BANK 18
V5LXT50-FF665
External. single-ended CLK
External. differential CLK
FIBER Interface
FTRJ1421SMCL
ROCKET I/O
U10M
MGT_112
U10N
MGT_114
Power Regulators
AVCCPLL
U2 AVTTX
U3 AVTRX
AVCC RXC
U4 AVCC
U5 VCCO
U6 VCCAUX
U7 VCCINT
U8 VCCR
U9 VCCT
Power Entry
FPGA Power pins
U10R
U10Q
U10S
VCC
U10D
GC BANK 3
U10E
GC BANK 4
U10A
BANK 0
U13
TMP401
Remote TEMP MON
FAN Control
SCAN90CP02-LZP28
CROSS SWITCH
CLK
JTAG
SLAVE
MODE
Signals to SHEET-2
AgFo 8/32T
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Design Name = G:\MWA_AGFO\AGFO_8T\AGFO_8T.DSN
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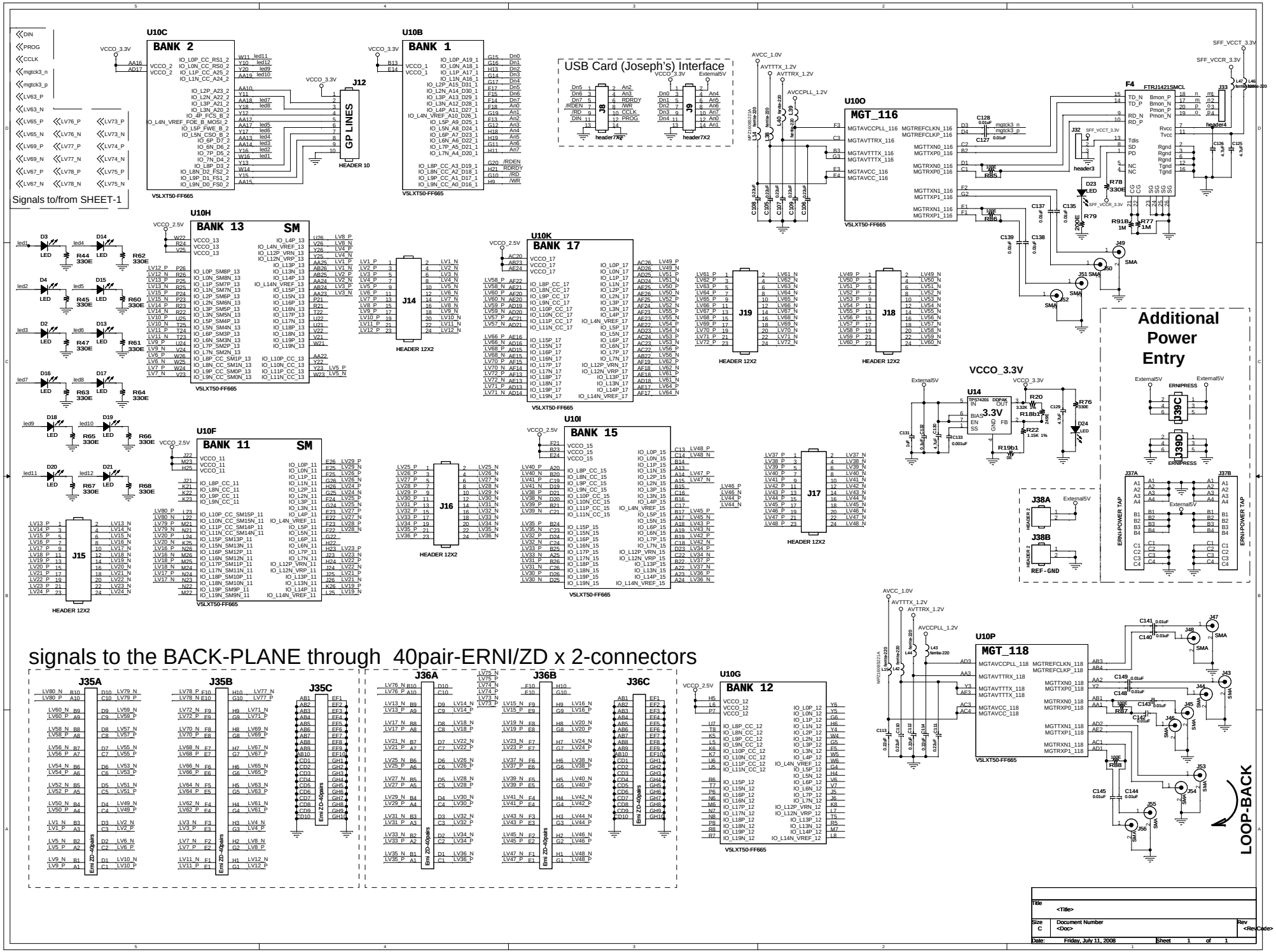

Signals to/from SHEET-1
U10C
BANK 2
U10B
BANK 1
USB Card (Joseph's) Interface
U10O
MGT_116
U10H
BANK 13
SM
U10K
BANK 17
U10F
BANK 11
SM
U10I
BANK 15
U10G
BANK 12
U10P
MGT_118
Additional Power Entry
VCCO_3.3V
GP LINES
HEADER 10
HEADER 12X2
V5LXT50-FF665
J12
J14
J15
J16
J17
J18
J19
J32
J33
J38A
J38B
J39C
J39D
J37A
J37B
J35A
J35B
J35C
J36A
J36B
J36C
J47
J48
J49
J50
J51
J52
J53
J54
J55
J56
F4
FTRJ1421SMCL
U14
3.3V
ERNI-POWER TAP
REF-GND
LOOP-BACK
signals to the BACK-PLANE through 40pair-ERNI/ZD x 2-connectors
Title
<Title>
Size
C
Document Number
<Doc>
Rev
<RevCode>
Date: Friday, July 11, 2008
Sheet 1 of 1