

REVISIONS

Letter	ECO No.	Description	Checked	Approved	Date
A		INITIAL RELEASE	BK	WFM	

	NAME	DATE	MASSACHUSETTS INSTITUTE OF TECHNOLOGY CENTER FOR SPACE RESEARCH			
Drawn:	J. R. O'Connor		Component Lead Preparation Procedure			
Checked:	Brian Klatt					
Approved:						
Released:						
			Size	Code Identification No.	Drawing No.	Rev.
			T	80230	99-03003	A
			Scale: NONE		Sheet: 1 of 3	

1.0 SCOPE

This drawing describes methods used to prepare electronic components for soldering into printed circuit boards.

2.0 PRECAUTIONS

2.1 CMOS IC's are particularly susceptible to damage, due to static discharge, prior to installation and termination into P.C. boards; therefore, care must be taken in handling while tinning. Refer to MIT spec. 64-02017.2006.

2.2 Solder with a gold content of greater than 3% can cause a problem. Solder with a gold content of 5% or greater causes gold embrittlement which reduces the ductility of the solder. Tinning of leads which have been gold plated, with a soldering iron, generally does not remove enough gold to prevent embrittlement. Solder pots contain a relatively large volume of solder compared to the amount of gold on leads, thus reducing the percentage of gold in the solder. This in turn, will maintain the ductility of the solder. Therefore, all leads which have been gold plated must be tinned in a solder pot.

2.3 The solder in the solder pot used for tinning of leads, should be changed frequently to prevent gold build-up in the solder.

3.0 REQUIREMENTS

Equipment and supplies to be used, are specified in and used per NHB 5300.4(3A-2)

Soldering irons, solder pots, solder, flux, lead-cleaning tools, solvents and wipes.

4.0 PROCEDURES

4.1 Discrete components (tin plated) R's, C's, CR's.

4.1.1 Equipment specified-solder pot or solder iron.

4.1.2 Remove lead oxidation with braid lead cleaner. Remove debris with kimwipe and ethyl alcohol. Tin leads using either solder pot or solder iron; Temperature 600 ± 35 F. Leads which show evidence of gold plating must be tinned in a solder pot. Clean flux off leads with kimwipe and ethyl alcohol.

4.2 Dip IC's

4.2.1 Clean with kimwipe and ethyl alcohol ONLY.

4.3 Gold plated lead devices. Discretes, Q's, CR's, relays, OP amps.

4.3.1 Equipment: Solder pot only.

4.3.2 Remove lead oxidation, where possible, with braid cleaner; otherwise, clean leads with Q-tip and ethyl alcohol. Remove debris with kimwipes and ethyl alcohol. Tin discrete leads with solder pot or solder iron unless leads were gold plated. Such devices must be tinned in a solder pot; Temperature 600 ± 35 F. Remove tinning with dri wick. Repeat tinning and removal process for a total of three (3) times if tinning with soldering iron; two (2) times if tinning in a solder pot. Clean flux off leads with kimwipe (or Q-tip) and ethyl alcohol.

4.4 Gold plated devices. Pin grid arrays and flat packs.

4.4.1 Equipment: Solder pot only.

4.4.2 Precautions: Insure anti-static handling.

MIT QA verify: Solder pot within specification. Work station must be properly grounded. Personnel voltage monitor should be used if available. Technician must be properly attired: Anti-static labcoat and wrist strap.

4.4.3 Clean leads with Q-tip and ethyl alcohol. Tin leads with solder pot. Temperature 600 ± 35 F. Repeat tinning and removal process for total a of two (2) times. Clean off flux with Q-tip and ethyl alcohol.

5.0 Q.A. PROVISIONS

MIT QA to inspect and sign off on A.W.O. on all tinned leads. MIT QA to verify anti-static handling in step 4.4.

6.0 PACKING

Tinned devices are to be replaced in anti-static foam (kit) for next assembly step.