Run BIASRET as etch alongside VBIASTHICK and VBIASTHIN from BiasVoltage Generation to J2 (analog subsystem connector).

Due to procurement issues, D504 and D505 are not populated on the flight boards.
28V from S/C is received via chassis mounted EMI-Filter and routed to chassis mounted DC-DC converters.

Chassis Ground connected to Signal Ground at the Power Supply.

Title: Crater Digital Control Board - Power In

- Pins 19 and 20 are used for Purge Flow Rate Monitor.
- 28VP/28VN: forwarded to analog housekeeping for voltage monitoring.
- 28VS/28VN: forwarded to analog housekeeping for current monitoring.

Distribute 10uF capacitors around board in Vcc regions.

Decouple AVN
Decouple AVP
ATEMP0: APB Temperature  -  ATEMP1: TB Temperature

Pin 61 is spare -- previously used for VREF

Crater Digital Control Board - Analog Board Interface
Diodes are not included in the Engineering board artwork, and have been added via rework.
Populate 0 ohm resistors to set the Instrument Serial Number. (Each 0 ohm resistor sets digit to zero.)

FPGA Spare Pin Test points - configured as spare gates or driven low.