Run BIASRET as etch alongside VBIASTHICK and VBIASTHIN from BiasVoltage Generation to J2 (analog subsystem connector).
28V from S/C is received via chassis mounted EMI-Filter and routed to chassis mounted DC-DC converters.

Chassis Ground connected to Signal Ground at the Power Supply.

Pins 19 and 20 are used for Purge Flow Rate Monitor.

Distribute 10uF capacitors around board in Vcc regions.

28VS/28VN: forwarded to analog housekeeping for voltage monitoring.
28VS/28VN: forwarded to analog housekeeping for current monitoring.
Comparator output pull-up option (dnp = do no populate resistors): current plan is to place the pull-ups on the analog board.

Pin 61 is spare -- previously used for VREF

256 Bits @ 1MHz
0-5V IN @ 1MHz, 0-5V-DC OUT
Vs = 400 kHz

256 Bits @ 1MHz
0-5V IN @ 1MHz, -0.047 - 0.141 V-DC OUT
Vs = 400 kHz

File: Crater Digital Control Board - PWM to DC Converters (Test Pulse and LLD)
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**Circuit Diagram Showing:***
- **R60, R61, R62, R63, R64, R65**: Resistors
- **C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64**: Capacitors
- **RH1498 U16, U17**: Operational Amplifiers
- **U16, U17**: Operational Amplifiers
- **R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82**: Resistors
- **C49**: Capacitor

**Component Values:**
- **R60, R61, R62, R63, R64, R65**: Various values
- **C50, C51, C52, C53, C54, C55, C56, C57, C58, C59, C60, C61, C62, C63, C64**: Various values
- **RH1498 U16, U17**: Operational Amplifiers
- **U16, U17**: Operational Amplifiers
- **R71, R72, R73, R74, R75, R76, R77, R78, R79, R80, R81, R82**: Various resistors
- **C49**: Various values

**Notes:**
- **0-5V IN @ 1MHz, 0-5V-DC OUT**
- **Vs = 400 kHz**
- **256 Bits @ 1MHz**
- **0-5V IN @ 1MHz, -0.047 - 0.141 V-DC OUT**
- **Vs = 400 kHz**

**Document Information:**
- **Consultation Number:** 02-0503
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**Date:** Wednesday, September 6, 2006
Populate 0 ohm resistors to set the Instrument Serial Number. (Each 0 ohm resistor sets digit to zero.)

FPGA Spare Pin Test points - some are configured as spare gates; unused I/Os will be driven low in final version.

No Ref Des required on silkscreen for these -- via size plated through hole OK

FPGA Pin 198 = 0 for flight layout; 1 for engineering layout.