Chassis Ground connected to Signal Ground at the Power Supply

T1 output routed to Chassis Mounted J-3 (A-bus)
T2 output routed to Chassis Mounted J-4 (B-bus)

Dynamic Bus Control disabled

Decouple each Power/Gnd set of U20 (BU-63705)

Keep CLK16 etch as short as possible, run as single line (no branches).

28V from S/C is received via chassis mounted EMI-Filter and routed to chassis mounted DC-DC converters to (chassis mounted) RTD

Locate R83 near U41

DCR - Address = 0x10
ADDRP set to 0 (for odd parity)

Dynamic Bus Control disabled

20V from S/C is received via chassis mounted EMI-Filter and routed to chassis mounted DC-DC converters (Chassis Ground connected to Signal Ground at the Power Supply)
Run BIASRET as etch alongside VBIASTHICK and VBIASTHIN from BiasVoltage Generation to J2 (analog subsystem connector).
Pins 19 and 20 are used for Purge Flow Rate Monitor

Distribute 10μF capacitors around board in Vcc regions

28VP/28VN: forwarded to analog housekeeping for voltage monitoring
28VISEN/28VN: forwarded to analog housekeeping for current monitoring
Comparator output pull-up option (dnp = do no populate resistors): current plan is to place the pull-ups on the analog board.
256 Bits @ 1MHz
0-5V IN @ 1MHz, 0-5V-DC OUT
Po = 400 kHz

See Sh. 1

Crater Digital Control Board - PWM to DC Converters (Test Pulse and LLD)
Populate 0 ohm resistors to set the Instrument Serial Number. (Each 0 ohm resistor sets digit to zero.)

FPGA Spare Pin Test points - some are configured as spare gates; unused I/Os will be driven low in final version.

No Ref Des required on silkscreen for these -- via size plated through hole OK