Chassis Ground connected to Signal Ground at the Power Supply.

T1 output routed to Chassis Mounted J-3 (A-bus)
T2 output routed to Chassis Mounted J-4 (B-bus)

Broadcast mode disabled

RT-Address = 0x10
ADDRP set to 0 (for odd parity)

Dynamic Bus Control disabled

Keep CLK16 etch as short as possible, run as single line (no branches).

32V-03003 see Sh. 1

Decouple each Power/Gnd set of U20 (BU-63705)

Locate R93 near U41

Decouple each Power/Gnd set of U20 (BU-63705)
Connections for the VBIAS subsystem

BVCK[1:0] (not used by Bias Voltage Generator) are spares
28VP/28VN: Outputs of EMI Filter - forwarded to analog housekeeping

Distribute 10uF capacitors around board in Vcc regions

Pins 12 and 5 are used for Purge Flow Rate Monitor

Decouple AVN
Decouple AVP

DTEMP[2:1]
Comparator output pull-up option (dnp = do no populate resistors): current plan is to place the pull-ups on the analog board.
256 Bits @ 1MHz
0-5V IN @ 1MHz, 0-5V-DC OUT
F0 = 400 Hz

File: Crater Digital Control Board - PWM to DC Converters (Test Pulse and LLD)
Revision B
Document Number: 02-03003

Tuesday, May 30, 2006
Populate 0 ohm resistors to set the Instrument Serial Number. (Each 0 ohm resistor sets digit to zero.)

FPGA Spare Pin Test points - some are configured as spare gates; unused I/Os will be driven low in final version.

No Ref Des required on silkscreen for these -- via size plated through hole OK