Check decoupling
Do not overlap analog versus digital grounds
Place power on separate PCBs
Check power traces and components
Check output signals/inputs termination

C

AnalogSignalProc

GATE[5:0]
RAMP[5:0]
SCLK[5:0]
SDAT[5:0]
CS[5:0]
DETTRIG[5:0]
DET[6:1]
LLD[1:0]
VREF25

AnalogProcIF

Connector to CRaTER Analog Board

DET[6:1]
VBIASTHICK
VBIASTHIN
PULSERDC
SCOUNT[5:0]
DETIMON[6:1]
ATEMP[1:0]
PCLOCK[1:0]
TDMON[3:1]
BIASRET
VREF25

BiasVoltageGen

VBIASTHICK
VBIASTHIN
ENBVBTHICK
ENBVBTHIN
IMONTHIN
IMONTHICK
VMONTHIN
VMONTHICK
BVCK[1:0]
BIASRET
VREF25

PowerIn

Connector to Power Modules

28VP
28VN
PURFLWRATE

PWMtoDC

PULPWM
LLDPWM[1:0]
LLD[1:0]
PULSERDC

CNTL

SA[4:0]
CLK16M
DATA[15:0]
TRRCV
HSFAIL
DATCMD
RDWR
NBGT
INCMD
BITEN
STATEN
GBR
DTREQ
DTSTR
WC[4:0]
SSREQ
SSFLAG
SSBUSY
ILLCMD
DTGNT
HWRSTL
CLK1HZ_SC
DETTRIG[5:0]
SDAT[5:0]
GATE[5:0]
RAMP[5:0]
SCLK[5:0]
CS[5:0]
HKSCLK
HKSDAT
HKMUXSEL[1:0]
HKMUXADR[3:0]
BVENB[1:0]
LLDPWM[1:0]
PULPWM
SCOUNT[5:0]
BVCK[1:0]
PCLOCK[1:0]
DTACK

Housekeeping

HKCS
HKSCLK
HKMUXSEL[1:0]
VREF25
28VP
28VN
IMONTHICK
IMONTHIN
VMONTHICK
VMONTHIN
ATEMP[1:0]
TDMON[3:1]
DETIMON[6:1]
RTD_SC
HKSCLK
HKSDAT
HKMUXSEL[1:0]
VREF25
28VP
28VN
IMONTHICK
IMONTHIN
VMONTHICK
VMONTHIN
ATEMP[1:0]
TDMON[3:1]
DETIMON[6:1]
RTD_SC

SciInterface

HWRSTL
ILLCMD
DTGNT
RTD_SC
HKSCLK
HKMUXADR[3:0]
BVENB[1:0]
LLDPWM[1:0]
PULPWM
SCOUNT[5:0]
BVCK[1:0]
PCLOCK[1:0]
DTACK

BiasVoltageGen

VBIASTHICK
VBIASTHIN
ENBVBTHICK
ENBVBTHIN
IMONTHIN
IMONTHICK
VMONTHIN
VMONTHICK
Chassis Ground connected to Signal Ground at the Power Supply

T1 output routed to Chassis Mounted J-3 (A-bus)
T2 output routed to Chassis Mounted J-4 (B-bus)

Broadcast modedisabled

RT-Address = 0x10
ADDRP set to 0 (for odd parity)

Dynamic Bus
disabled

Decouple each Power/Gnd set of the BU-63705
DECOUPLE Oscillator and 26C32

Keep CLK16 etch as short as possible, run as single line (no branches).

28V from S/C is received via chassis mounted EMI-Filter and routed to chassis mounted DC-DC converters
To (chassis mounted) RTD

Use Vcc and digital ground here? (so that analog ground doesn’t have to run to this segment of the board)

CRATER Digital Control - Spacecraft Interface
Connections for the VBIAS subsystem

Title: Crater Digital Control Board - Bias Voltage Generation

Date: Thursday, February 23, 2006

Sheet 4 of 11
4.08V

Assume AD590, biased to Analog VP at location sensor site

Voltage Range OK?

Scaling of these values?

Used for testing only. Analog and Digital grounds are connected at the supply in the final configuration.

Radiation Tolerance of ADG526A sufficient?

TBD: Temp Sensor Locations

13           IMONTHICK
14           VMONTHICK
15           -6V Monitor
16           VMONTHIN
17           +6V Monitor
18           5V Monitor
19           28V Monitor
20           Purge Flow Rate
21           AMUX-ADDR       Measurement
22           LLD0 Level
23           LLD1 Level
24           IMONTHIN
25           Housekeeping Entries:
26           RTD - S/C
27           DTEMP0
28           DTEMP1
29           ATEMP0 - Telescope Temp
30-31        Detector Current Monitors
32-33        Dose Monitor
34           Test Pulser Level
35           Need to add inputs (or assign the DTEMP inputs) for:
36           Aft Bulkhead Temp
37           Forward Bulkhead Temp
38           Power Supply Temp
39           32-03003
40           see Sh.1
41           Crater Digital Control Board - Housekeeping

Title
Size Document Number Rev Date: Sheet

VREF25
HKMUXADR0
HKMUXADR1
HKMUXADR2
HKMUXADR3
HKMUXSEL0
HKMUXSEL1
HKMUXSEL2
HKMUXSEL3
VMON28V
VMON5V
VMON6VP
VMON6VN
LLD0
LLD1
ATEMP[1:0] ATEMP0
ATEMP1
DTEMP[1:0] DTEMP0
DTEMP1
DETIMON1
DETIMON2
DETIMON3
DETIMON4
DETIMON5
DETIMON6
TDMON1
TDMON2
TDMON3

AVP
AVN
VCC
AVP
AVN
AVP
AVN
AVP
AVN
AVP
AVN
AVP
AVN
AVP
AVN
AVP
AVN
28VP/28VN: Outputs of EMI Filter - forwarded to analog housekeeping

Distribute 10uF capacitors around board in Vcc regions

Decouple AVN
Decouple AVP

Distribute 10uF capacitors around board in Vcc regions

28VP/28VN: Outputs of EMI Filter - forwarded to analog housekeeping
Comparator output pull-up option (dnp = do no populate resistors): current plan is to place the pull-ups on the analog board.

Any other termination recommended?

Analog Board Requires 0-5V -- further scaling or termination required?

ATEMP[1:0] AFIN Temperature - ATEM0: THTemperature

Comparator output pull-up option (dnp = do no populate resistors): current plan is to place the pull-ups on the analog board.

Any other termination recommended?

Analog Board Requires 0-5V -- further scaling or termination required?

ATEMP[1:0] AFIN Temperature - ATEM0: THTemperature
Should the ADC be connected to AGND or DGND (it is connected to the digital supply)?
256 Bits @ 1 MHz
0-5V IN @ 1 MHz, 0-5V-DC OUT
Fc = 400 Hz

256 Bits @ 1 MHz
0-5V IN @ 1 MHz, 0-1V-DC OUT
Fc = 400 Hz