CRaTER

Analog to Digital Subsystem

Electrical Interface Control Document

Drawing Number: 32-02052

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1. Scope
This document specifies the electrical interface between the Analog Processing Board and the Digital Processing Board within the CRaTER electronics box. This document does not describe the interface between the Detector Telescope and the Analog Processing Board, although references are made to the Detector Boards inside the Telescope as appropriate.

2. Applicable Documents
32-01205 CRaTER Level 2 Mission Requirements Document
32-02001 Spacecraft to CRaTER Data ICD
32-02002 Spacecraft to CRaTER Electrical ICD
32-10201 Analog PCB Outline Drawing
32-10202 Digital PCB Outline Drawing

3. Functional Description
The Analog Processing Board (APB) will be located inside the electronics box in an conductively shielded enclosure. The Digital Processing Board (DPB) will also reside in the same box and will interface to the APB with two connectors, one for power and one for signals. A high-level functional interface block diagram is shown in Figure 1.

![Analog Interface Block Diagram Concept]

Figure 1: Analog Interface Block Diagram Concept
3.1. Analog Processing Board
The APB provides a linear transfer function of output signal amplitude to detector energy deposit for three thin detectors and three thick detectors. A functional block diagram of a single amplifier string is shown in Figure 2. The shape of each output pulse is Gaussian and scaled in amplitude to achieve the full dynamic range of the DPB A/D subsystem. An amplified signal with low-level discriminator is provided to aid ground testing of the APB and to increment singles counters on the DPB.

![Figure 2: Single Amplifier String Block Diagram](image)

3.2. Digital Processing Board
The DPB function is to determine event validity through the use of a stacked detector coincidence scheme, digitize the pulse-heights of the APB output signals, provide control of the APB test pulser, supply power and detector bias, and provide the command and telemetry interface to the spacecraft.

4. Detector Signal Interfaces
Detector signals are amplified and filtered versions of the detector charge. There are three thin detector signals and three thick detector signals. Correspondingly, there are three thin and three thick discriminator signals.

4.1. Thin Detector Signal (DET_140_1, DET_140_3, DET_140_5)
The thin detector signal is a pulse whose peak voltage is proportional to the charge deposited in a thin detector. The source of the thin detector signal is the APB and the destination is the DPB. There are three thin detector signals each corresponding to one of three thin detectors.

4.1.1. Voltage Range
The thin detector signal shall be a positive unipolar pulse with a linear range of 0V to +3V. Input protection of the ADC system shall be implemented on the DPB to protect against signals outside this range. There will be no limiting on the APB, except the power supply rails.
4.1.2.  Peaking Time
The thin detector signal shall be a Gaussian shaped pulse with a peaking time of 1 usec +/- 20%.

4.1.3.  Noise
The thin detector noise voltage shall be less than 1.5 mVrms.

4.1.4.  Transfer Function
The thin detector transfer function shall be nominally 3 mV/MeV into 1 Meg-ohm. The actual transfer function will be determined during electrical calibration of the APB with the DPB.

4.1.5.  Output Impedance
The thin detector signal output impedance shall be less than 100 ohms.

4.2.  Thick Detector Signal (DET_1000_2, DET_1000_4, DET_1000_6)
The thick detector signal is a pulse whose peak voltage is proportional to the charge deposited in a thick detector. The source of the thick detector signal is the APB and the destination is the DPB. There are three thick detector signals each corresponding to one of three thick detectors.

4.2.1.  Voltage Range
The thick detector signal shall be a positive unipolar pulse with a linear range of 0V to +3V. Input protection of the ADC system shall be implemented on the DPB to protect against signals outside this range. There will be no limiting on the APB, except the power supply rails.

4.2.2.  Peaking Time
The thick detector signal shall be a Gaussian shaped pulse with a peaking time of 1 usec +/- 20%.

4.2.3.  Noise
The thick detector noise voltage shall be less than 1.5 mVrms.

4.2.4.  Transfer Function
The thick detector transfer function shall be nominally 30 mV/MeV into 1 Meg-ohm. The actual transfer function will be determined during electrical calibration of the APB with the DPB.

4.2.5.  Output Impedance
The thick detector signal output impedance shall be less than 100 ohms.
4.3. **Thin Detector Discriminator (DISC_140_1, DISC_140_3, DISC_140_5)**
The thin detector discriminator is a CMOS digital signal giving early indication of the arrival of the thin detector signal. The source of this signal is the APB and the destination is the DPB.

This signal shall be used by the DPB to increment thin detector singles counters.

4.3.1. **Voltage Range**
Logic 0 corresponds to 0-volts and logic 1 corresponds to 5-volts. The pulse width shall be 5 usecs +/- 10%.

4.3.2. **Timing**
The rising edge indicates the arrival of a thin detector signal and shall occur no less than 200ns before the peak amplitude is reached. The rising edge of this signal shall be less than 25 nsecs into 1-MegOhm and 10pF.

4.4. **Thick Detector Discriminator (DISC_1000_2, DISC_1000_4, DISC_1000_6)**
The thick detector discriminator is a CMOS digital signal giving early indication of the arrival of the thick detector signal. The source of this signal is the APB and the destination is the DPB.

This signal shall be used by the DPB to increment thick detector singles counters.

4.4.1. **Voltage Range**
Logic 0 corresponds to 0-volts and logic 1 corresponds to 5-volts. The pulse width shall be 5 usecs +/- 10%.

4.4.2. **Timing**
The rising edge indicates the arrival of a thick detector signal and shall occur no less than 200ns before the peak amplitude is reached. The rising edge of this signal shall be less than 25 nsecs into 1-MegOhm and 10pF.

5. **Test Pulser Interfaces**
The test pulser function is used during ground test phases and on-orbit to monitor the transfer function stability with time. The test pulser injects a known charge into the front of each preamplifier at a known rate. The DPB will supply one programmable voltage level and two clocking signals; one for a high range input to test amplifier saturation and one for a low range input to test the thresholds. The APB will convert these signals into a charge injection into the detector preamplifiers.

5.1. **Pulser Level (P_LEVEL)**
The source of this signal is the DPB and the destination is the APB.
5.1.1. Voltage Range
The pulser level is a DC analog voltage. The linear range is from 0 to 5-volts. Input protection of the circuitry shall be implemented on the APB to protect against signals outside this range. There will be no limiting on the DPB, except the power supply rails.

5.1.2. Resolution
The resolution for level settings shall be 8-bits.

5.1.3. Output Impedance
The output impedance shall be less than 100 ohms.

5.2. Pulser High Range Clock (PCLK_H)
The High Range Clock is a clock whose frequency corresponds to the rate of charge injection into the preamplifiers and whose amplitude is controlled by the pulser level and scaled on the APB to test the APB amplifiers mid range and overload performance. The source of this signal is the DPB and the destination is the APB. This signal will be used for both thin and thick detector strings.

5.2.1. Voltage Range
The High Range Clock is a CMOS digital signal with 0-volts corresponding to logic 0 and 5-volts corresponding to logic 1. A logic 0 triggers the test pulser circuit on the APB to inject charge into the front of both the thin and thick detector preamps. The amount of charge injected is determined by the pulser level and by a fixed resistor on the APB.

5.2.2. Timing
The logic 0 pulse width shall be fixed and no less than 50 usec. The logic 1 pulse width shall be determined by the low and high rate selections on the DPB.

5.3. Pulser Low Range Clock (PCLK_L)
The Low Range Clock is a clock whose frequency corresponds to the rate of charge injection into the preamplifiers and whose amplitude is controlled by the pulser level and scaled on the APB to test the APB amplifiers threshold and mid range performance. The source of this signal is the DPB and the destination is the APB. This signal will be used for both thin and thick detector strings.

5.3.1. Voltage Range
The Low Range Clock is a CMOS digital signal with 0-volts corresponding to logic 0 and 5-volts corresponding to logic 1. A logic 0 triggers the test pulser circuit on the APB to inject charge into the front of both the thin and thick detector preamps. The amount of charge injected is determined by the pulser level and by a fixed resistor on the APB.

5.3.2. Timing
The logic 0 pulse width shall be fixed and no less than 50 usec. The logic 1 pulse width shall be determined by the low and high rate selections on the DPB.
5.4. **Pulser Reference (PREF)**
A 2.5V reference shall be supplied by the DPB for use by the APB in the test pulser driver circuit. The maximum load created by the APB shall be less than 250 uA.

6. **Housekeeping Signal Interfaces**

6.1. **Telescope Temperature (TB_TEMP)**
The telescope temperature signal is a DC analog signal in the range 0 to +3 volts corresponding to a linear function of temperature from –50C to +60C, respectively. The source of this signal is the APB, however the temperature transducer will actually be located in the Telescope. The output impedance shall be less than 100 ohms.

6.2. **Analog Processing Board Temperature (APB_TEMP)**
The APB temperature signal is a DC analog signal in the range 0 to +3 volts corresponding to a linear function of temperature from –50C to +60C, respectively. The source of this signal is the APB. The output impedance shall be less than 100 ohms.

6.3. **Total Dose Monitor (TDMON_1, TDMON_2, TDMON_3)**
The APB board will contain a device for measuring the total radiation dose experienced by the electronics on the APB board. The device will provide three analog outputs corresponding linearly to total dose with three respective coefficients.

Total Dose = D1*Range1 + D2*Range2 + D3*Range 3.

6.3.1. **Output Voltage Range 1**
The signal range shall be from 0 to +3 volts, DC. This output provides the highest resolution approximately equal to 0.976 volt per milli-Rad. The actual coefficient, D1, is TBD and will be obtained during device testing. The source impedance shall be less than 100 ohms.

6.3.2. **Output Voltage Range 2**
The signal range shall be from 0 to +3 volts, DC. This output provides a medium resolution approximately equal to 3.81 volt per Rad. The actual coefficient, D2, is TBD and will be obtained during device testing. The source impedance shall be less than 100 ohms.

6.3.3. **Output Voltage Range 3**
The signal range shall be from 0 to +3 volts, DC. This output provides a low resolution approximately equal to 14.9 milli-volt per Rad. The actual coefficient, D3, is TBD and will be obtained during device testing. The source impedance shall be less than 100 ohms.
6.4. **Thin Det. Leakage Current Monitor (MON_140_1, MON_140_3, MON_140_5)**
The thin detector leakage current monitors shall be a DC voltage in the range 0 to +3 volts. The output resistance shall be less than 100 ohms. The conversion will be nominally 0.3V per micro-amp.

6.5. **Thick Det. Leakage Current Monitor (MON_1000_2, MON_1000_4, MON_1000_6)**
The thin detector leakage current monitors shall be a DC voltage in the range 0 to +3 volts. The output resistance shall be less than 100 ohms. The conversion will be nominally 1V per micro-amp.

7. **Detector Bias Supplies**
The specifications for the bias supplies are derived from several system parameters: range of detector operating voltage, size of detector bias resistor, and maximum practical loading of the bias source. Because the detector specification allows for a wide range of depletion voltages, the bias supplies must be capable of much larger voltages than what might be necessary once the detectors are delivered. In light of this, a voltage divider on the Telescope board will allow the bias voltage to be reduced as necessary to operate the detector in the safe range. Nominally, the bias will be set to 30 volts higher than the full depletion voltage. The total equivalent resistance, including the divider and the series bias resistor, is chosen to keep the bias point stable within 15 volts, so that the detectors will always be biased 15 volts higher than depletion over a large range of leakage currents. These factors contribute to the maximum load capability required of the bias supplies.

7.1. **Thin Detector Bias (BIAS_75V)**
The thin detector bias is supplied by the power system through the DPB.

7.1.1. **Output Voltage**
The thin detector bias is a stable positive DC voltage of +75V +/- 2.5%. This voltage will be tuned on the APB/Detector Board using a resistive divider to meet the bias requirements of the thin detector.

7.1.2. **Load**
The detector leakage current in addition to the resistive divider current creates the total load on the bias supply. The total current drawn by the thin detector bias supply (i.e., sum of all three thin detectors) shall not exceed 50 uA.

7.1.3. **Ripple**
The ripple on this bias shall be less than 1-volt peak-to-peak at an oscillator frequency of 100 KHz or greater at the maximum load. The APB will have a low pass filter with cutoff nominally set to 10 Hz, which will attenuate the ripple by 80dB assuming this oscillator frequency. Therefore, ripple at the detector will be kept well below the noise.

7.1.4. **Output Impedance**
The output resistance shall be less than 10 Kohm.
7.2. **Thick Detector Bias (BIAS_225V)**

The thick detector bias is supplied to the APB/Detector Board by the power system through the DPB.

7.2.1. **Output Voltage**

The thick detector bias is a stable positive DC voltage of +225V +/- 2.5%. This voltage will be tuned on the APB/Detector Board using a resistive divider to meet the bias requirements of the thick detector.

7.2.2. **Load**

The detector leakage current in addition to the resistive divider current creates the total load on the bias supply. The total current drawn by the thick detector bias supply (i.e., sum of all three thin detectors) shall not exceed 150 uA.

7.2.3. **Ripple**

The ripple on this bias shall be less than 3-volt peak-to-peak at an oscillator frequency of 100 KHz or greater at the maximum load. The APB will have a low pass filter with cutoff nominally set to 10 Hz, which will attenuate the ripple by 80dB assuming this oscillator frequency. Therefore, ripple at the detector will be kept well below the noise.

7.2.4. **Output Impedance**

The output resistance shall be less than 30 Kohm.

8. **Power Supply Interfaces**

8.1. **+5V Analog Power (P5V_ANLG)**

The DPB/Power system will supply a positive power supply for the analog electronics. The APB and Telescope Boards will use this supply for the detector signal processing.

8.1.1. **Output Voltage**

The DPB/Power system shall provide positive regulated power of +5V +/- 5%.

8.1.2. **Load**

The APB/Telescope shall draw no more than 250 mA from the +5V supply. The nominal load will be 230 mA.

8.1.3. **Ripple**

The ripple shall not exceed 60mV peak-to-peak at a frequency not less than 100 KHz.

8.2. **–5V Analog Power (N5V_ANLG)**

The DPB/Power system will supply a negative power supply for the analog electronics. The APB and Telescope Boards will use this supply for the detector signal processing.
8.2.1. Output Voltage
The DPB/Power system shall provide negative regulated power of -5V +/- 5%.

8.2.2. Load
The APB/Telescope shall draw no more than 155 mA from the -5V supply. The nominal load will be 140 mA.

8.2.3. Ripple
The ripple shall not exceed 60mV peak-to-peak at a frequency not less than 100 KHz.

8.3. +5V Digital Power (P5V_DIG)
The DPB/Power system will supply a positive power supply for digital electronics. The APB will use this supply voltage for the discriminator and test pulser.

8.3.1. Output Voltage
The DPB/Power system shall provide positive regulated power of +5V +/- 10%.

8.3.2. Load
The APB/Telescope shall draw no more than 55 mA from the +5V supply. The nominal load will be 50 mA.

8.3.3. Ripple
The ripple shall not exceed 200mV peak-to-peak at a frequency not less than 100 KHz.

9. Grounding

Figure 3: Grounding Diagram
The CRaTER grounding diagram is shown schematically in figure 3.

9.1. **Power Returns (ARTN, DRTN)**
The analog +/- 5V return shall be connected to the digital +5V return at the input to the A/D converters on the DPB, and nowhere else unless a board jumper is provided that can be removed.

9.2. **Bias Supply Returns (BIAS_RTN)**
The thin and thick bias supply returns shall be united as one bias return and connected to the digital ground on the DPB. The bias return will not be connected to any grounds in the Telescope or APB unless a board jumper is provided that can be removed.

9.3. **Chassis Grounding**
The telescope housing shall be connected to the analog ground inside the telescope assembly, and nowhere else unless a jumper is provided that can be removed.

The telescope housing shall be electrically isolated from the electronics box in order to prevent noise coupling from the spacecraft into the detector front-end.

The electronics box housing shall be connected to the digital ground inside the electronics box.
10. **Connector Pin Assignments**

The APB shall provide a 78 pin high density D-subminiature, pcb-mount, male connector per Analog Board Outline drawing 32-10201. The pin assignments shall be as follows.

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