AT40KEL040 Reprogrammable SRAM based FPGA Total Dose (TID) and Single Event Effects (SEE)

Radiation Test Summary Report

AT40KEL040

Abstract

Taking into account the growing demand of the space industry for reprogrammable FPGAs as alternatives to low gate count ASICs, Atmel has redesigned its existing commercial SRAM based reprogrammable FPGA, into a radiation hardened device: the AT40KEL040, allowing typically for 40K used gates (in addition with 18 Kbits of user SRAM), while SEU (Single Event Upset) hardening all heavy ions susceptible structures.

This chip has been designed on the Atmel CMOS 0.35 micron radiation hardened process.

This report gives a summary of the radiation test results obtained on this product. In addition, some information are given on the 1Mbit Serial EEPROM AT17LV010-10DP to be used as a configuration memory in association with the AT40KEL040 FPGA.

Total Dose Capability

The AT40KEL040 FPGA is manufactured on Atmel CMOS 0.35 micron radiation hardened process.

This radiation hardened process is regularly monitored and test vehicles are irradiated to confirm the high tolerancy of this process to cumulated dose.

The last total dose test on the dedicated test vehicle was performed in 2003 in accordance with 1019.5 MIL STD 883 test method. Tests were performed on 10 parts (with one additional control part) using a Co-60 source. The irradiation was performed at 25°C with a dose rate of 360 rad/h to a total dose of 300 krad(Si), with a 3.6V bias. Electrical tests were performed before irradiation and after 100, 200 and 300 krad(Si) of cumulated dose. After a 24 hours room temperature annealing, a high temperature annealing under bias during 168h at 100°C was performed, with a final electrical characterization.

All parts passed all functional and electrical tests up to 200 krad(Si).

At 300 krad(Si), all parts were functional, the dynamic parameters were unchanged and no leakage was measured. For two parts only, the standby current (ICCSB) showed a drift out of the specification at this total dose value.

After the 100°C accelerated ageing, all parts were still functional and the supply current of the two above mentioned parts did not exhibit parametric shifts above the specification any more. No rebound effect was found.

The Atmel CMOS 0.35 micron radiation hardened process is therefore developed and monitored to support a total dose of at least 200 krad(Si).

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The AT40KEL040 FPGA, using this radiation hardened process, can therefore be considered to be capable of supporting at least 200 krad(Si) of total dose. A dedicated total dose test on AT40KEL040 FPGA parts is on-going to confirm these results. The result of this dedicated test will be available on demand from Q3 2004.

SEU Test Rationales

The AT40KEL040 FPGA reprogrammable capability brings new advantages to the space community, such as fast and multiple prototyping iterations at no additional cost for the silicon, and potential on-orbit changes. However, this reprogrammable capability exhibits a sensitivity of the functionality of the device. If a bit in the configuration memory upsets due to an heavy ion impact, the functionality of the device can be lost.

A few approaches exist to mitigate such SEE effects on the configuration memory of SRAM based FPGAs. One of these approaches is to detect upsets by readback of the memory and to re-configure the SRAM based FPGA in case a difference with a configuration reference is found. An other approach uses memory scrubbing. In both cases, these mitigation techniques bring significant system overhead and put some constraints on other devices around the SRAM based FPGAs (e.g. PROMs or EEPROMs, additional logic).

The approach taken by Amel is significantly different. The objective, when designing the AT40KEL040 re-programmable FPGA, was to get a SEU hardened configuration memory so that the error rate in space is sufficiently low to prevent using complex additional mitigation techniques at the expense of the available useable gates.

Atmel has replaced all the memory elements of this design (configuration memory as well as user SRAM) by SEU hardened flip-flops. Of course, this use of SEU hardened flip-flops had to fit with the following constraints:

- no impact on the functionality of the device,
- minimize the impact on the performance of the device,
- minimize the impact on the die area,
- minimize the impact on the power consumption.

The SEE test results presented below will focus on the sensitivity of the configuration memory.

SEU Test Methodology

Configuration memory upset impact

The impact of an upset in the configuration memory varies with the place where the upset could occur. The following categories of impacts can be expected by such an event:

- functional failure: the bit upset changes the functionality of the device,
- no impact: the bit upset is not used for the particular design resources,
- programming system error: the state machine can be modified by an heavy ion impact. Such event could imply for example a misfunctioning of the configuration download or a functional failure.

Test Set-up

The AT40KEL040 configuration memory has been tested in January and February 2003 during two test campaigns at IPN (Orsay, France) and JYFL (Jyvaskyla, Finland), at 3V biasing.

The test sequence used is the following:

- the device is programmed outside of the beam from a serial EEPROM,

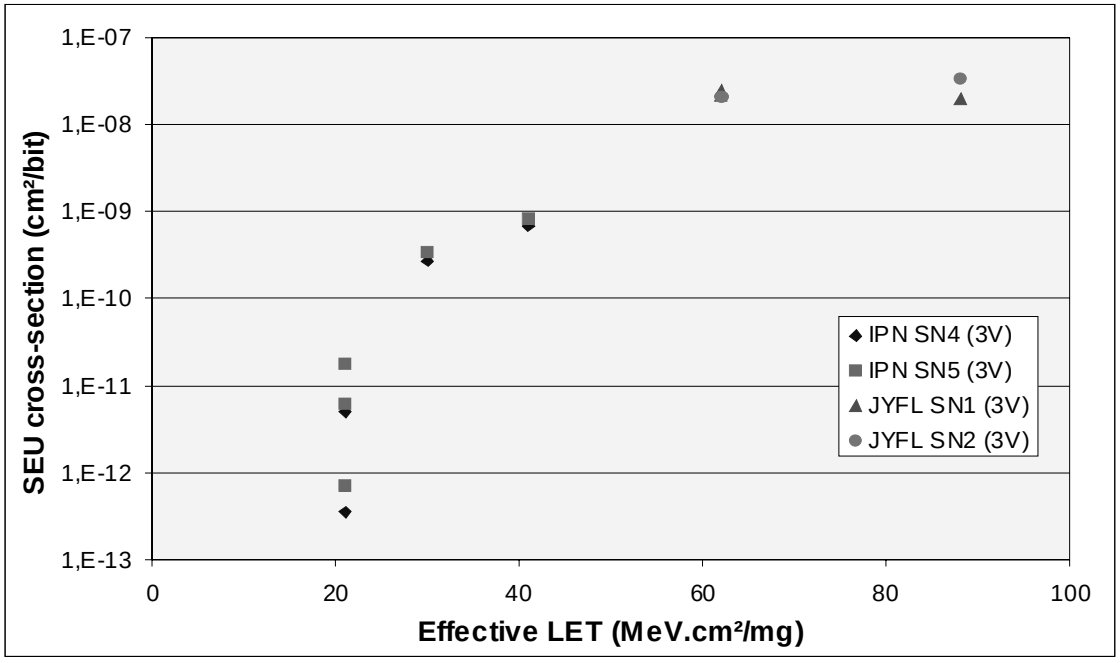
- the state of the device is then changed to “parallel SRAM access” configuration mode. In this mode, the configuration memory can be read as a standard SRAM,
- the device is exposed to the ion beam during a certain period of time, the configuration memory being in static mode,
- the device is moved out of the beam and the content of the configuration memory is read and compared to the initial download,
- the device is then re-programmed from EEPROM with a new pattern, and the sequence above is repeated again.

Two configuration memory patterns were used alternatively during this SEE test in order to avoid any influence of a specific pattern on the results.

SEU Test Results

The cross section versus effective LET derived from the tests performed in IPN and JYFL is presented in figure 1.

Figure 1. Cross section (cm2/bit)= f(LET) for configuration memory at 3V (IPN & JYFL, 4 parts used)



The mathematical description of this cross section versus LET for the configuration memory is (in cm²/bit):

$$Xs = 3e\text{-}8\ (1 - \exp\{-[(x-20)/40]^3\})$$

In term of error prediction in space orbit, the use of CREME96 software allowed to obtain the results presented in the table 1. This table 1 gives only examples of orbits and

conditions, the previous mathematical description allows to simulate other space conditions and evaluate the probability of errors for a dedicated space mission.

Table 1. Configuration memory error rate in space

Orbit	Conditions	Configuration memory error rate / device / day
GEO	Solar Min 100 mils Alu shielding Z=1 to 92	2.5E-6 (a MTTF of 1100 years)
LEO (53°/1000km)	Solar Quiet 100 mils Alu shielding Z=1 to 92	1.5E-7 (a MTTF of 18000 years)

As shown in the table 1, the possible occurrence of a SEU event in the configuration memory of the FPGA AT40KEL040 is very low.

Anyway, some simple methods to mitigate this very rare event could be put in place if felt necessary to fully secure the use of this SRAM based FPGA in space. It is for example possible to periodically reload the configuration memory from a serial EEPROM.

Single Event Latch-up Test Results

The AT40KEL040 FPGA does not exhibit any single event latch-up up to 70 MeV/mg/cm2 (maximum LET used for the test).

1 Mbit EEPROM AT17LV010-10DP Radiation Test Results

The AT40KEL040 SRAM based FPGA can be re-programmed with the AT17LV010-10DP, a 1Mbit Serial EEPROM from Atmel. This section gives some information about the total dose and SEE sensitivity of this 1Mbit EEPROM.

A total dose test has been performed in accordance with 1019.5 MIL STD 883 test method at low dose rate, with 20 parts, 10 with a 3.6V bias and 10 unbiased. All the biased parts passed all read and electrical tests up to 20 krad(Si). All the unbiased parts passed all read and electrical tests up to 40 krad(Si). When the AT40KEL040 FPGA is not in configuration mode, it is thus recommended to power off the AT17LV010-10DP EEPROM so as to increase its mission life time capability.

No Single Event Latch-up has been observed up to 80 MeV/mg/cm^2 (maximum LET used for the test) on the AT17LV010-10DP product.

Heavy ions SEU testing of the AT17LV010-10DP has shown that from a LET of 6 MeV/mg/cm^2 some permanent functional errors during read operation could occur (pattern offset). A power off/power on of the device allows a full functional recovery. In addition, the initial data can be read again, i.e. no corruption of the data stored in the memory cells has been noticed. It is thus recommended to use the checksum function implemented on the AT40KEL040 FPGA when configuring it from the AT17LV010-10DP, and to resume the configuration in case a checksum error is detected during the configuration download.

Conclusion

The AT40KEL040 reprogrammable SRAM based FPGA was developed by Atmel using SEU hardening design techniques and manufactured using a radiation hardened process.

The radiation test results illustrate the benefit of such an approach. This FPGA has a radiation capability of 200 krad(Si). There is no single event latch-up up to 70 MeV/mg/cm^2. The occurence of loss of configuration due to any Single Event Effects is lower than once every 1000 years per device, if all configuration memory bits are actually used. This product is therefore very well suited to answer to the needs of the space community in term of radiation tolerancy.

The other SEE errors usually met for that kind of FPGA devices, such as functional upsets or architectural upsets, were not addressed in this paper. However, as the same hardening method was applied to the user logic and memory as well, the SEE test results are in line with the requirements of space applications. Additional test results on that respect are available on demand.

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