REVISIONS

Rev No.	ECO No.	Description	Checked	Approved	Date
A	30-032	AE2 Initial Release			12-06-02

NOTES:

1. This schematic sheet is fo documentation purposes only.
   It can serve as a central point of reference for this board.
   See the file WhatsInaName.txt in the bp project directory
   for John Doty's description of netlist generation.
   This design consists of two parts:
   a) Connector pinout lists, and
   b) the schematic sheets filters.1 and filters.2
2. The backplane design is the same for EM1 and EM2
   Schematic revs are 1.0
   Netlist and Partlist text files are designated as rev A

NAME	DATE
Drawn: FJLAROSA	12-03-02
Checked:	
Approved:	
Released:	

MIT CENTER FOR SPACE RESEARCH

ASTROE-2

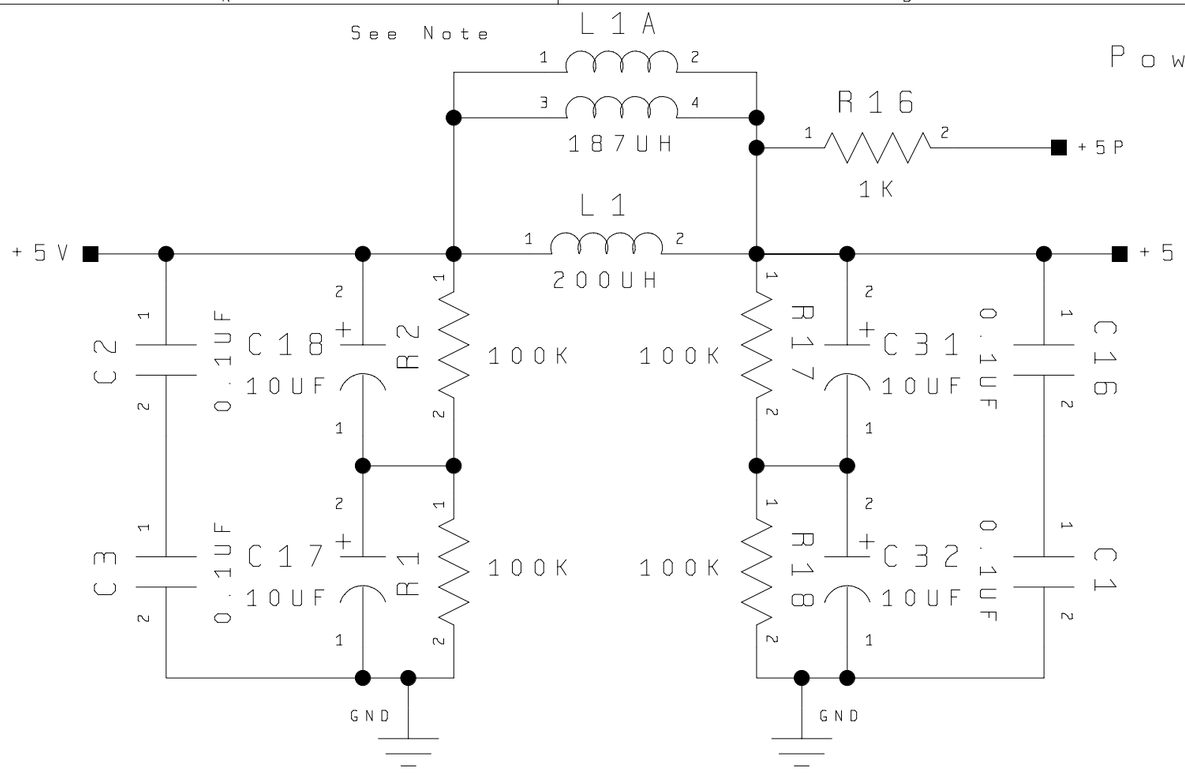
XIS BACKPLANE

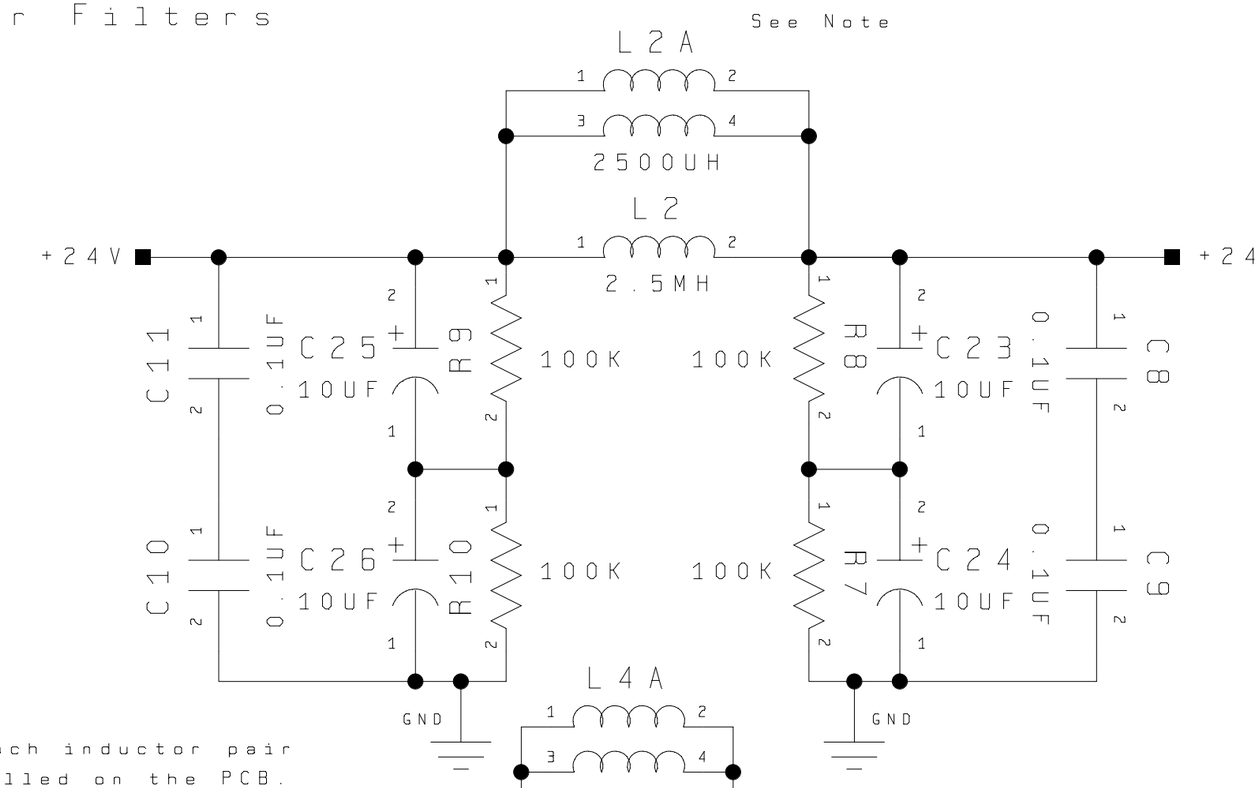
Sheet filename: backplane.1

Size	Code Identification No.	Drawing No.	Rev.
B		30-05001.01	A

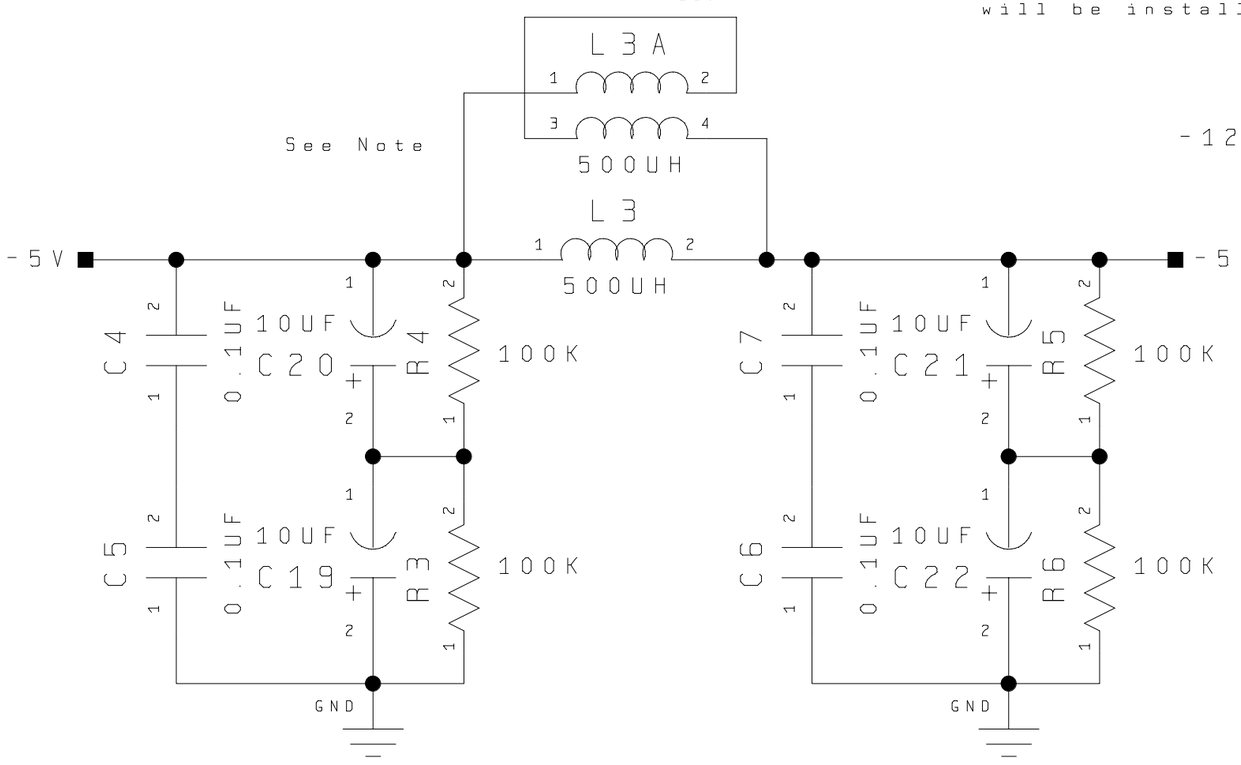
Scale: | Sheet: 1 of 10

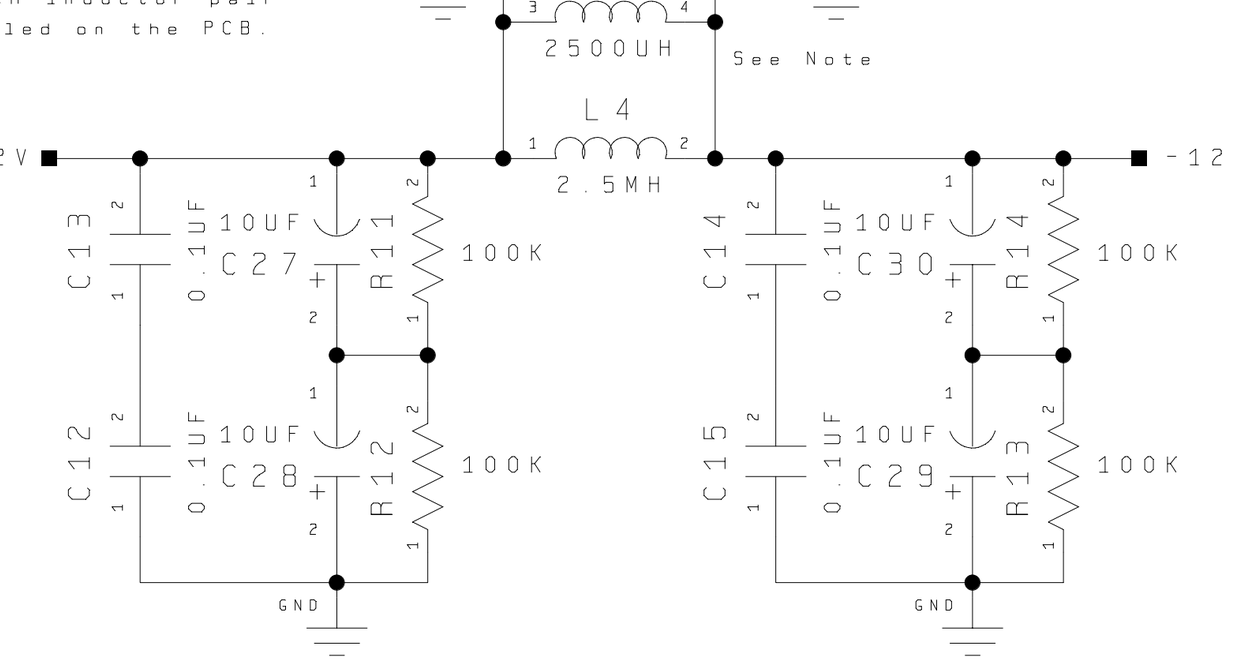
Power Filters





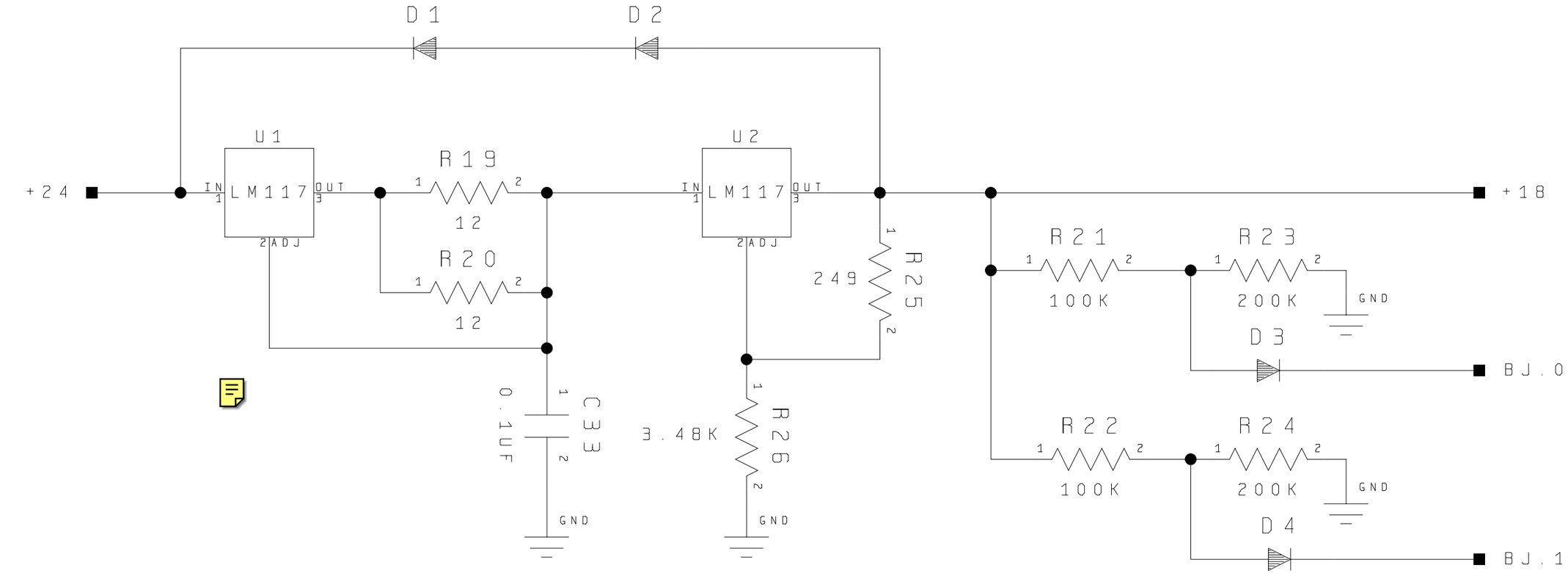
Note: Only one of each inductor pair will be installed on the PCB.

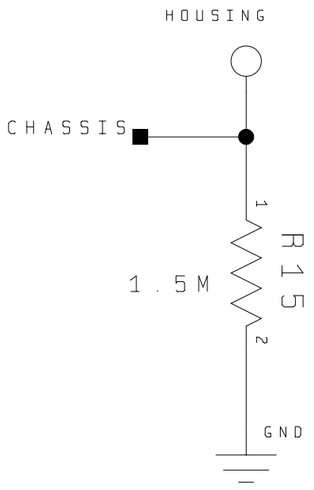




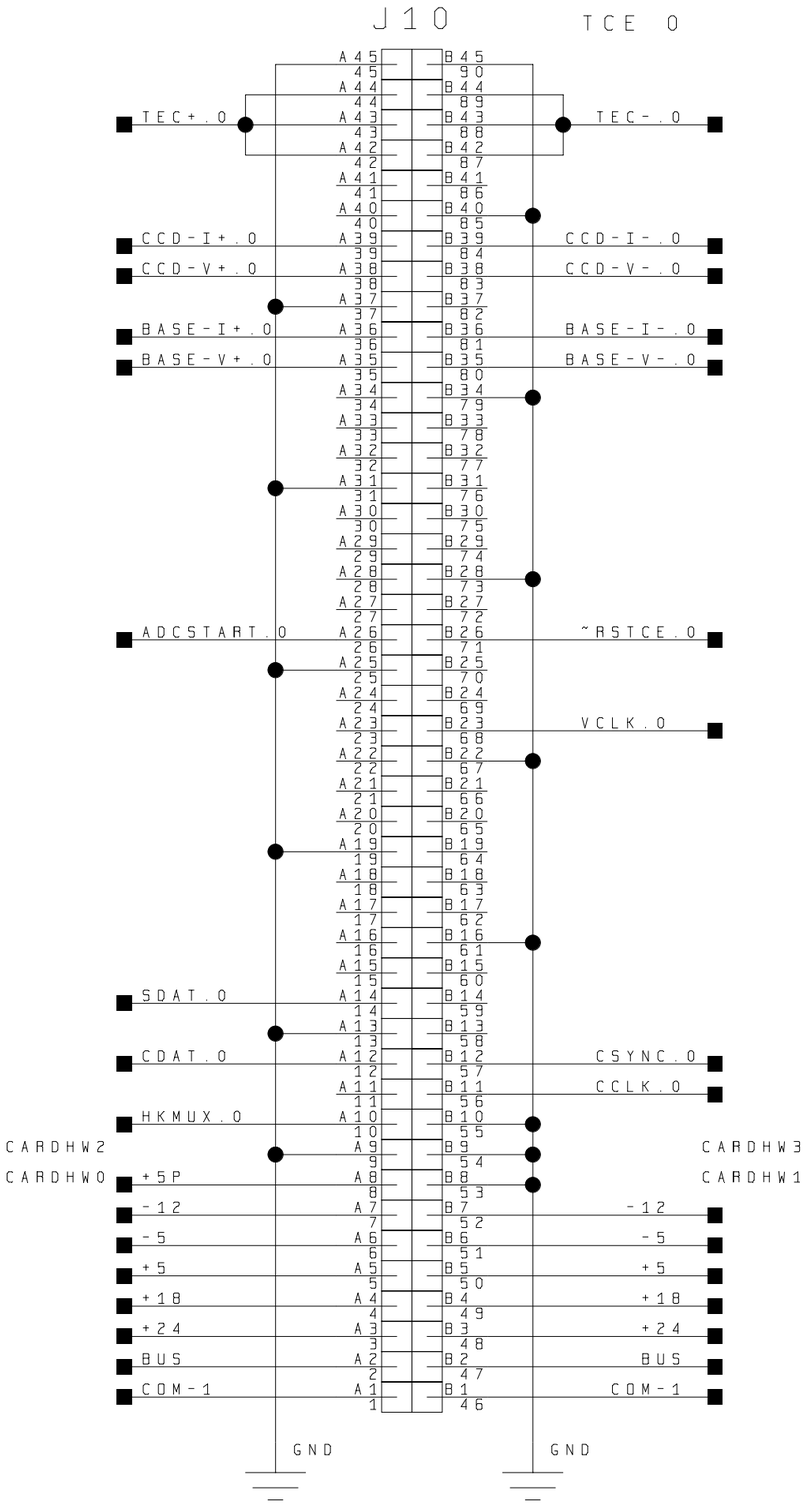
MIT Center for Space Research — CCD Laboratory			
ORIG: John Doty 2/8/96		DRAWING: XIS AE2 Backplane	
CHK: Edited FJL 11/16/96	SIZE B	SCALE N/A	SHEET 2 REV=A

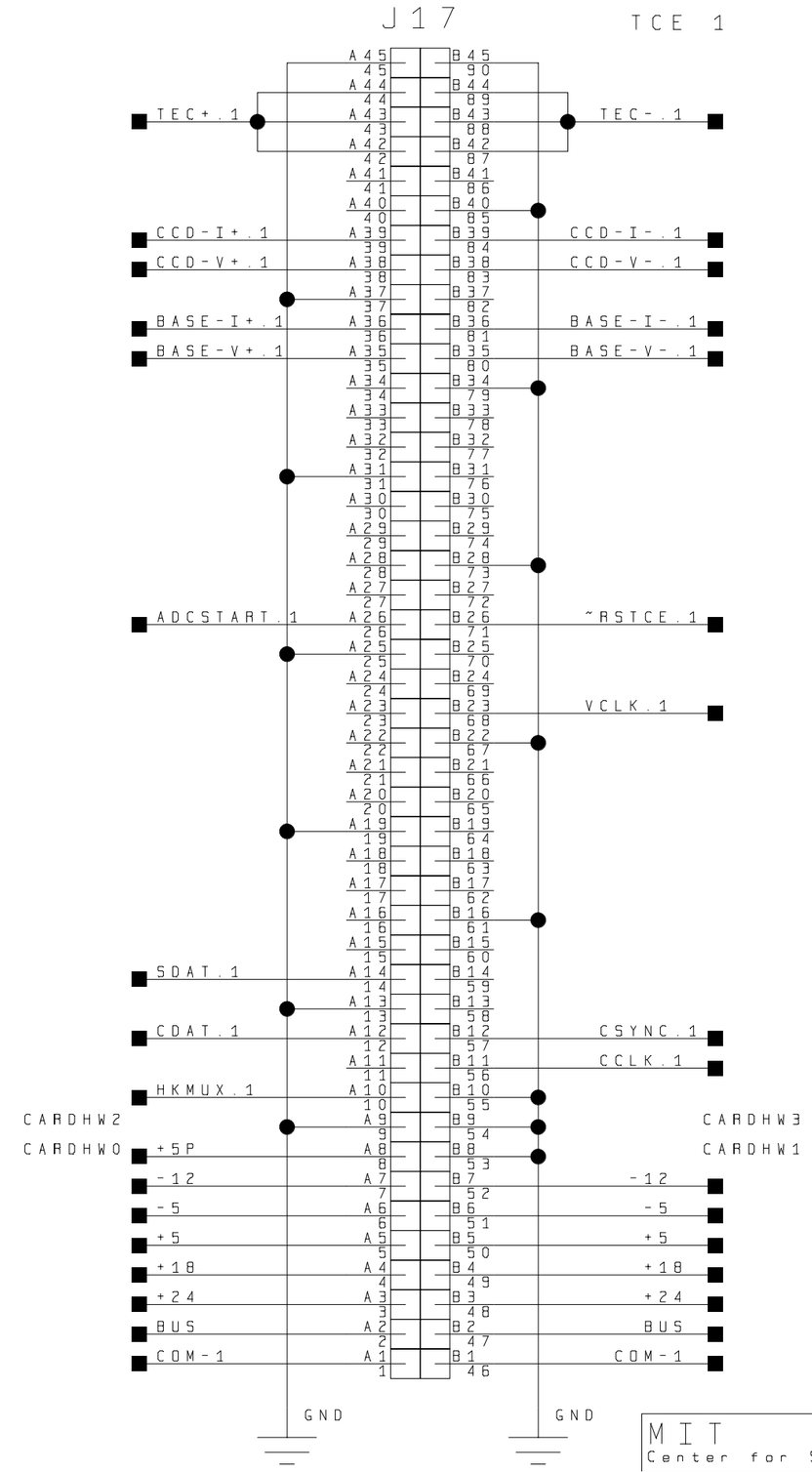
18V Regulator





MIT CCD Laboratory Center for Space Research			
ORIG: John Doty 2/8/96		DRAWING: XIS AE2 Backplane	
CHK: Edited FJL 11/16/96	SIZE B / SCALE N/A / SHEET 3 REV=A		





TCE BACKPLANE CONNECTORS 0 & 1

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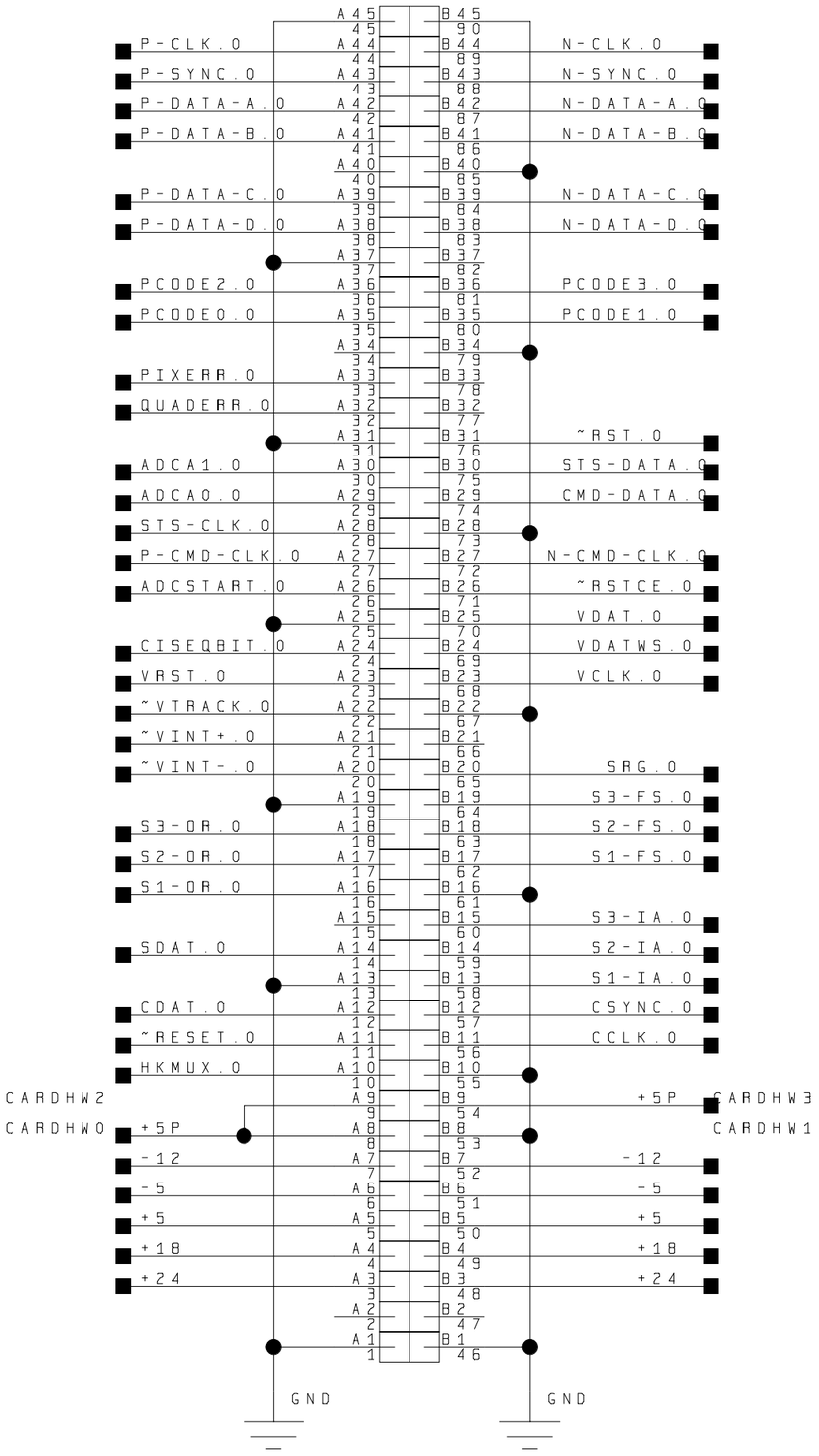
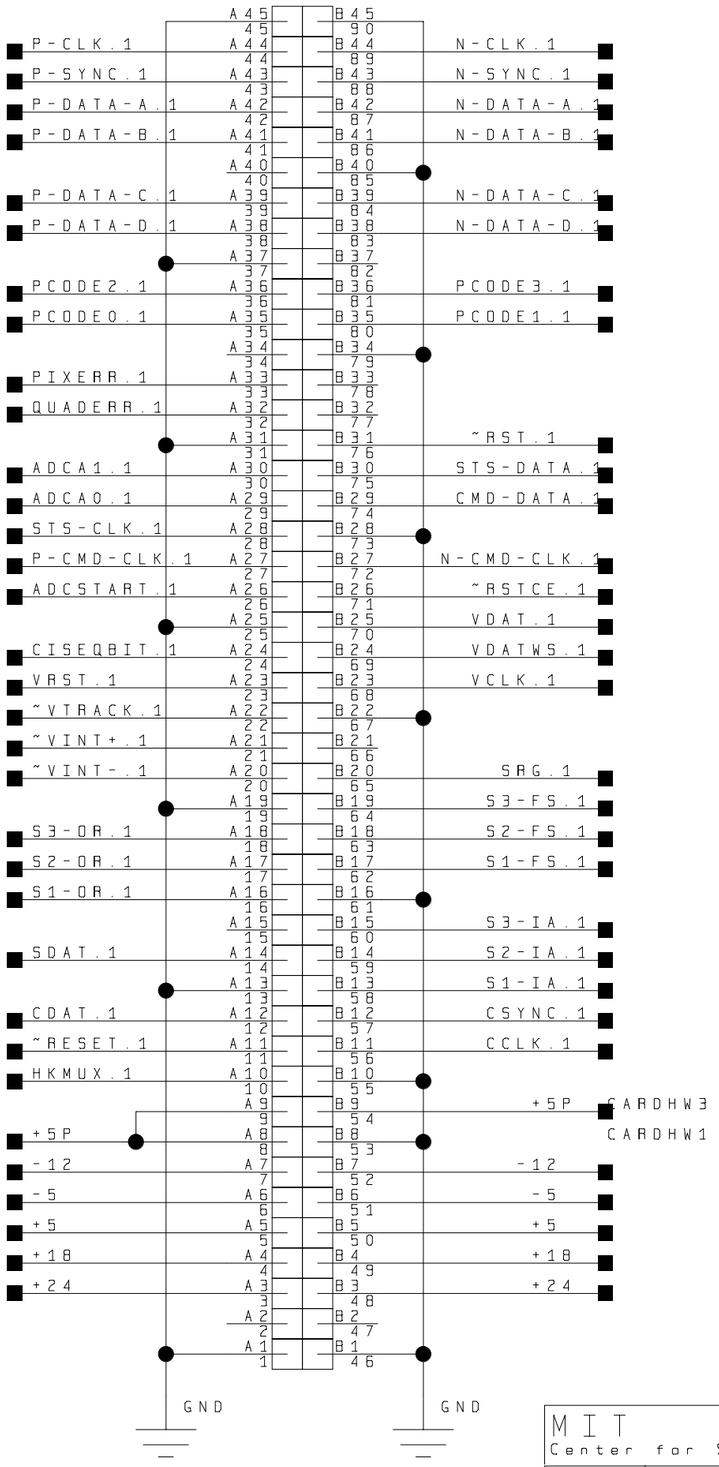
Center for Space Research

ORIG: FJLAROSA 12-03-02		DRAWING: XIS AE2 Backplane	
CHK:	SIZE B	SCALE N/A	SHEET 4 REV=A

J11 CONTROLLER 0



J16 CONTROLLER 1



CONTROLLER BACKPLANE CONNECTORS 0 & 1

MIT CCD Laboratory Center for Space Research			
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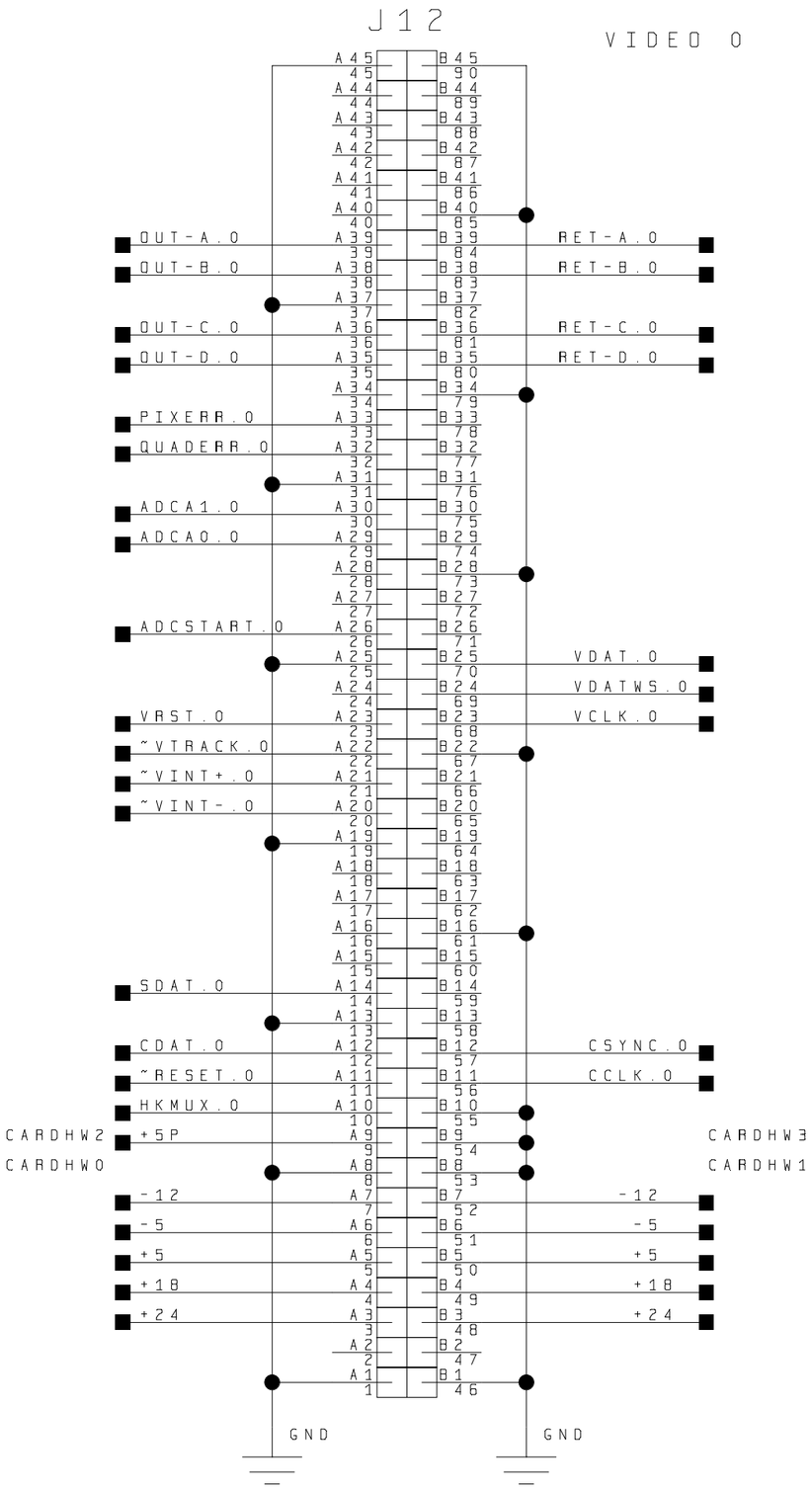
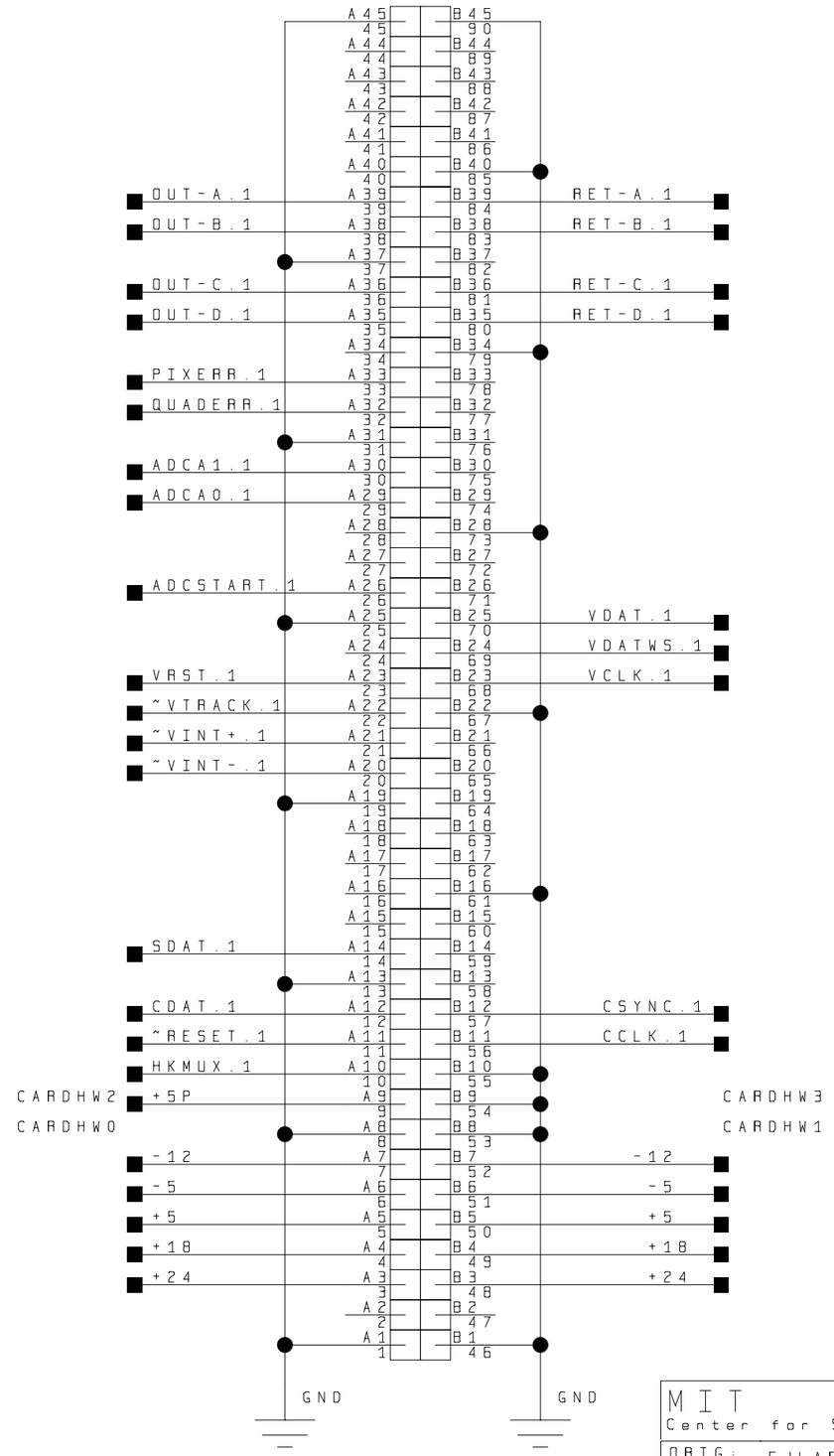
CHK:	SIZE B	SCALE N/A	SHEET 5 REV=A





VIDEO BACKPLANE CONNECTORS 0 & 1

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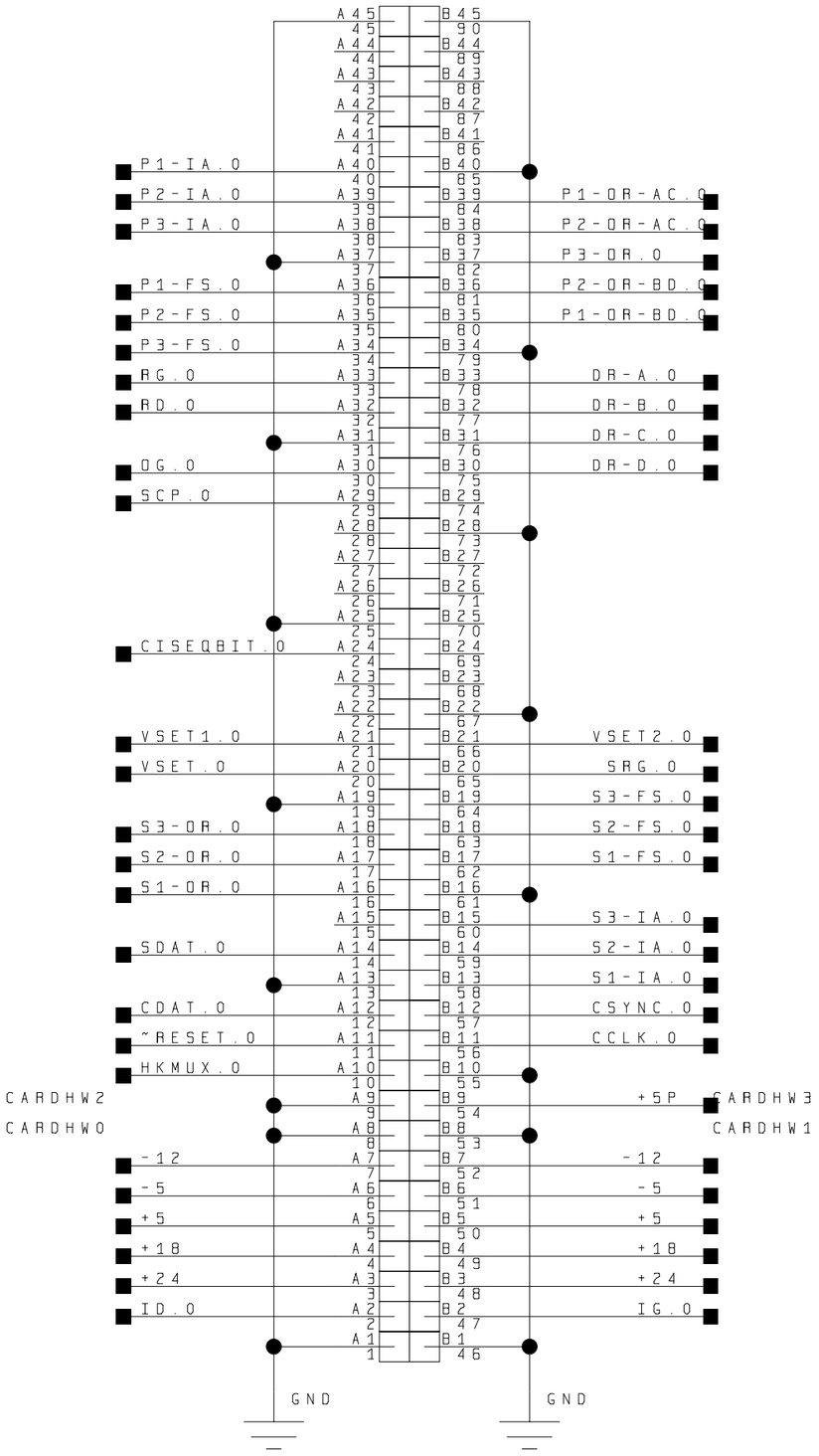
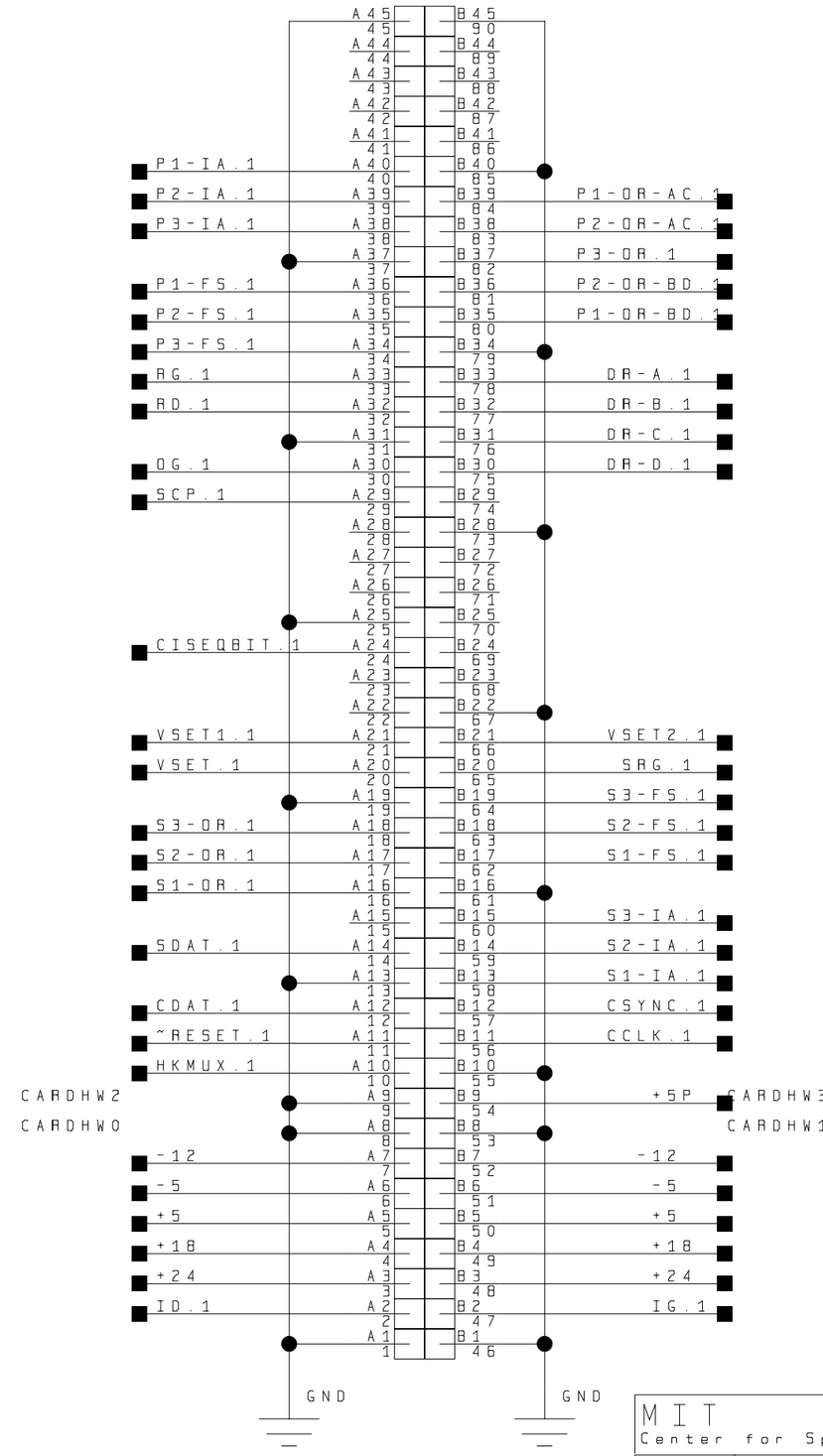
ORIG: FJLAROSA 12-03-02		DRAWING: XIS AE2 Backplane	
CHK:	SIZE B	SCALE N/A	SHEET 6 REV=A

J13 DRIVER 0



J14 DRIVER 1



DRIVER BACKPLANE CONNECTORS 0 & 1

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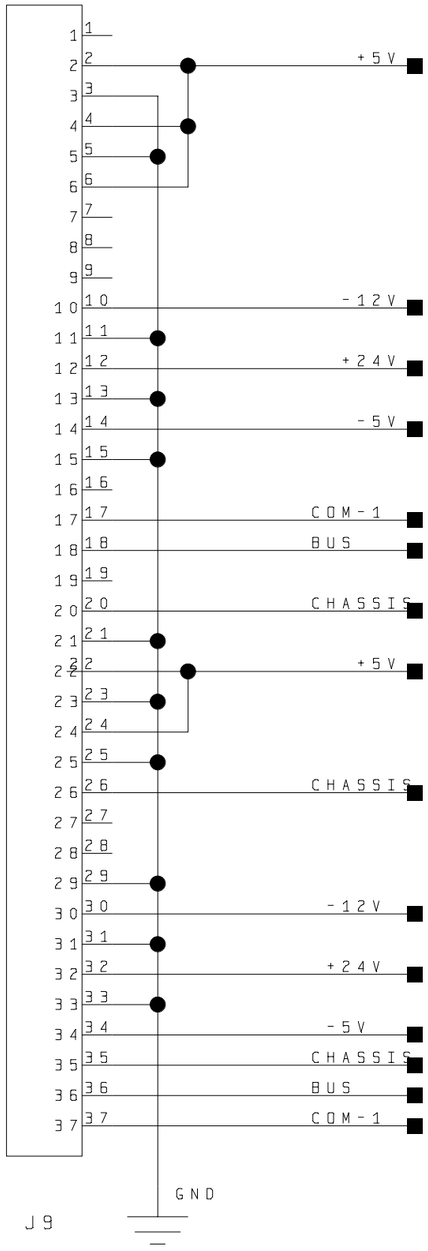
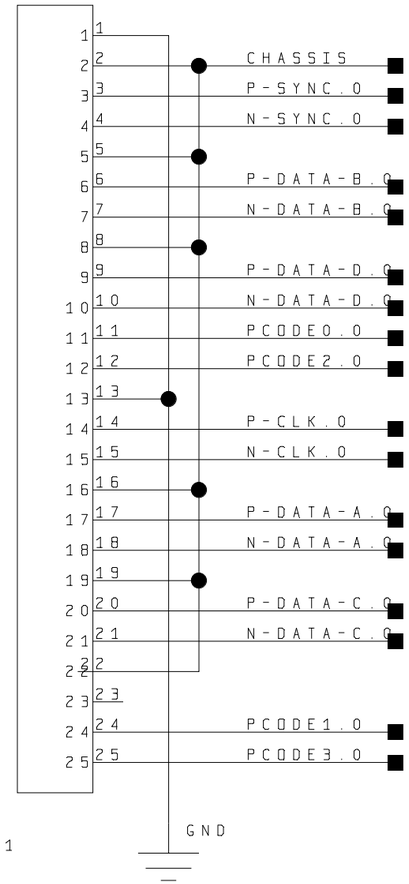
ORIG: FJLAROSA 12-03-02	DRAWING: XIS AE2 Backplane		
CHK:	SIZE B	SCALE N/A	SHEET 7 REV=A

PSU (D37)



PPU 0 (D25)



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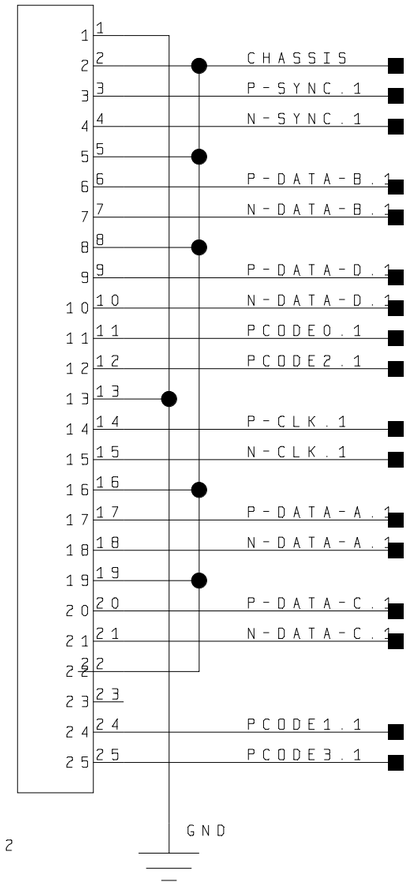

PSU CONNECTOR and

PPU CONNECTORS 0 & 1

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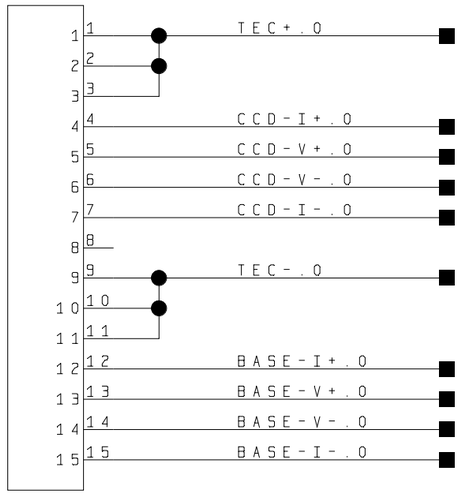
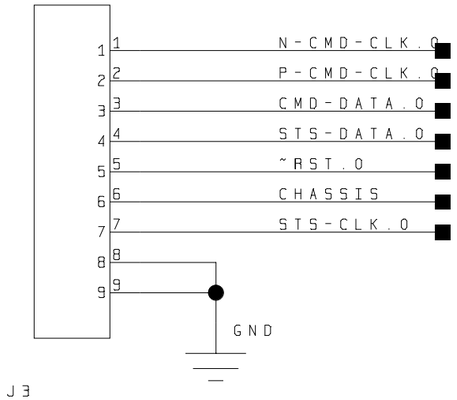
ORIG: FJLAROSA 12-03-02	DRAWING: XIS AE2 Backplane		
CHK:	SIZE B	SCALE N/A	SHEET 8 REV=A

TEC 0 (D15)



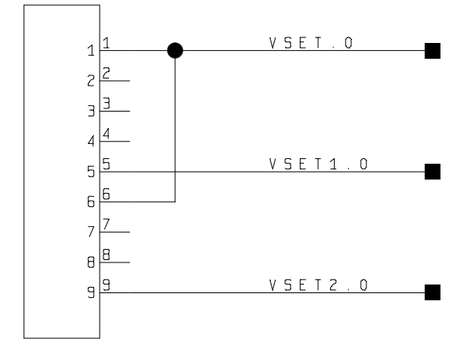
J7

MPU 0 (D9)



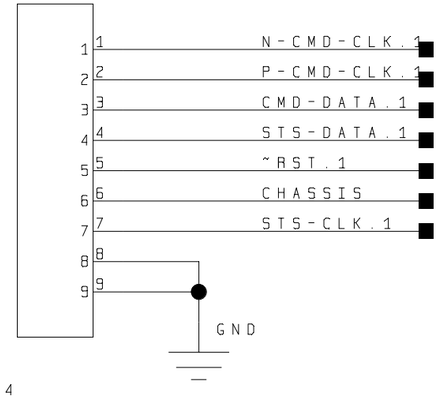
J3

IGOFFSET 0 (D9)



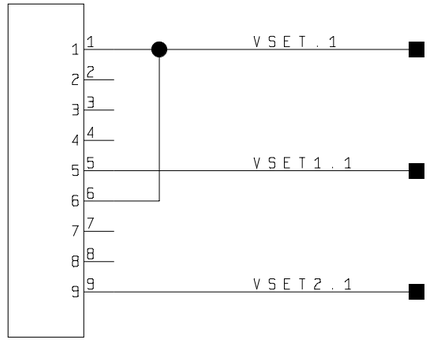
J18

MPU 1 (D9)



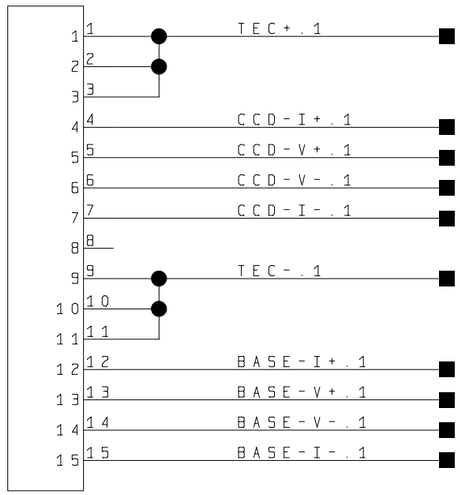
J4

IGOFFSET 1 (D9)



J19

TEC 1 (D15)



J8

TEC CONNECTORS 0 & 1
MPU CONNECTORS 0 & 1
IGOFFSET CONNECTORS 0 & 1

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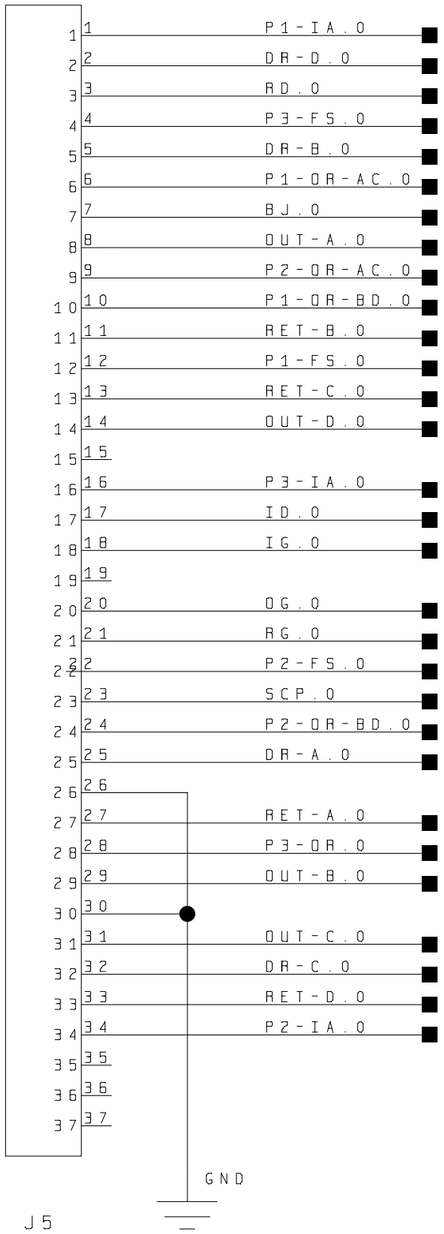
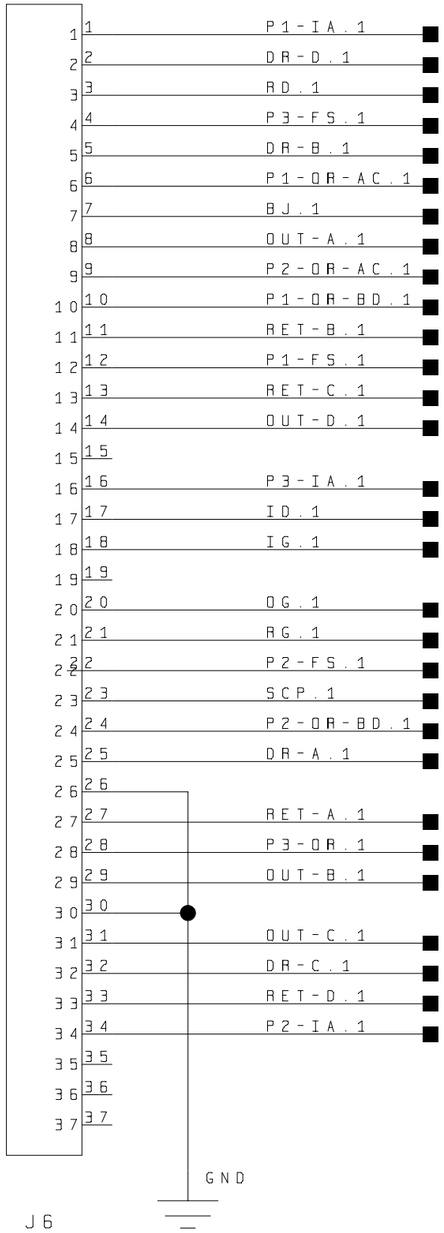
ORIG: FJLAROSA 12-03-02			DRAWING: XIS AE2 Backplane
CHK:	SIZE B	SCALE N/A	SHEET 9 REV=A

CCD 0



CCD 1



CCD CONNECTORS 0 & 1

(TO POSITRONICS CONNECTORS)

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ORIG: FJLAROSA 12-03-02	DRAWING: XIS AE2 Backplane
CHK:	SIZE B | SCALE N/A | SHEET 10 REV=A